A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process

Hugo França-Santos [a]

[a] CERN, 1211 Geneva 23, Switzerland

hugo.franca.santos@cern.ch

Abstract

This paper presents a 10-bit analogue to digital converter (ADC) that will be integrated in a general purpose charge readout ASIC that is the new generation of mixed-mode integrated circuits for Time Projection Chamber (TPC) readout. It is based on a pipelined structure with double sampling and was implemented with switched capacitor circuits in eight 1.5-bit stages followed by a 2-bit stage. The power consumption is adjustable with the conversion rate and varies between 15 and 34mW for a 15 to 40MS/s conversion speed. The ADC occupies a silicon area of 0.7mm^2 in a 0.13µm CMOS process and operates from a single 1.5V supply.

I. Introduction

Time Projection Chambers (TPCs) are one of the most widespread particle detectors for high energy physics. The largest TPC to date (88 m^3 in volume) is the core of the "*A Large Ion Collider Experiment*" (ALICE) [1] built at CERN for the "*Large Hadron Collider*" (LHC) particle accelerator. Future planed TPCs (e.g. LCTPC, CLIC and Panda) entail even higher spatial resolution in larger gas volumes hence require readout electronics with an unprecedented high density, low power and low mass. The state of art front-end electronics for TPCs is the one developed specifically for the ALICE TPC. It is based in two ASICs: the PASA and ALTRO [2], and is the groundwork for further technical improvements that will lead to a new generation of readout electronics that fully integrate low-noise amplifiers, analog-to-digital converters (ADCs) and digital signal processing in a single chip.

The ADC presented in this paper is one of the components of a general purpose charge readout chip that is being developed at CERN and meets these requirements providing at the same time flexibility for covering most of the upcoming TPC facilities. It offers adequate features in terms of speed and resolution with a reasonable power consumption and die area; therefore it is suited for an ASIC that incorporates 16 to 32 channels.

II. ADC Architecture

The pipelined analogue-to-digital conversion architecture is the one that best suits the constraints of this System-on-Chip (SoC) and is the preferable architecture for most applications that require ADCs with resolutions between 10 and 14-bit with speeds up to 300MS/s. The break-up of the conversion process combined with several circuit artifices enable the implementation of a high-performing structure with relatively little hardware.

A. Pipelined ADC Block Diagram

The pipelined ADC is established in an effective architecture that distributes the quantization along an analogue handling sequence with multiple stages. Each one subtracts part of the pertinent information from the sampled signal and passes the residue to the following stage until the last one, which contains only the sub-ADC function. The outputs of these series of high-speed low-resolution conversion stages are combined afterwards to achieve a high-speed high-resolution ADC.

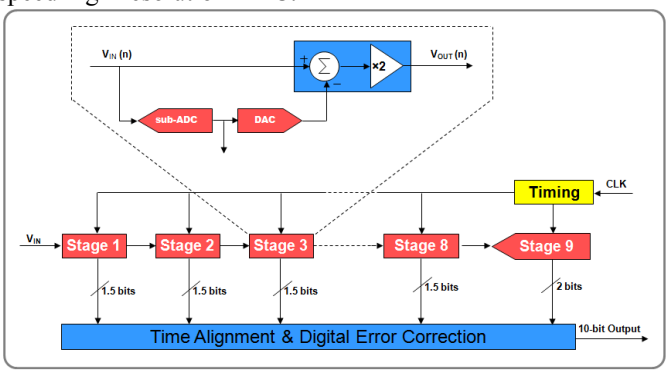

Figure 1: Pipelined ADC architecture

An arrangement of eight 1.5-bit plus one 2-bit stage was chosen for this design since it offers good trade-offs for the speed and resolution required.

B. Double Sampling

A slice of 90 to 95% of the power consumption of the pipelined ADC goes to the OTAs, therefore these are the most important circuits to improve in terms of power efficiency. In a standard pipelined configuration, at a given time, half of the stages are in the sampling phase and the other half in the multiplication phase, hence, only half of the amplifiers are actually being used simultaneously however all are consuming power. Several modifications to the standard multiplying digital-to-analog converter (MDAC) that fully exploit the OTAs exist, the one used in this work is the double sampling technique that was first introduced in the 80's by Choi and Brodersen [3]. It consists on the duplication of the switch capacitor circuitry allowing the parallel execution of the sampling and multiplication operations as shown in Figure 2.

This circuit has greater power efficiency since it allows the reduction of the OTAs bandwidth to half but also suffers

from several draw-backs. It occupies more die area, given that it has twice the number of capacitors, which are relatively big for matching reasons; it has a memory effect that arises from the suppression of the OTA reset phase, so, a fraction of each sample remains stored in the parasitic capacitance of the OTAs input, due to their finite gain and incomplete settling [4], and is added to the next sample. This error can be negligible if the OTA has a considerable higher gain than the minimum required for the corresponding ADC resolution, which is the case in this design.

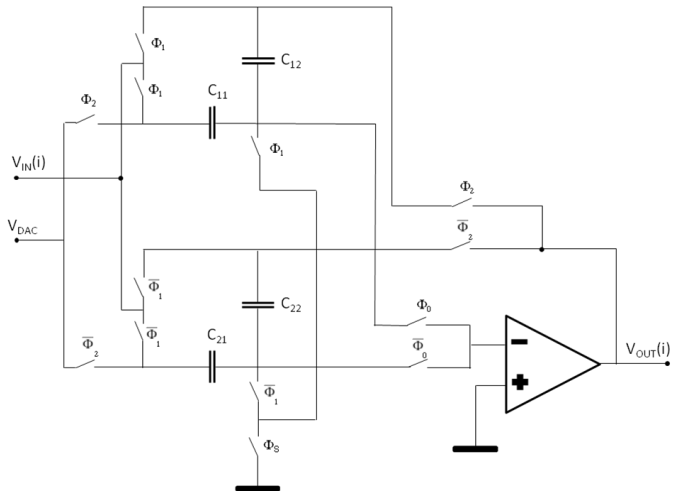

Figure 2: A double sampling MDAC

Another potential problem of the double sampling is the gain error that may arise from mismatches between the ratios C_{12}/C_{11} and C_{22}/C_{21}, and an additional problem that may also take place is a different offset between even and odd samples, the reason being a mismatch in the charge injection of the switches Φ_0 and $\overline{\Phi}_0$.

The clocking circuitry that divides the frequency by two and delivers it to the sampling switches is very likely to introduce a different timing skew to the parallel track-and-hold (T/H) switches. When the input is a sine wave the error turn out to be a tone at the frequency $F_S/2 - F_{IN}$ [5]. In this design, a changing of the sampling circuit permitted the removal of this problem [6]. The idea was to introduce a new switch that synchronized the two parallel T/Hs, terminating the sampling phase (turning off) just before the switches Φ_1 or $\overline{\Phi}_1$ depending on the phase being odd or even.

C. *Sub-ADC Threshold Levels*

In the 1.5-bit per stage configuration, the redundancy of the sub-ADCs allows to set the thresholds in the range of $0 < \pm V_{TH} < \pm \frac{1}{2} V_{REF}$, so, typically these thresholds are set to the value that maximizes the error tolerance and that is in the middle of the allowed range: $\pm\frac{1}{4}V_{REF}$ [7] [8] [9]. On the other hand, the error introduced by the capacitors mismatch is proportional to the amount of charge transferred between them as depicted in the Figure 3. It is noticeable in this figure that there is a relationship between the threshold positions and the effect of the capacitor mismatch. The error increases linearly as the input signal deviates from the reference voltages and from the common mode voltage since there is a greater charge transfer. The value of the thresholds that would minimize the error is $\pm\frac{1}{2}V_{REF}$ however it would require very accurate comparators and would not tolerate any timing disparity between the triggering of the sub-ADCs and the triggering of the T/H, which exists in this design as will be explained later in the section III-D.

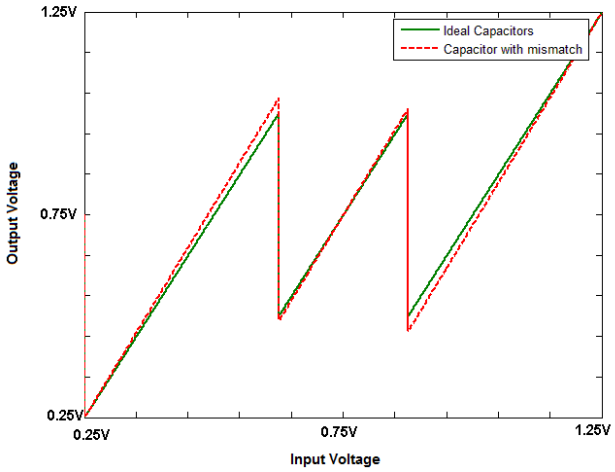

Figure 3: Capacitor mismatch effect

In this design the thresholds were set to $\pm\frac{3}{8}V_{REF}$ because the Monte Carlo simulations showed that an error margin of $\frac{1}{8}V_{REF}$ was still large enough. In a pipelined ADC with 1.5-bit per stage, the improvement in terms of reduction of INL is 12.5% in each stage. Since the capacitor mismatch contribution to the INL is divided by two as the stage number increases the total reduction of is 24.9% in a 10-bit ADC if there is no stage scaling; or even more if there is a capacitor scaling factor.

III. CMOS IMPLEMENTATION

The ADC presented here is fully differential since it offers the double of the output swing, which is convenient in low voltage designs; and superior tolerance to power supply noise, that can be critical in a mixed-signal circuit like this one. It operates from a single 1.5V power supply and occupies a die area of $0.7mm^2$.

A. *Operational Amplifier*

The operational amplifier is the fundamental block that dictates the performance of the switched-capacitor pipelined ADC. The maximum speed and, to a large extent, the power consumption of the ADC are determined by the operational amplifier that at the same time is the block where the limits of the technology are meet [5].

The selected amplifier has two stages: a gain boosted telescopic amplifier input stage and a rail-to-rail output stage.

The common mode feedback is continuous in time being sensed with a resistor/capacitor divider.

The frequency compensation is both direct (or Miller) with a nulling resistor and indirect. This gives the best control over the phase margin of the main amplifier and the common mode loop, (71º and 57º respectively) keeping the bandwidth loss reasonable.

The first stage of the amplifier is the one that most contributes to the gain since it provides 72.7dB, the second stage contributes with 30.3dB, making a total of 104dB and a unitary gain bandwidth of 332MHz in the simulated version.

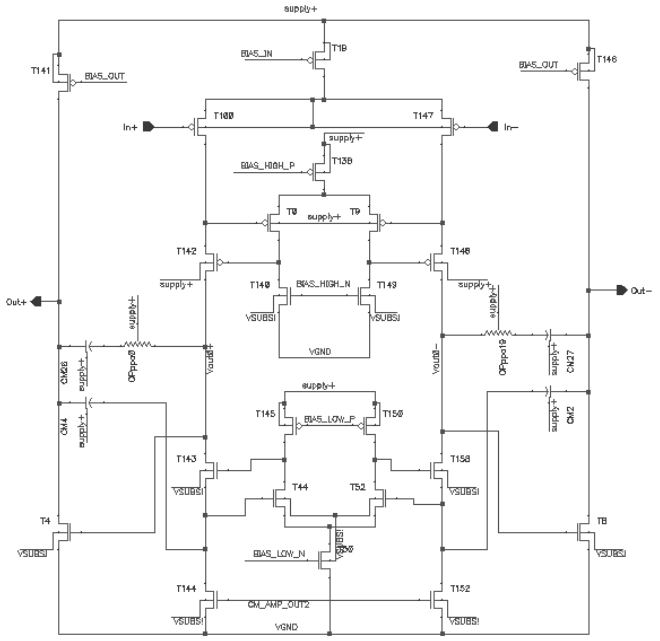

Figure 4: Operational Amplifier

After the parasitic extraction of the layout, considering resistors and capacitors, these values changed to 101dB and 326MHz. It consumes 4mW in normal speed i.e. for operating the ADC at 40MS/s.

The biasing circuit is based in the beta-multiplier principle that provides constant Gm over a wide range of temperature. It is externally regulated and independent of the process parameters [10].

B. Track & Hold Switches

The sampling switches were implemented with complementary low-threshold FETs. Since a low on-resistance is required these transistors are relatively large and consequently inject a considerable amount of charge when they change their on/off state, this phenomenon is called clock feedthrough. If no measures were taken this charge would contaminate in a non-linear way the sample that is stored in the capacitors. To reduce this effect, two dummy transistors were added by the sides of each active switch, each one injecting half of the charge that the active one injects but with opposite signal, reducing considerably the amount of input dependant charge injection [11].

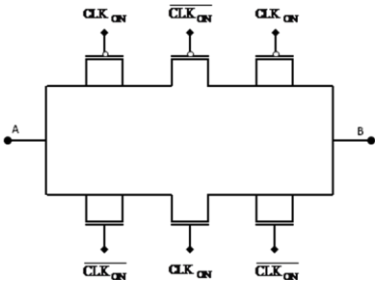

Figure 5: Transmission gates with charge cancellation

Another important constraint of the sampling switches is their linearity over the input range of the ADC. The non-linear trait of the transmission gate switches introduces a distortion that can affect the overall performance of the ADC, especially at high input frequencies. In the next figure is shown the on-resistance over the power supply range of three transmission-gate switches: minimum length regular V_T, minimum length low-V_T and low-V_T with optimized length.

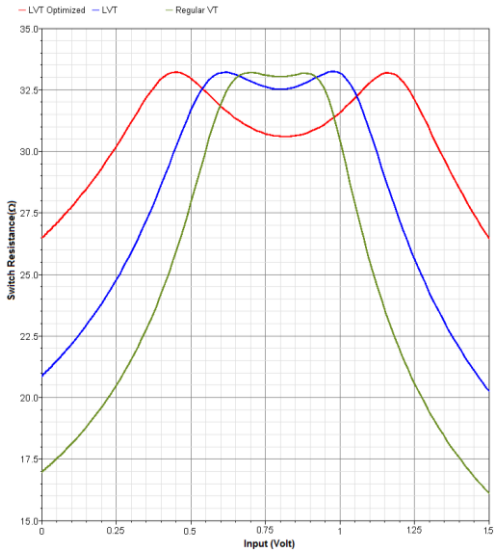

Figure 6: On-resistance of transmission gates

The voltage range that was considered in the analysis is comprised between 250mV and 1.25V since it corresponds to the full range of the ADC. The maximum on-resistance is determined by the time constant of the sampling and was set to 33Ω for the various switches in comparison. The on-resistance of the regular V_T switch has a variation inside the range in the order of 12Ω; in the low-V_T switch this value is reduced to 8Ω and in the optimized one even further reduced to only 3Ω. To measure the effect of this non-linearity a simulation with a full amplitude sine wave at the maximum input frequency (20MHz) was done and consequent harmonic distortion is depicted in the next figure.

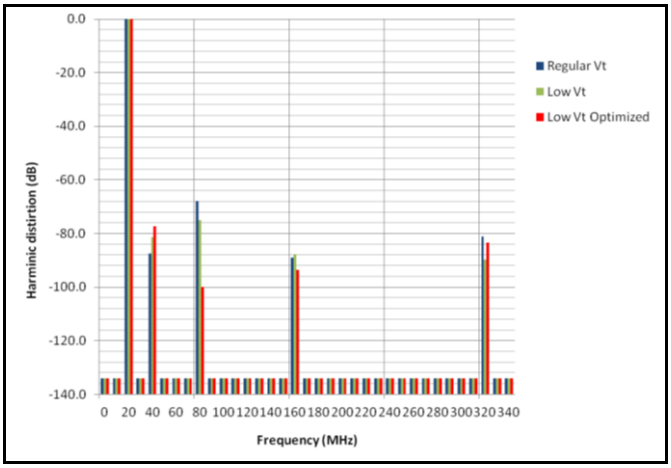

Figure 7: Distortion of transmission gates

This analysis has shown a reduction of the highest spurious harmonic from -68dB to -77dB with typical process parameters and this value increased to -72dB in the process

corner fast-slow. These magnitudes of distortion are still tolerated by a 10-bit ADC given that it has an intrinsic quantization noise of -62dB.

C. Comparators

The precision requirements for the comparators are not very strict, however they should be fast and should not introduce a relevant kick-back noise. The selected architecture is called resistive divider latched comparator; it was introduced by Cho and Gray [12] and became a widely-used comparator in pipelined ADCs.

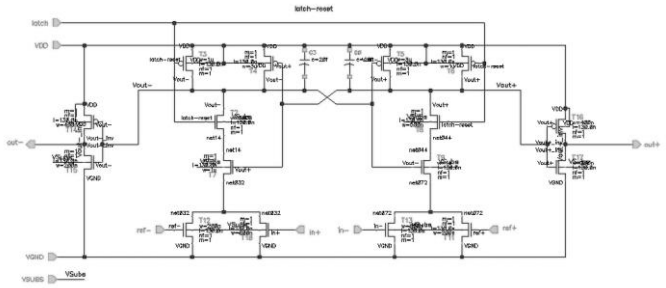

Figure 8: Resistive divider latched comparator

The comparator used in this design is similar to the originally published circuit but with the adding of one capacitor in each branch to make it less vulnerable to mismatches of the transistors, hence more accurate.

The setting of the thresholds is done according to the principles described in section II-C, so:

$$IN_+ - IN_- = \pm\frac{3}{8}(REF_+ - REF_-)$$

This is translated into two comparators. One does the comparison:

$$IN_+ + \frac{3}{8}REF_- = IN_- + \frac{3}{8}REF_+$$

and the other one:

$$IN_+ + \frac{3}{8}REF_+ = IN_- + \frac{3}{8}REF_-$$

therefore the width of the transistors connected to the reference voltages are ⅜ the width of the ones connected to the inputs, both having the same length.

D. Clocking

The circuit that generates the clocks for the various blocks of the ADC is complex and for practical reasons will not be shown here, however the most important features will be described.

The main clock drives two distinct branches: one that works at half clock speed and another that operates at full clock speed. The first one is applied to a non-overlapping clocking circuit that provides the clock sequencing for the double-sampling MDACs; the second triggers the sub-ADCs and the synchronization switches Φ_S as explained in the section II-B.

For the sampling operation, the switches of the MDACs turn off in a sequence that minimizes the charge injection and in particular the input signal dependency; this is done by the well-known bottom plate sampling technique [13].

For minimizing the effect of the kick-back noise introduced by the latched comparators in the sample, the triggering of the MDAC of the first stage is done slightly after the triggering of the corresponding sub-ADC. This introduces a desynchronization between the MDAC and the sub-ADC however this error can be seen as an additional error in the thresholds of the comparators and will not influence the performance of the ADC since it has enough margin of redundancy.

The triggering of the Φ_S is done with a small delay from the input clock since the bigger the skew the bigger the clock jitter, which can compromise the performance of the ADC at high input frequencies.

E. Layout

A two-channel prototype of this ADC was built in a multi-project wafer (MPW); the layout is shown in the next figure.

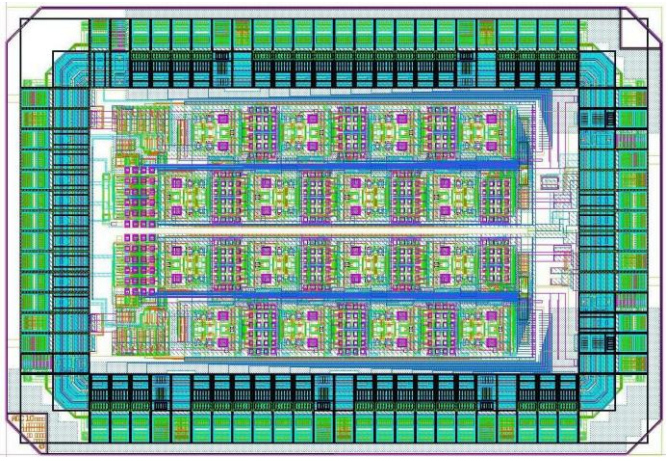

Figure 9: Chip layout

For a maximum level of testability the outputs from the stages are directly connected to the output pads, so the data alignment and the redundant sign digit code blocks are implemented outside, in the test system.

The digital and the analogue domains are properly separated at the various levels: pads, power distribution, wires and also at the substrate level using high resistivity enclosures around the digital parts.

IV. TESTING

In this prototype one channel is more focused in verifying the functionality and the other in evaluating the performance, so they have different testing capabilities; however the tests gave similar results in both channels.

A. Static characterization

The static measurements were done through the output code density method [14] using a sine wave input with the frequency 50.0488KHz that exceeded slightly the full range of the ADC. The results are depicted in the figures 10 and 11 and summarized in the Table 1.

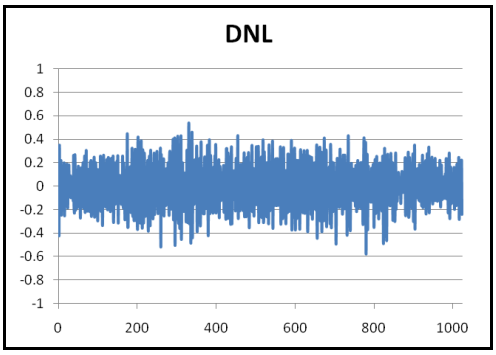

Figure 10: Differential non-linearity

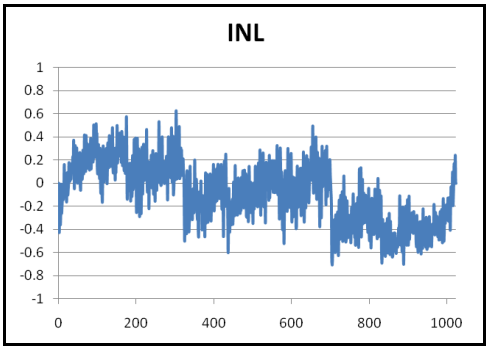

Figure 11: Integral non-linearity

	DNL	INL
MAX	0.54	0.62
MIN	-0.58	-0.71

Table 1: INL and DNL range

The maximum values of DNL and INL are below ±1LSB therefore they are within the specifications for this ADC. In the INL graph it is possible to recognize the influence of the capacitors mismatch of the first stage and confirm the influence of the selection of the thresholds according to the ideas explained in the section II-C.

B. Dynamic Characterization

A dynamic characterization was done at 20 and 40MS/s. Sine wave signals with frequencies that ranged from 1 to 20MHZ and amplitudes near the full scale of the ADC were applied to the inputs. The results ranged from 9.07 effective number of bits (ENOB) for the lowest frequency input signal to 8.63 ENOB for the Nyquist frequency.

Whilst operating at 20MS/s the power consumption could be reduced from 34mW to 26mW without any significant loss in performance.

The tests are still ongoing for a complete characterization and optimization of power efficiency for a wider range of sampling frequencies.

V. Conclusion

A 10-bit Pipelined ADC in the 0.13 um CMOS technology was presented. A switched-capacitor with double sampling architecture was used. The proper design of the switching circuitry and selection of sub-ADC thresholds enabled to deal with the low voltage constraints and reduce the sensitivity to capacitor matching. The evaluation tests revealed a performance that matched the specifications.

References

[1] ALICE Collaboration, *"ALICE Time Projection Chamber: Technical Design Report,"* Tech. Design Report ALICE, CERN-LHCC-2000-01

[2] R. Esteve Bosch, A. Jiménez de Parga, B. Mota and L. Musa *"The ALTRO Chip: A 16-Channel A/D Converter and Digital Processor for Gas Detectors,"* IEEE Transactions on Nuclear Science, Vol. 50, No. 6, December 2003

[3] Tat C. Choi and Robert W. Brodersen *"Considerations for High-Frequency Switched-Capacitor Ladder Filters,"* IEEE Transactions on circuits and systems, Vol. CAS-27, No. 6, June 1980

[4] Seyfi Bazarjani and W. Martin Snelgrove, *"A 160-MHz Fourth-Order Double-Sampled SC Bandpass Signa-Delta Modulator,"* IEEE Transactions on circuits and systems, II: Analog and Digital Processing, Vol. 45, No. 5, May 1998

[5] Mikko Waltari and Kari Halonen, *"Circuit Techniques for Low-Voltage and High-Speed A/D Converters,"* Kluwer Academic Publishers, 2002

[6] Mikko Waltari and Kari Halonen, *"Timing Skew Insensitive Switching for Double-Sampled Circuits,"* proc. IEEE ISCAS, Vol. II, pp. 61-64, May 1999

[7] Tsung-Hsien Lu, Chun-Kuei Chiu and Chin-Cheng Tien, *"A 10 Bit 40-MS/s Pipelined Analog-to-Digital Converter for IEEE 802.11a WLAN Systems,"* International Symposium on Communications, 2005

[8] Hamid Charkhkar, Alireza Asadi and Reza Lotfi, *"A 1.8V, 10-bit, 40MS/s MOSFET-Only Pipelined Analog-to-Digital Converter,"* proc. IEEE ISCAS, pp. 63-66, September 2006

[9] Geir S. Østrem, Øystein Moldsvor and Oddvar Aaserud, *"A Compact 3V, 70mW, 12-bit Video-Speed CMOS ADC,"* Analog Integrated Circuits and Signal Processing, 15, 27-36, Kluwer Academic Publishers, 1998

[10] R. Jacob Baker, "*CMOS Circuit design, Layout, and Simulation*" IEEE Press Series on Microelectronic Systems, 2008

[11] Phillip E. Allen and Douglas R. Holberg, *"CMOS Analog Circuit Design,"* Oxford University Press, 2004

[12] T. B. Cho, P. R. Gray, *"A 10 b, 20 Msample/s, 35 mW Pipelined A/D Converter,"* IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166-172, Mar. 1995

[13] D. Haigh, B. Singh, *"A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminals,"* Proc. 19h IEEE ISCAS, pp.586-589, 1983

[14] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Std 1241-2000