OMEGAPIX: 3D integrated circuit prototype dedicated to the ATLAS upgrade Super LHC pixel project

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Abstract

In late 2008, an international consortium for development of vertically integrated (3D) readout electronics was created to explore features available from this technology.

In this paper, the OMEGAPIX circuit is presented. It is the first front-end ASIC prototype designed at LAL in 3D technology. It has been submitted on May 2009.

At first, a short reminder of 3D technology is presented. Then the IC design is explained: analogue tier, digital tier and testability.

I. 3D CONSORTIUM, MULTI-PROJECT WAFER (MPW) AND PROCESS

The Handbook of 3D Integration [1] defines the 3D integration as "an emerging, system level integration architecture wherein multiple strata (layers) of planar devices are stacked and interconnected using through silicon (or other semiconductor material) vias (TSV) in the Z direction".

The more expected benefits of this emerging technology for High Energy Physics (HEP) applications are to reduce the insensitive area (in particular for the pixel sensor), add more functionalities (several CMOS technologies in the same global device) and improve the form factor (less material, more little device size).

A. 3D consortium: a large number of international institutes

In late 2008, Fermilab, U.S.A., took the initiative in gathering several international laboratories and institutes with interest in HEP to intend to bring together resources to investigate options and share cost [2].

Besides Fermilab, this consortium gathers six IN2P3 institutes in France, six Italian institutes, University of Bonn and AGH University of Science & Technology in Poland.

A MPW has been submitted on May 2009 for "only" a two layers device.

B. Chartered/Tezzaron 3D process

Among the various available 3D technologies, the process from Tezzaron was chosen. This process is wafer to wafer, face to face and since it is via first (TSVs are built in the same time than transistors) another company has to build the wafer. Tezzaron are working with Chartered which performs the wafer fabrication with TSV as a part of its foundry process.

Chartered technology is a 130 nm CMOS one with various types of transistors: 3p3, 1p5, 1p5 low Vt. It builds TSV of 6 µm length and 1,2 µm for the diameter. (See picture below, TSVs are called Super-Vias).

Then Tezzaron performs the wafer connection with the Cu-Cu thermocompression bonding technique making both electrical and mechanical connections. The alignment between the two wafers is better than 2 µm. Next, the back-side of one wafer is thinned up to reach the TSV contact: this wafer has about 12 µm thickness.

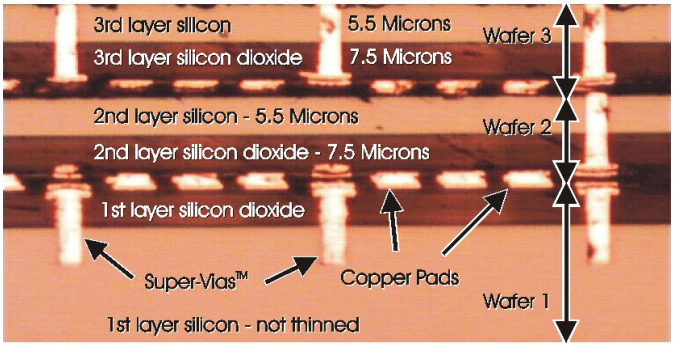

Figure 1: Picture from Tezzaron website showing a three layers device

In the picture above, we can see that the two first wafers from the bottom have been stacked in a face-to-face process (Cu-Cu pads). Then the back-side of one wafer is thinned up to reach the TSV, Cu pads are placed on each TSV and this face becomes a new "front-side" for another face-to-face stacked process. Also a large number of wafers can be stacked.

II. OMEGAPIX DESIGN

OMEGAPIX circuit embeds 64x24 readout channels that have been developed to match very drastic requirements. Into the first layer, called analogue tier, there are the analogue part of the front-end cell, a block which performs the selection of the column and the bias. Into the other layer, called digital tier, there is a shift register with a read logic into each channel.

A. Requirements

Although one of goals of this first chip is to explore this new technology, as much the 130 nm CMOS process from Chartered as reliability and yield of 3D devices from Tezzaron, requirements have been chosen in such a way they go to the future likely requirements of the ATLAS upgrade Super LHC pixel project.

So, we want to explore a new possibility to minimize the pixel pitch down to 50x50 µm. Thus a readout array matching a new MPI-HLL plannar pixel sensor prototype from Munich has been designed.

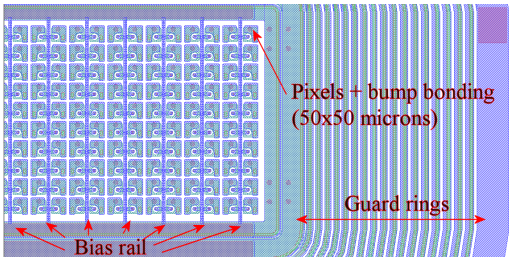

Figure 2: pixel array sensor prototype

Some specifications are given bellow:

Channel size: 50x50 µm. The first limitation of the pixel size is currently the electronics readout area.

Dissipation: 3 µW/ch. If we want to keep an equivalent power consumption after the pixel size shrinking, we have to low drastically the power dissipation for each channel. Typically the consumption should be 2.4 µW/Ch to keep the power density at 96 mW/cm². The power density has been low down to 80 mW/cm² (2 µW/ch) for the analogue tier and 40 mW/cm² (1 µW/ch) for the digital tier.

Noise: the IC has been designed to low the noise down to 100 e- and to be able to decrease the threshold down to 1000 e-.

B. Analogue Tier

The analogue channel is divided into three parts: the preamplifier, the shaper with threshold tuning and the discriminator.

The power voltage for all the analogue part, except for the discriminator, is 1.2 V.

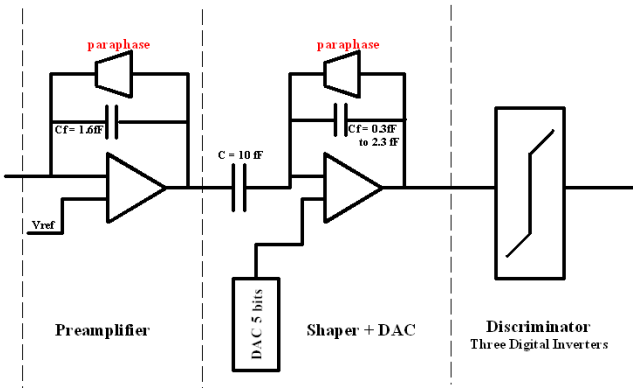

Figure 3: analogue one channel schematic

1) Preamplifier description

In order to reach the very low power requirement and low channel area, design has been done in such a way that the global capacitance has been minimized.

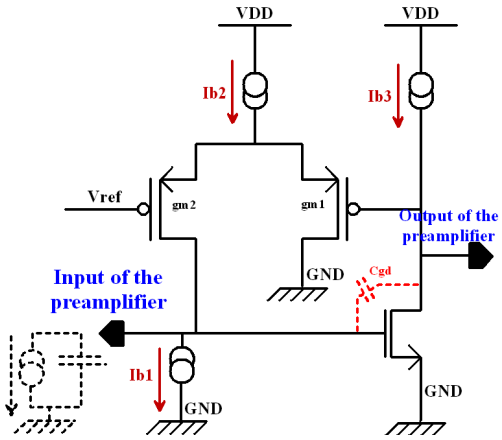

Figure 4: preamplifier schematic

The parasitic capacitance Cgd performs the feedback capacitance.

Cf = Cgd = ~ 1.6 fF

The ideal gain is 1/Cf = 100 mV/ke- or 625 mV/fC. In simulation, the gain is about 60 mV/ke- or 375 mV/fC. This lower value is due to the non infinite preamplifier open loop gain.

The bias current are Ib1 = 100 pA, Ib2 = 2 nA, Ib3 = 1 µA. A paraphase structure has been used to fix the DC points, equivalent to a non-inverting Common Source; transconductance = gm1.gm2/(gm1+gm2) depending of the current.

Rf = Req = ~180 MΩ if Ib1 = 100 pA

Rf = Req = 74 MΩ if Ib1 = 1 nA

2) Shaper description

The shaper has almost the same structure than the preamplifier with a capacitive coupling but also with an additional variable gain and a 5 bits DAC to adjust the DC output and thus the threshold.

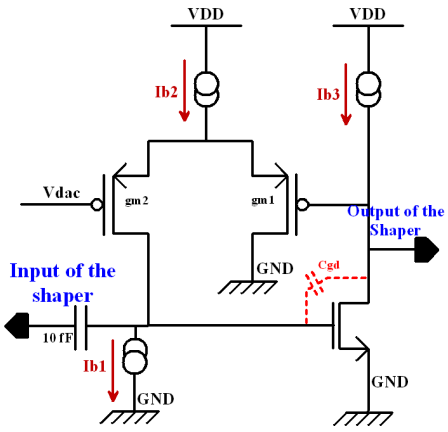

Figure 5: shaper schematic

The bias current are Ib1 = 2.5 nA, Ib2 = 5 nA, Ib3 = 60 nA.

The variable gain consist in four various NMOS in parallel which can be switched leading to make the global Cgd value to vary. So the gain varies from 172 mV/ke- to 487 mV/ke-, or from 1.075 V/fC to 3 V/fC.

The DAC fixes the output DC voltage.

3) The 5 bits DAC

Since the high resistance poly option from Chartered was not taken, the DAC would have been designed with only transistors.

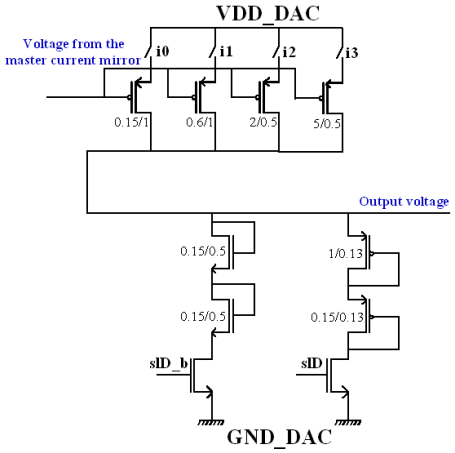

Figure 6: 5 bits DAC schematic

The principle of this DAC is not usual: two sets of diodes have been designed in such a way that the equivalent impedances are different. Four current sources can be selected to make the current to vary. One bit selects the diode we want to use; the four other bits adjust the current which draws through the selected diode. The DAC value can vary from 460 mV to 850 mV which is sufficient for tuning the threshold.

4) Discriminator description

The discriminator consists of three inverters. At first, this block should be into the digital tier to minimize the bulk coupling between the discriminator and the preamplifier input. This design will be made in a next circuit.

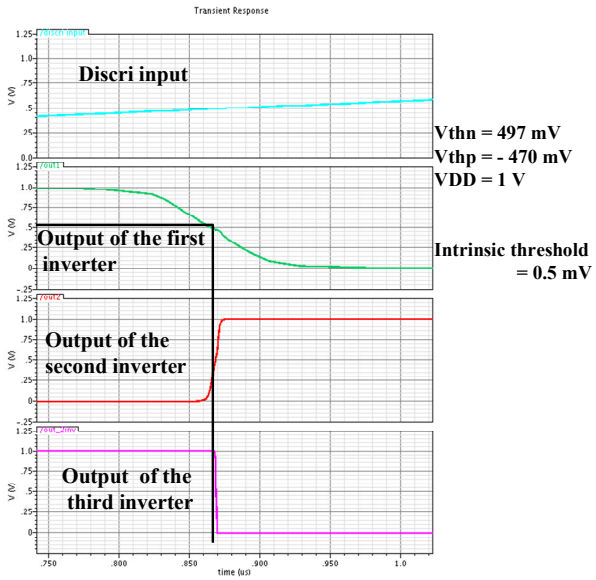

Figure 7: outputs after the three inverters

5) Dedicated test chip

This circuit has been design in such a way that it can be easy to test and measure the signals.

Three probes have been added into each analogue channels after the preamplifier, the shaper and the discriminator to observe signals by oscilloscope.

Several column types have been designed allowing us to study various flavors of transistor types (normal, low Vt, 3p3), noise, oscillations…

- ✓ Column 1 to 10: reference channels
- ✓ Column 11 to 18: various preamplifier transistor types have been integrated
- ✓ Column 19 to 22: without variable gain
- ✓ Column 23: discriminator has been removed
- ✓ Column 24: shaper has been removed

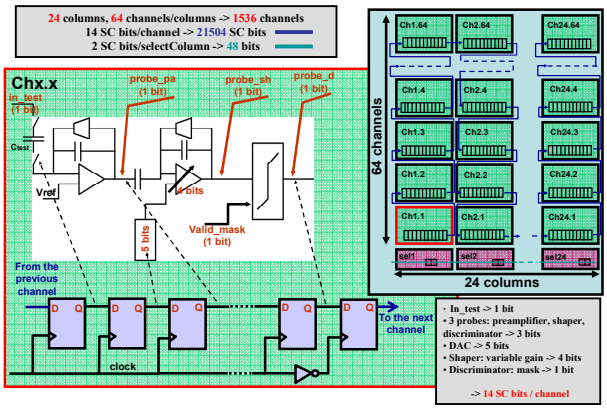

Figure 8: Slow Control in the analogue tier

Three shift register for the slow control have been implemented. One to configure each analogue channels: test capacitance, DAC, variable gain, masked discriminator output, three probes. There are 14 bits for each channel and, with 1536 channels, this shift register has 21504 bits of slow control.

Another shift register has been implemented to configure the Select Column block: one bit to power or shut off the column, another bit to select the column in which the channel with selected probes is. This shift register has 48 bits of slow control.

6) *Simulations*

At this time the only results are simulations.

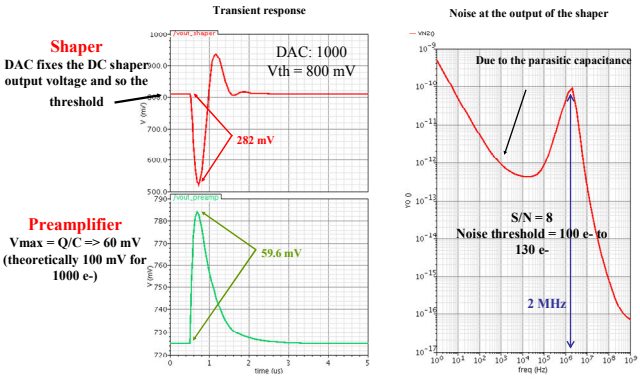

Figure 9: simulation of the analogue channel

We can get a very high gain after the shaper, up to 3 V/fC.

The simulated rms noise gives 16.2 mV, or 46 e-, which gives: S/N = 21.

The figure below shows the linearity of the Time Over Threshold (TOT) for various injected charge.

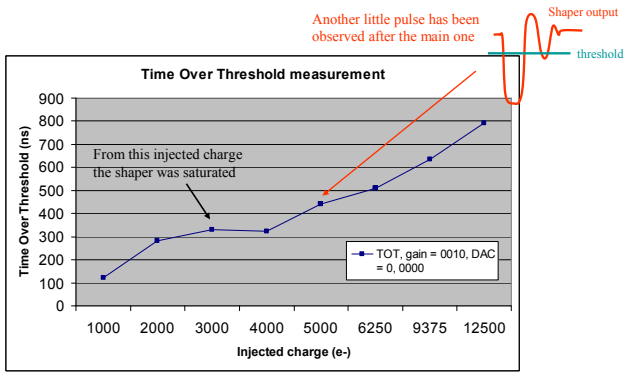

Figure 10: TOT for different injected charge values

The TOT linearity is limited because the shaper output is rapidly saturated and oscillations can be observed which leads to introduce defaults in the effective time over threshold: the shaper has been tuned for a little injection charge threshold, 1000 electrons or 0,16 fC, but the typical injection charge will be significantly different with a sensor of about 200 µm thickness or about 75 µm.

C. *Digital Tier*

For the digital tier, the supply voltage was fixed to 1 V.

Three parts divide this tier: a RS FlipFlop, a shift register of 24 DFlipFlops and a reading structure into each digital channel placed just above the corresponding analogue channel.

The digital tier has just been designed to get out the pulse coming from the discriminator and to create digital noise.

One of the more important targets will be to examine the coupling between the two tiers; and so, creating activity in digital tier will allow us to observe the behaviour of one layer when the neighbouring layer is working.

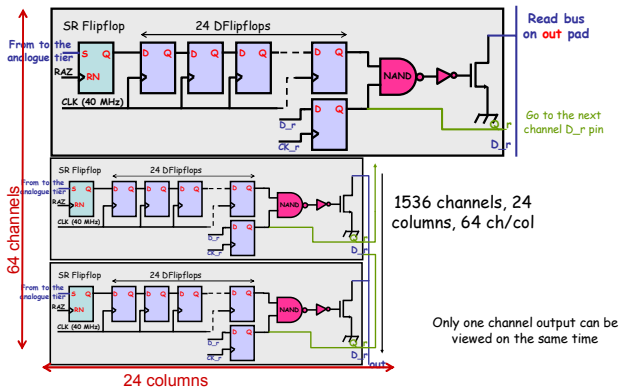

Figure 11: digital channel schematic

A shift register into the digital tier has been implemented to select the channel we want to read. This shift register has 1536 bits of shift register.

D. Power consumption

The power consumption for one channel, in simulation, is about 1.75 µW/ch, below the requirement.

III. TEST BOARD

A test board has been designed with a specific firmware to control the chip I/O. A LabView software manages the board.

It is possible to observe and measure the influence of coupling between the digital tier and the analogue tier.

The three probes allow us to observe the signals after the preamplifier, the shaper and the discriminator by oscilloscope.

To characterize the discriminators S-Curve measurements will be made.

IV. REFERENCES

[1]: Handbook of 3D Integration, Technology and applications of 3D Integrated Circuits, edited by Philip Garrou, Christopher Bower and Peter Ramm.

[2]: website of 3DIC at Fermilab, http://3dic.fnal.gov