Commissioning of the CSC Level 1 Trigger Optical Links at CMS

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Abstract

The Endcap Muon (EMU) Cathode Strip Chamber (CSC) detector at the CMS experiment at CERN has been fully installed and operational since summer of 2008. The system of 180 optical links connects the middle and upper levels of the CSC Level 1 Trigger chain. Design and commissioning of all optical links present several challenges, including reliable clock distribution, link synchronization and alignment, status monitoring and system testing. We gained an extensive experience conducting various tests, participating in local and global cosmic runs and in initial stage of the LHC operation. In this paper we present our hardware, firmware and software solutions and first results of the optical link commissioning.

I. Introduction

The CSC detector [1] comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of the CMS with the goal to provide muon identification, triggering and momentum measurement.

The CSC Level 1 trigger electronics consists of: (1) on-chamber anode and cathode front-end (AFEB and CFEB) and Anode Local Charges Track (ALCT) boards; (2) Trigger Motherboard (TMB) and Muon Port Card (MPC) in sixty 9U crates on the periphery of the return yoke of CMS; and (3) one Track Finder (TF) in the underground counting room (Fig.1). This system provides four trigger candidates to the CMS Muon Trigger within 80 bunch crossing (BX) latency, or 2.5 us.

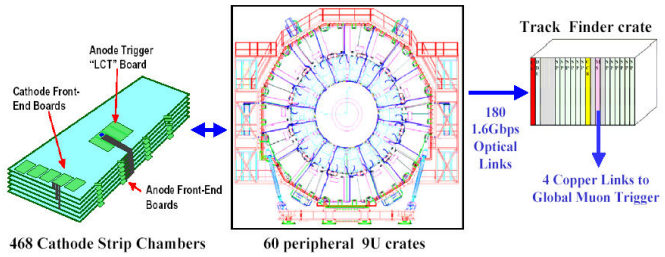

Figure 1: EMU CSC Level 1 Trigger Electronics

The AFEB amplifies and discriminates the anode signals. The CFEB (4 or 5 boards per chamber) amplifies, shapes and digitises the strip charge signals. The anode patterns provide more precise timing information than the cathode signals, and also provide coarse radial position and angle of passing particle for the trigger chain. The FPGA-based processing unit in the ALCT searches for patterns of hits in six planes that would be consistent with muon tracks originating from the interaction point. The patterns are considered valid, if hits from at least four planes are present in the pattern.

Two valid anode patterns, or ALCT's, are sent to the TMB. Based on comparator half-strip hits sent from CFEBs, the TMB searches for two patterns of hits from at least four planes and then matches these two Cathode Local Charged Track (CLCT) patterns with two ALCT ones, making a correlated two-dimensional LCT.

Up to nine TMBs, in pairs with Data Acquisition Motherboards (DMB), one Clock and Control Board (CCB), and one MPC reside in the peripheral 9U crate. 60 such crates are mounted along the outer rim of the endcap iron disks. Every bunch crossing, the MPC receives up to 18 LCTs from 9 TMB boards, sorts them and sends the three best ones via optical links to the Sector Processor (SP) residing in the TF crate in the underground counting room. There are 180 CSC synchronous trigger optical links in total. Each DMB has its own asynchronous optical link for data transmission to the CMS DAQ system using the Data Dependent Units (DDU) and Data Concentrator Cards (DCC). They reside in a four custom 9U crates in the underground counting room.

The TF consists of 12 SP boards, the Muon Sorter (MS), the DDU and the CCB. Each SP receives 15 data streams with trigger primitives from five MPCs and performs track reconstruction for the 60° sector. The three selected tracks are sent to the MS via a custom backplane. The MS sorts the 36 incoming tracks and selects the four best ones and transmits them over copper links to the Global Muon Trigger receiver in the Global Trigger crate. Every SP also provides data to the DAQ system via the TF DDU module.

II. Optical Link Architecture

The basic units of the CSC optical link are the Texas Instruments TLK2501 [2] gigabit serializer/deserializer (SERDES) and the Finisar FTRJ8519 optical transceiver (Fig.2). All links are simplex and operate at a double (~80.16MHz, later in this paper referred as 80MHz) of the LHC clock frequency. The source of trigger data is the MPC board, and the target is the SP. Each muon pattern (called later in this paper as "muon") is sent via a separate link. The MPC transmits the three best muons in ranked order. Each SP receives up to 6 muons from inner station ME1, and three muons from each of stations ME2, ME3 and ME4 (Fig.2). In total, there are 15 optical receivers and 15 TLK2501 deserializers on each SP boards. Due to layout constraints the length of optical fibers varies from 59 m to 112 m, so the propagation times vary up to 270 ns (assuming ~5ns/m delay

in multi-mode fiber). All optical connections are implemented through the front panels of the MPC and SP boards. A front view of the TF crate with 180 optical fibers connected is shown in Fig.3.

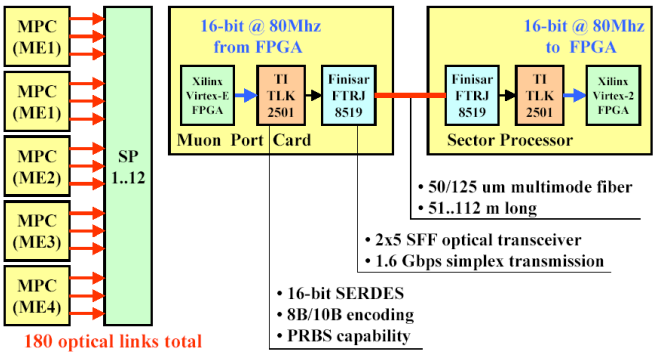

Figure 2: CSC Level 1 Trigger Optical Links

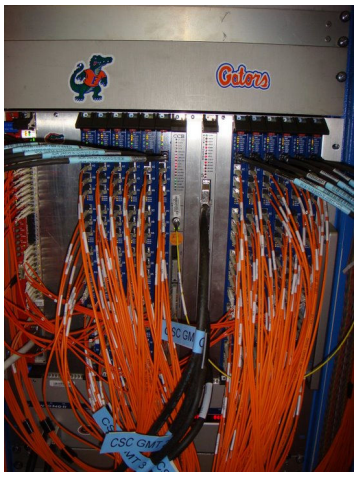

Figure 3: Front View of the CSC Track Finder crate

III. Clock Distribution

The TLK2501 specification requires that the peak-to-peak jitter of the SERDES reference clock (80.16MHz in our case) be no more than 40 ps [2]. Since our trigger links are synchronous, we must use a derivative of the LHC clock frequency. The CCB, which is the source of the clock and control signals, includes the CERN designed TTCrq mezzanine board [3] with the TTCrx and QPLL2 ASICs. The TTCrx transmits the 40MHz clock with relatively high jitter of about few hundred picoseconds, while the QPLL2 provides three LVDS clock outputs of 40MHz, 80MHz and 160MHz with a jitter below 50 ps [4]. It was decided to route the QPLL2 80Mhz LVDS clock output via the custom peripheral backplane to the MPC and use it as a reference for the TLK2501 serializers.

On a SP board the 80MHz reference clock is obtained from the 40MHz frequency arriving from the CCB. Such a solution allows us to use the peripheral CCB board in the TF crate without any modifications. The default CCB source is the 40MHz clock from the QPLL2; and all the twelve 40MHz clocks to SP boards in the TF crate are delivered over separate LVDS backplane lines of the same length.

On the first prototype of the SP board, in 2002, the 80MHz reference clock was synthesized in the FPGA using the Digitally Controlled Module (DCM). The output jitter was excessive and the link did not lock properly. It was decided to build a small daughter board (Fig.4) that comprises the same QPLL2 ASIC that the TTCrq mezzanine is using. This board is installed on top of the SP main board and provides a low jitter 80MHz LVDS clock. This clock is distributed via clock repeaters from the daughter board to all 15 deserializers.

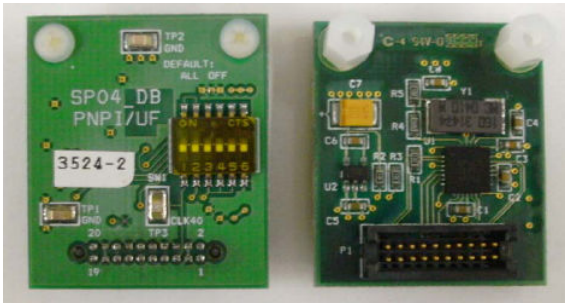

Figure 4: SP Clock Daughter Board (top and bottom view)

The QPLL2 on both the CCB and SP mezzanines are set to default operation "mode 1" [4], when the QPLL2 calibration logic is active, and frequency calibration cycle is executed after a reset or each time the lock is lost. This mode requires minimal monitoring and automatically executes a frequency calibration cycle every time the loss-of-lock state is detected. Locking time, including a frequency calibration cycle is ~180 ms. The "lock" state can be monitored with the LEDs on the front panel of the SP and CCB boards as well as from status registers available via VME.

The locking range of the 22 production SP clock daughter boards as well as a couple of the TTCrq mezzanines was studied during production tests of the TF. It was shown that all the tested boards can withstand a variation of at least –84, +42 ppm of the LHC frequency and thus meet the CMS trigger requirements (Fig.5).

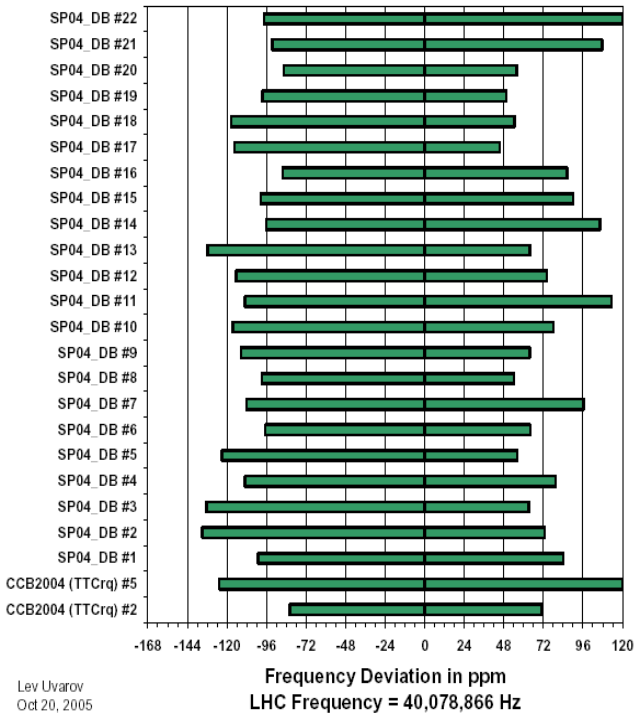

Figure 5: QPLL Locking Range

IV. Link Synchronization and Alignment

The 16-bit parallel data in the TLK2501 transmitter is encoded into 20 bits using an 8B/10B encoding format. There are also two other control signals called TX_EN and TX_ER that specify the "normal data character", "idle", "carrier extend" and "error propagation". The latter three are the special codes defined in the 8B/10B format. One of them, the "idle" is used as a synchronization pattern to recover the byte boundary. The decoder in the deserializer detects the "idle" symbol called the K28.5 comma which generates a synchronization signal aligning the data to their 10-bit boundaries for decoding. Then the decoder converts the data back to 8-bit, removing the control symbols. The receiver has two status outputs RX_DV and RX_ER to indicate one of four link states listed above.

The only way to synchronize (or re-synchronize) the TLK2501 chipset is to put a transmitter into "idle" state for at least 3 clock cycles. This is done upon the arrival of the L1Reset (Resynch) command distributed from the Timing, Trigger and Control (TTC) system of the CMS at the beginning of each run. Then, after transmission latency, link propagation delay, and data reception latency, every TLK2501 receiver switches into "idle" mode. Three data streams from each MPC are supplied to the front FPGA of SP (there are five front FPGA in total), where the input alignment FIFO buffers (one per muon) have been reset by the same L1Reset command and are waiting for valid data from the receiver. Each alignment FIFO resumes writes after the corresponding TLK2501 receiver has switched to normal data transmission. When all receivers have started getting valid data (and all their RX_DV outputs became "1"), the AND of all RX_DV outputs is synchronized with the SP bunch crossing (BX) clock CLK40 and enables the FIFO reads (Fig.6), thus the SP is aligned to the latest (longest) link. In the present MPC firmware the length of the "idle" pattern is set to 128BX, or 3.2us.

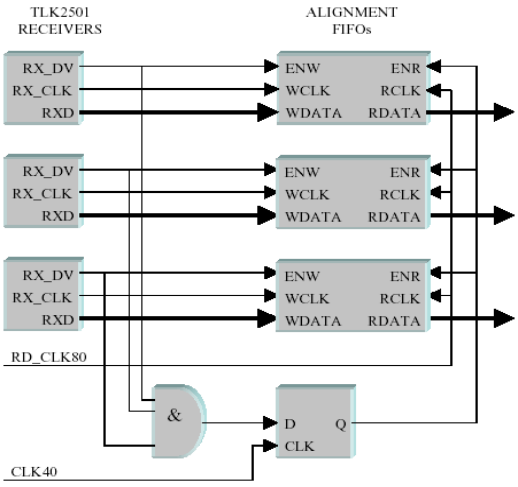

Figure 6: Simplified Alignment Scheme

For the whole TF crate with 12 Sector Processors the synchronization and alignment of all 180 links require to set and adjust the Alignment FIFO delays individually for each SP. They allow to equalize the different MPC-to-SP fiber lengths with 0.5BX accuracy (Table 1). This procedure is described in detail in the Note [5].

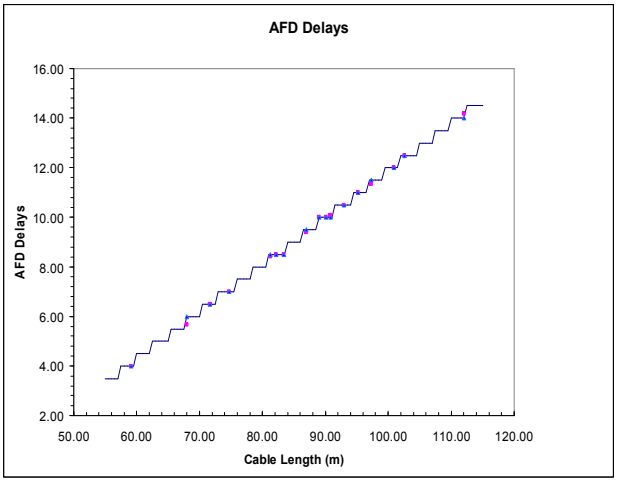

Table 1: Alignment FIFO Delays vs Optical Fiber Lengths

Since the TTC fiber lengths to peripheral CCBs also vary, the system-level synchronization procedure includes appropriate coarse and fine delays settings in the peripheral TTCrx ASIC on CCB boards and programmable delays in the TMB registers. An efficient test of the global CSC synchronization is possible using the Bunch Crossing Zero (BC0) signal coming from the TTC system. All the CSC trigger boards (TMB, MPC, SP, MS) are transparent to this signal. So we can check isochronous clocking by comparing BC0 arrival times at SP level from various peripheral crates and from individual TMB boards in each crate. This test was conducted in May 2009. Each MPC was set into "transparent" mode, when it can transmit any given LCT1…LCT18 to any specific optical link 1..3 without sorting. 936 individual measurements were made (468 chambers x 2 LCT per chamber) and the synchronization was verified.

V. Link Testing, Monitoring and Performance

The simplest data transmission test can be run from the transmitter TLK2501 to the receiver TLK2501 using the embedded 2^7-1 Pseudo-Random Bit Stream (PRBS) generators. Within ~15 minutes the bit error rate below 10^{-12} per link can be verified. This test does not involve the transmitter and receiver FPGA. A more elaborate test allows to transmit test patterns from the output buffer in the MPC (or even in the TMB) and verify them from the spy SP FIFO.

There are several clock and link status monitorables available from the SP registers via VME. They include the following: SP daughter board and TTCrq "lock" statuses and "Loss of Lock" counters; "signal detect" status of each optical receiver; alignment FIFO "empty flag" and word count; "signal loss", "carrier extend", "error word", "alignment FIFO underflow", "BC0 arrived later/early", "BX mismatch" and "PRBS error" counters; "valid pattern" and "valid track" counters for occupancy monitoring.

Immediately after the "idle" pattern every MPC sends to SP an 8-bit word with its unique board (1..60) and link (1..3) numbers. These numbers are stored in the SP status register and are used as a basic tool to verify the integrity of links.

Monitoring procedures include periodic (at present, every 10 seconds) data read out over VME from all the TF boards.

Most relevant quantities (any link errors, "unlocked" and "FIFO full" statuses, real-time trigger rates) are available to shifters and used for alarms. Monitoring data is periodically logged to the local file and Condition Database. An example of the link status display showing three links SP2/F1/M1/M2/M3 in error state is shown in Fig.7.

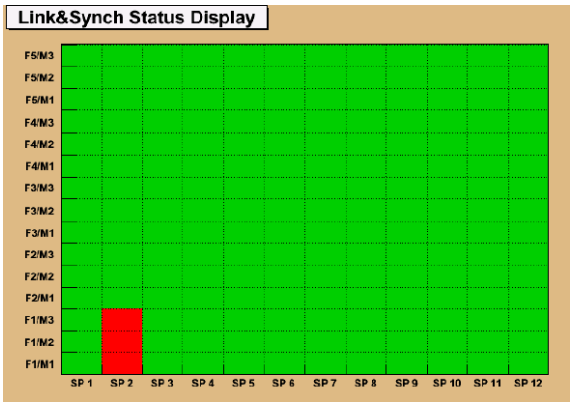

Figure 7: Link Status Monitoring Display

A long term study of link behavior using these monitorables allowed us to detect at an early stage of commissioning that some random fraction of optical links accumulated synchronization errors in certain runs. Detailed bench tests confirmed the problem and it was traced back to minor error in the SP's front FPGA firmware, where the receiver control signals crossing two clock domains in the FPGA were not handled properly, resulting in occasional synchronization failures. The error was fixed, and all the 12 SP boards reprogrammed, and since October 2008 we haven't seen any synchronization errors. Red alarms in the display above may well indicate the other hardware problems, for example, not properly initialized or non-powered peripheral crate, when all three links from a given MPC are not running properly.

The correlated two-dimensional LCTs are transmitted to both the trigger (TF-DDU) through the MPC and to DAQ chains (Fig.8). So the quality of data transmission via optical links can be evaluated by comparison of the trigger and DAQ data streams.

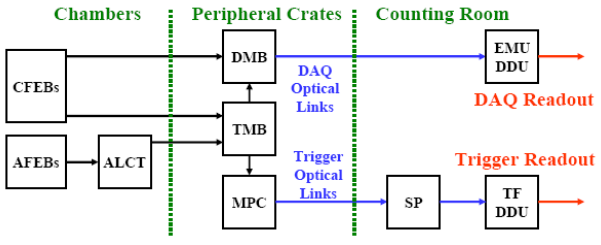

Figure 8: CSC DAQ and Trigger Readout

We have done two types of data analysis. The first one is data to data comparison of the LCTs between the trigger and main DAQ streams per event for all transmitted bits. The study consists of comparing the number of LCTs found in DMB and TF DDU for each chamber and on event by event basis. 6% of the total LCTs/event presents the largest class of mismatches, when there are no LCTs in the DMB, but at least one LCT in the TF DDU which should never happen. Most of this discrepancy was traced to disabled chambers in the main readout while being kept in the trigger. 0.4% of the total LCTs/event corresponds to the case when we have more LCTs in the main readout with respect to the trigger. This is explained by the fact that the MPC selects only three best-quality LCTs out of 18 as expected.

The second type of analysis is based on data to emulator comparison for the MPC. The CSC Trigger Primitives emulator simulates the functionalities of the ALCT, CLCT, TMB and MPC processors. Collections of the CSC wire and comparator digis are the inputs to the simulator, and ALCT, CLCT and correlated LCTs before and after the MPC sorting are its outputs. The results of this study are consistent with the previous one.

VI. Conclusion and Future Plans

The system of 180 CSC Level 1 trigger optical links has been in operation for more than a year. The firmware on a receiver part was updated several times to fix minor bugs and improve abilities to monitor link performance. Optical links are running reliably since autumn of 2008. CSC TF cell of Trigger Supervisor software allows to access all libraries to control, perform configuration, monitoring and hardware tests of the TF, including optical links. Several monitoring panels are available for shifters in the control room.

It was essential for successful commissioning at the CMS to have a testing stand in the CMS test area in building 904 at CERN. This stand includes one operational CSC chamber and a full chain of trigger boards, including the TF. This test stand is being used for various hardware, firmware and software checks, debugging and measurements. It is important to maintain such a stand for the lifetime of the experiment, along with simpler stands at the universities involved in hardware and firmware development.

The proposed Super-LHC upgrade with increased luminosity of 10^{35} $cm^{-2}s^{-1}$ implies higher data volumes to be transmitted through the Trigger and DAQ systems. Preliminary estimates show that the volume of data through the EMU trigger optical links will increase 3..6 times, so the present MPC becomes a bottleneck. It is envisaged that the CSC Muon Port Card, Sector Processor and optical links will have to be upgraded to accommodate higher throughput, more complex sorting and track reconstruction algorithms.

VII. References

[1] The CMS Experiment at CERN LHC. The CMS Collaboration. Published in Journal of Instrumentation 2008 JUNST 3 S08004.
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