e-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication

S. Bonacini[a], K. Kloukinas[a], P. Moreira[a]

[a]CERN, 1211 Geneva 23, Switzerland

sandro.bonacini@cern.ch

Abstract

The e-link, an electrical interface suitable for transmission of data over PCBs or electrical cables, within a distance of a few meters, at data rates up to 320 Mbit/s, is presented. The e-link is targeted for the connection between the GigaBit Transceiver (GBTX) chip and the Front-End (FE) integrated circuits. A commercial component complying with the Scalable Low-Voltage Signaling (SLVS) electrical standard was tested and demonstrated a performance level compatible with our application. Test results are presented. A SLVS transmitter/receiver IP block was designed in 130 nm CMOS technology. A test chip was submitted for fabrication.

I. Introduction

With the future upgrade of the LHC and its associated experiments the number of tracker detector channels will increase by one order of magnitude with respect to the LHC trackers just completed. Nonetheless, the design strives to reduce the total material inside the detectors, which is mainly due to cables, cooling and mechanical support, the last one being related to the other two. It is thus necessary to minimize the power consumption of the electronic devices in the front-end (FE) and the number of cables required. This can be achieved by new low-power interconnection schemes between the FE and the off-detector electronics, and among the on detector Application-Specific Integrated Circuits (ASICs); numerous slow data links could be aggregated into fewer faster and more efficient links.

The use of an advanced CMOS technology, which allows several supply voltage levels for different purpouses, helps the minimization of power of the FE's ASICs.

The recent technology advancements demonstrated serial links as fast as 10 Gbps and above implemented in 130 nm CMOS technology. The GBT project was started to design the future optical data link for the experiments, which brings together the functions of data readout, trigger and control. The GBT will be connected to a number of up to 32 FE ASICs, requiring each one a dedicated electrical link, in a star-point topology. These links target short distance transmission (typically up to 2 meters on PCB, and up to 4 meters on cable) and shall be as much as possible insensitive to common-mode voltage variations.

The front-end electronics of particle physics detectors aim to achieve high levels of performance in terms of resolution and accuracy. This performance is limited by the system intrinsic noise, therefore electrical links should be designed to minimize crosstalk and power supply noise.

For these reasons, the study of a low-power low-voltage-swing electrical link was carried out. Among the several link examined, the Scalable Low-Voltage Signaling (SLVS) industry standard was chosen and tested. The protocol is briefly described in section II. The tests are described in section III.

Since the link circuitry shall be placed in the FE, it needs to work properly in the harsh environment of the experiments characterized by high level of radiation (up to hundreds of Mrd) and intense magnetic field (up to 4T). These constraints make commercial components not suitable and require the design of novel radiation-hard trasmitter and receiver circuits.

The design of an SLVS transmitter and an SLVS receiver was carried out, as part of the GBT project, for the interconnection between the GBTX chip and the FE ASICs. The design is presented in section IV.

II. The SLVS standard

The SLVS standard is defined in [1] and describes a differential current-steering electrical protocol with a voltage swing of 200 mV on a 100 Ω load and a common mode of 200 mV. The differential voltage is therefore 400 mV as depicted in Fig. 1.

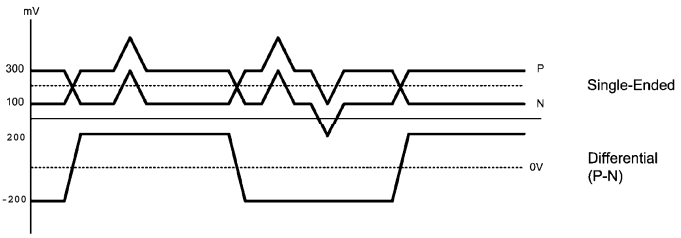

Figure 1: SLVS standard signaling scheme.

The output current is 2 mA, with a power consumption at the load of 0.4 mW. The reduction in common-mode with respect to other standards, like LVDS, allows the use of a supply voltage as low as 0.8 V for the output driver circuitry.

A few commercial parts which comply to this standard are available, mainly from National Semiconductors, and their target application is in mobile/portable devices as short (< 30 cm) communication links over PCB traces and flat cable.

III. Bit error rate testing

The test aimed to demonstrate the capability of the electrical protocol to work with longer distances and different media than

the parts normal application.

A. Test setup

A commercial part which uses the SLVS standard was tested with several media types and lengths (5 m Ethernet cable, 24 cm kapton, 2 m PCB and others) at two different speeds (320 Mbps and 480 Mbps). The part we used is the LM4308 from National Semiconductors.

The test setup is composed of

- two Xilinx Spartan-3E evaluation boards,
- two custom PCBs holding each two LM4308 components,
- two link media,

arranged like in Fig. 2.

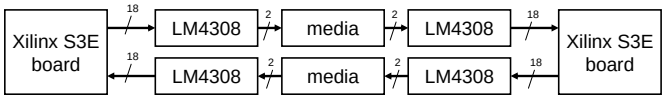

Figure 2: Test setup (clock signals are not shown).

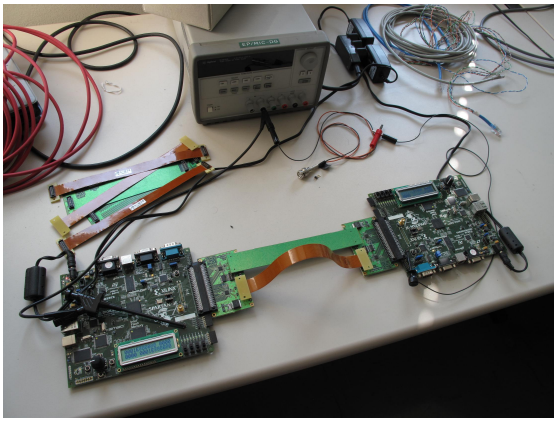

Figure 3: Test setup picture.

The LM4308 chip is an SLVS serdes, which can be hardwire-configured to be either a serializer or a deserializer. In the test, two LM4308 chips are serializers while the other two are deserializers.

Each one of the Xilinx Spartan-3E chips generates a pseudo-random sequence, which is fed to a serializer chip, and checks the sequence coming from a deserializer chip. The link media are connected to the serdes boards through Samtec QTE/QSE connectors.

A few special PCB-type media were fabricated for this purpouse: a 1-m microstrip, a 2-m microstrip and a 2-m stripline; these lines follow a serpentine path to minimize area. An Ethernet plug adapter was also fabricated in order to test Ethernet cables.

B. Test results

The test results are described in Table 1. The eye-diagram in Fig 4 has been obtained at 480 Mbps at the load of a 2-m microstrip PCB line.

It should be noted that the LM4308 uses a forwarded-clock technique, therefore the bit errors which were measured might as well come from the clock line, which in all media runs along the data line.

Table 1: SLVS test results

Media	320 Mbps	480 Mbps
1-m microstrip	$< 1 \cdot 10^{-13}$	$< 1 \cdot 10^{-13}$
2-m microstrip	$< 1 \cdot 10^{-13}$	$< 1 \cdot 10^{-13}$
2-m stripline	$< 1 \cdot 10^{-13}$	$< 1 \cdot 10^{-13}$
24-cm Kapton	$< 3 \cdot 10^{-14}$	$< 1 \cdot 10^{-13}$
5-m ethernet cable	$< 1 \cdot 10^{-13}$	$2 \cdot 10^{-11}$

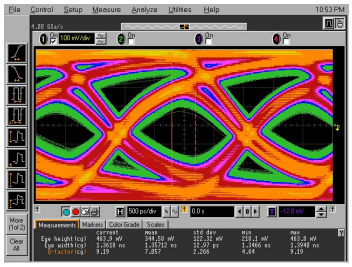

Figure 4: Eye diagram at load, at 480 Mbps using a 2-m microstrip board medium.

The test results of the SLVS standard were encouraging and demonstrated performance compatible with our target applications

IV. SLVS TRANSMITTER AND RECEIVER IP BLOCKS DESIGN

A transmitter and receiver IP blocks for integration in the FE ASICs, complying with the SLVS protocol, were designed in a 130 nm technology. The e-link can operate at any speed up to 320 Mbps. The transmitter and receiver blocks are designed to be rad-hard and SEU-hard.

Though these IP blocks are targeted for the implementation of the GBTX-FE connection, they are also suitable for general chip-to-chip communication within the LHC experiments.

The transmitter and receiver circuits are designed to be powered in the range from 1.0 to 1.5 V.

Studies on the radiation tolerance of the technology used [3] suggest that thin-oxide transistors suffer limited total dose effects. Only thin-oxide transistors are used in the design, avoiding any special layout technique. SEU-robustness is assured by triplicating all low-capacitance nodes and logic elements.

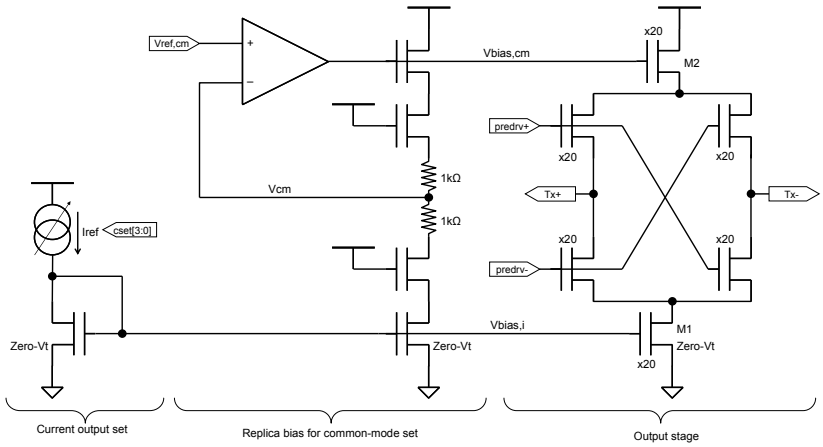

Figure 5: Transmitter output stage schematic.

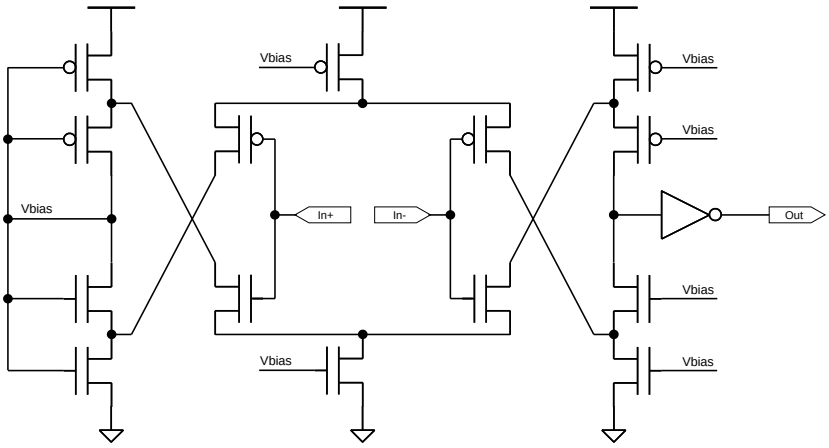

Figure 6: Receiver first stage schematic.

A. Transmitter

The transmitter, whose schematic is shown in Fig. 5, is implemented by a N-over-N driver which steers the current given by the current source M1. The common-mode is kept at $V_{ref,cm}$ = 200 mV by the replica bias of the source-follower M2.

In order to minimize the power consumption, the current output is adjustable from 2 mA down to 0.5 mA, with a 60% power reduction and thus proportional lowering of crosstalk. The transmitter can also be set into a power-down state when unused. The current output is set by a 4-bit digital switch (not in the figure).

In power-down mode, all the biasing circuits are switched off and the pre-driver stops toggling the final stage. The transmitter consumes 3 mW at 320 Mbps, with 1.2 V supply voltage and 2 mA output.

B. Receiver

The receiver is implemented by a rail-to-rail differential amplifier, shown in Fig. 6, such that it guarantees a wide common-mode voltage range. The receiver can be as well set into a power-down state when unused.

The first stage amplifier, similar to [2], is a combination of two basic complementary amplifiers, which together can cover fully the input range from negative to positive supply. Moreover, the amplifier is self-biased through a negative feedback mechanism.

In power-down mode the biasing is switched off, which prevents toggling on the output. The receiver consumes 210 μW at 320 Mbps, 1.2 V supply and with a 64 fF output load.

C. *Test chip*

A test chip containing the SLVS receiver and the SLVS transmitter was designed and submitted for fabrication. The test chip works as an LVDS-to-SLVS translator and viceversa. A few CMOS input pins are present to control the transmitter current output setting and the receiver shutdown. A loopback control pin is also provided for testing.

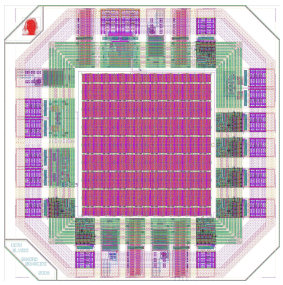

Figure 7: Test chip layout.

Testing will be performed on the chip to evaluate the bit error rate in the same fashion as the commercial part.

V. CONCLUSIONS

The SLVS electrical standard for the e-link, targeted for the connection between the GBTX chip and the FE ASICs, was tested with a commercial part and demonstrated a performance level compatible with our application. An SLVS transmitter/receiver IP block was designed in 130 nm CMOS technology and the test chip was submitted for fabrication.

Future improvements might include the implementation of programmable pre-emphasis in the transmitter and investigate LVDS compatibility of the electrical levels.

REFERENCES

[1] JEDEC, JESD8-13, *Scalable Low-Voltage Signaling for 400 mV* (SLVS-400).

[2] M. Bazes, *Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers*, IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, Feb. 1991.

[3] F. Faccio & G. Cervelli. *Radiation-induced edge effects in deep submicron CMOS. transistors*. IEEE Transactions on Nuclear Science, vol. 52, no. 6, pages 2413–2420, December 2005.