Readout and Data Processing Electronics for the Belle-II Silicon Vertex Detector

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Abstract

A prototype readout system has been developed for the future Belle-II Silicon Vertex Detector at the Super-KEK-B factory in Tsukuba, Japan. It will receive raw data from double-sided sensors with a total of approximately 240,000 strips read out by APV25 chips at a trigger rate of up to 30kHz and perform strip reordering, pedestal subtraction, a two-pass common mode correction and zero suppression in FPGA firmware.

Moreover, the APV25 will be operated in multi-peak mode, where (typically) six samples along the shaped waveform are used for precise hit-time reconstruction which will also be implemented in FPGAs using look-up tables.

I. Introduction

The Belle Experiment [1] at the KEK Research Laboratory in Tsukuba (Japan) has successfully been observing CP violation and other phenomena in the B system for a decade. It will conclude its data taking by the end of 2009 at an integrated luminosity of about $1\,\mathrm{ab}^{-1}$. The Belle Experiment as well as its counterpart BaBar [2] in Stanford (USA) were explicitly acknowledged in the 2008 physics Nobel Price statement for the experimental verification of the CP violation theory [3] by Makoto Kobayashi and Toshihide Maskawa.

Already now, the KEK-B machine [4], which stores electron and positron beams that are collided in the center of the Belle Experiment, provides the highest luminosity in the world, peaking at more than $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In order to study rare phenomena and increase the statistics of measurements, it is foreseen to upgrade the KEK-B machine until 2013 such that the ultimate luminosity will be 40 times higher than now. This also implies changes in the Belle Experiment, which was not designed for such an intensity and consequently all parts of the detector need an upgrade as well.

The present Silicon Vertex Detector [5] (SVD2) of the Belle Experiment is composed of four layers of double-sided silicon sensors and read out by the VA1TA front-end chip [6], which has a shaping time of about $800\,\mathrm{ns}$. Its innermost layer, located at a radius of $2\,\mathrm{cm}$ from the beam axis, suffers from an occupancy of about 10% at the present luminosity. Moreover, the readout speed of $5\,\mathrm{MHz}$ sets another limit, because the VA1TA has no pipeline memory and thus a dead time occurs after a trigger until the data are read out. This is at the percent level with the present trigger rate of about $450\,\mathrm{Hz}$, but will be prohibitive at 40 times higher luminosity with a projected trigger rate of up to $30\,\mathrm{kHz}$. Consequently, the present SVD2 is not suitable for Belle-II and a completely new silicon detector, together with a new readout chain, is being developed, which is described below.

II. Silicon Vertex Detector for Belle-II

The Silicon Vertex Detector for the future upgrade of the Belle Experiment, shown in fig. 1, will again consist of four layers of double-sided sensors which are arranged cylindrically around the interaction point. In contrast to the present SVD, however, a two-layer pixel detector, consisting of DEPFET sensors [7], will be placed in the innermost part at radii of 1.3 and $2.2\,\mathrm{cm}$. In this sense, the future vertex detector will consist of a total of six layers, which enables robust and redundant tracking as well as precise vertex reconstruction thanks to the pixel detector.

Another striking difference to the current SVD2 is, that the future detector, tentatively named SuperSVD, will cover the same angular acceptance, but with tilted (trapezoidal) sensors in the forward region. This will significantly complicate the mechanical assembly, but at the same time improve the signal-to-noise ratio in that area and also save a considerable amount of readout channels and thus cost. Simulation studies are ongoing whether or not to introduce such a lantern-shape also in the backward side, which would then lead to a silicon detector very similar to the one of the Babar experiment [8].

The SuperSVD will entirely be composed of double-sided silicon sensors made from 6" wafers, which are read out by four or six APV25 front-end chips on either side, depending on the position, strip pitch and overall size. In the SVD2, the strips of up to three sensors were concatenated and read out by readout chips located at the sides outside of the acceptance region. Such a concept is not possible anymore with the short shaping time of the APV25, which is necessary to reduce the occupancy, because this also implies an increased noise susceptibility related to load capacitance [9].

While those sensors that are located at the forward or backward edges can still be read out in the conventional way by placing a hybrid at the side (and thus outside of the acceptance), this is not possible for the inner sensors, for which we developed the Origami chip-on-sensor concept. As this idea is described in detail in this volume [10], we will just summarize the main features here. Thinned readout chips are placed on flex hybrids which sit on one side of the sensor and thus have very short connections to the strips on that sensor side. The opposite side of the sensor is contacted through flexible fanout pieces which are bent around the edge – hence the name Origami. Fig. 2 shows the first working prototype of such an Origami module assembly, which is described in detail in [10].

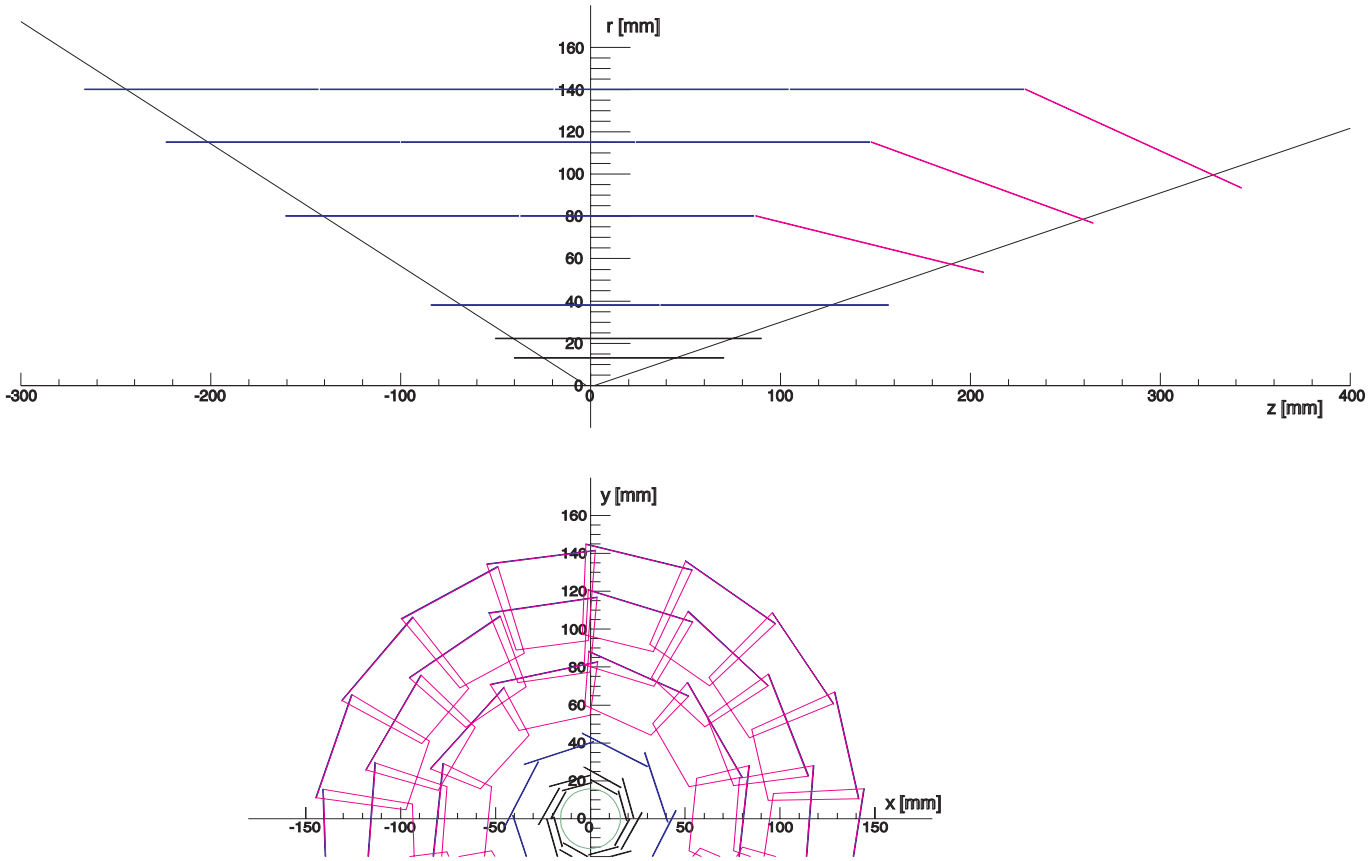

Figure 1: Conceptual design of the Silicon Vertex Detector for Super-Belle, consisting of two pixel layers surrounded by four double-sided silicon strip layers with slanted sensors in the forward region.

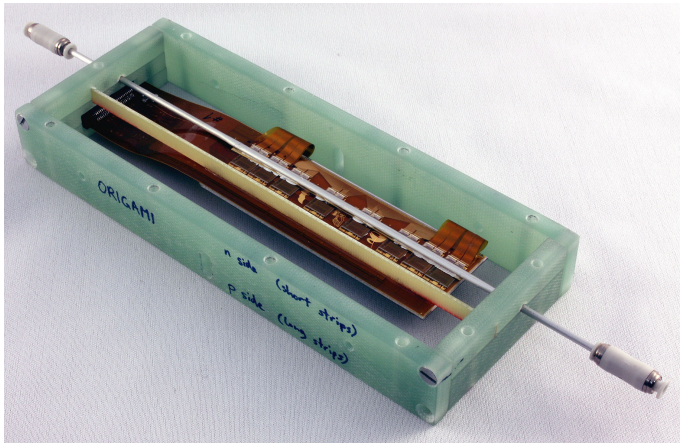

Figure 2: Origami chip-on-sensor prototype module on a 4" double-sided silicon detector read out by four thinned APV25 chips on either side, which are all cooled by a single cooling pipe. The fanout pieces wrapped around the edge to connect to the opposite sensor side are clearly visible. See [10] for details.

The Origami concept inevitably increases the material budget compared to conventional readout schemes, but it is the only way of maintaining a good signal-to-noise with fast shaping. Moreover, it also implies that the number of readout channels will roughly doubled compared to the SVD2, namely 243,456 strips being read out by 1,902 APV25 chips (cf. 110,592 strips and 864 VA1TA chips for the present system).

III. AVP25 Front-End Readout Chip

The APV25 [11] readout chip was originally developed for the CMS experiment at CERN, but it also fits the needs of the SuperSVD at Belle-II. Thanks to its short shaping time of 50 ns (compared to about 800 ns of the present VA1TA), it automatically reduces the occupancy by a factor of 16. (A factor of 12.5 was found by measurement because the actual waveforms are not exactly congruent and thresholds need to be considered.) The APV25 chip also features an internal analog pipeline of 192 cells and thus allows dead time-free measurement. (Actually, there is a very short dead time of 3 clock cycles by design, but this is irrelevant for Belle-II.)

In CMS, the APV25 is operated at a 40 MHz clock which is synchronous to the bunch crossings in the experiment. This also allows to use the so called "deconvolution" mode [12], where a weighted sum of three consecutive samples in the pipeline is calculated for each channel upon reception of a trigger. This on-chip processing narrows down the resulting signal such that the data can unambiguously be assigned to a particular bunch crossing at the cost of a moderate increase of noise.

Unfortunately, this feature cannot be used in Belle-II, because the bunch crossings occur in a quasi-continuous fashion (the accelerator frequency is about 508 MHz) and thus the APV25 clock cannot be synchronized to the collisions. However, the APV25 chips also offers a mode where the three samples from the pipeline can be obtained in raw format without passing the deconvolution algorithm. In this mode, integer mul-

tiples of three samples can be obtained by sending two or more triggers with the correct spacing. This opens the path for off-chip data processing which is pursued for the SuperSVD, as described in section V.

The APV25 has a differential analog output where multiplexed strip data are presented at clock frequency. Moreover, the APV25 has a slow control interface which uses the I^2C standard. Various internal bias voltages and currents as well as general settings (such as the mode of operation) can be controlled through this interface.

IV. Readout Chain

Fig. 3 shows the conceptual layout of the readout system, which follows a pretty conventional scheme that largely resembles the present situation. Repeater boxes (called "DOCK") are located a few meters away from the front-end hybrids and are used for buffering clock, trigger and control signals sent to the front-end as well as the analog data obtained from there. Moreover, the repeater has another important task. As we read out double-sided sensors, the front-end chips of each side are operated by floating LV power which is tied to the bias voltage level of each side, respectively. In the present SVD2, the sensors are biased at 80 V which means that the front-end readout chips are at ± 40 V. Consequently, the repeater box also has to translate the analog front-end signals to earth-bound levels and control signals in the opposite direction. Presently, this is done using optocouplers, but as the readout speed will be much faster in the future, a capacitive coupling scheme has been established for analog signals, clock and trigger, while optocouplers are only used for slow controls such as I^2C and reset lines.

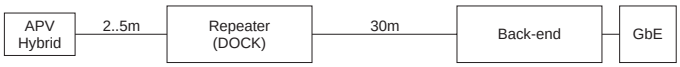

Figure 3: Schematic view of the readout chain for the SuperSVD.

A prototype readout system was built and successfully operated in the lab as well as in several beam tests. It consists of a mechanical repeater box ("DOCK", fig. 4) that contains a mother board ("MAMBO") which hosts up to six repeater boards ("REBO"). The latter are all identical, but are assigned to positive or negative bias voltages and hence readout of n- or p-sides of the detector, respectively, depending on the slot in the mother board. The actual level translation is performed on the REBO boards, each of which presently serves 16 APV25 front-end chips on four hybrids (fig. 5).

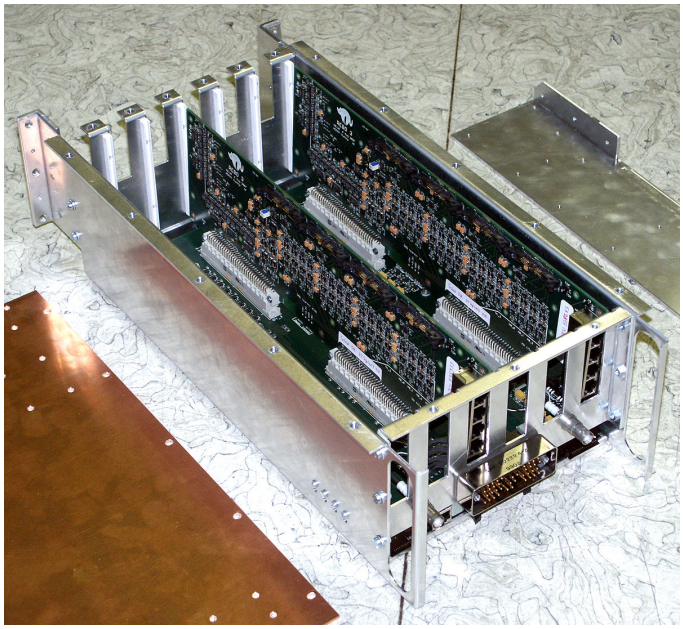

Figure 4: Prototype repeater system. An aluminum box ("DOCK") contains a mother board ("MAMBO") and up to six repeater boards ("REBO"). Each repeater board is mounted onto an aluminum bracket (shown detached to the right) which is then screwed to the water-cooled copper lid (shown to the left).

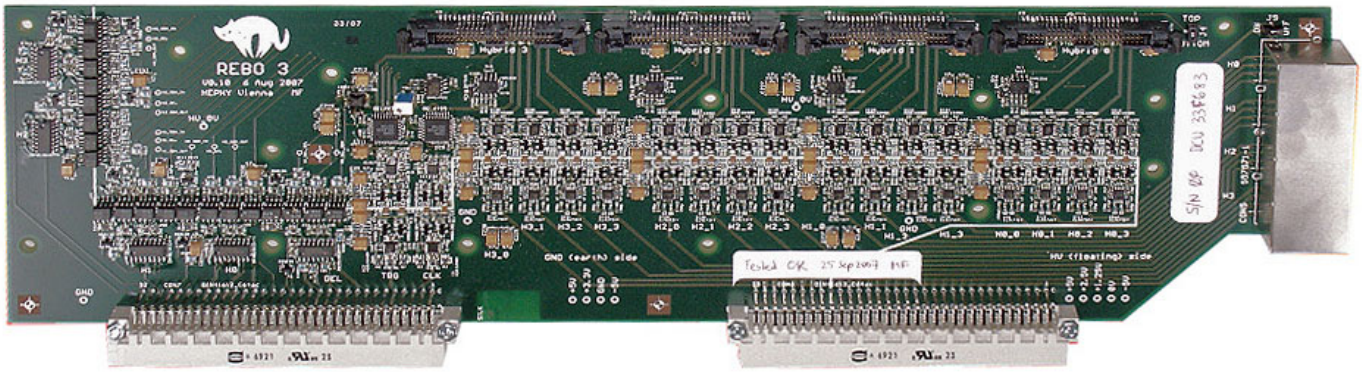

Figure 5: Prototype repeater board. The separation between earth-bound and floating voltage levels is indicated by a white line. Optocouplers (left part) translate I^2C and reset lines and capacitors with amplifiers on both sides bridge clock, trigger (center) and analog signals (right half).

The analog signals, once translated to earth-bound voltage levels, are transmitted to the back-end VME system through ethernet cables of 30 m length. Optical links are an alternative, but also driving up the cost and normally need digitization before, which would not only increase the density in the repeater boxes, but also their power consumption and thus the requirements of cooling. Moreover, radiation in the location of the repeater boxes is not an issue in the present system, but

may become critical in the future. The radiation dose was measured around the forward repeater boxes to be approximately $5\,\mathrm{kRad\,ab^{-1}}$. Although many parameters will change in the future machine, a simple scaling of this number implies a lifetime dose of about $250\,\mathrm{kRad}$, which is deadly for most commercial electronic devices. An alternative approach would be to place the repeater boxes farther away from the radiative area, which is under investigation now.

Clock and trigger signals are also propagated through ethernet cables from the controller unit to the repeater boxes, and round twisted flat cables are used for slow controls and switch controls which establish the connection of individual hybrids to $\mathrm{I^2C}$ and reset buses.

The prototype readout system was originally designed for an intermediate upgrade where only the two innermost layers of SVD2 should have been replaced by APV25 readout, but with the SuperSVD system the number of readout channels will double, and thus the density of the repeaters must also increase significantly. Some improvements are planned on the REBO boards to increase the number of channels on a single board while keeping the same size. Moreover, we believe that the number of REBOs within a single box can be increased to (almost) twice the present number.

Figure 7: Control modules of the prototype system. The master control unit (NECO, left) ist complemented by distribution units (SVD3_Buffer, right).

V. FADC+PROC Back-End Data Processing

Both data processing boards ("FADC+PROC") as well as the control units for distribution of clock, trigger and slow control signals to the front-end are based on 9U VME modules located in the electronics hut. The prototype system consists of one master controller ("NECO", left side of fig. 7), one control distribution unit ("SVD3_Buffer", right side of fig. 7) and two FADC+PROC modules (fig. 8), each of which receives the signals of 16 APV25 chips. This system is modular in the sense that in its present form it can spread over two crates with up to 32 FADC+PROC units serving 512 APV25 channels. Clearly this is not sufficient for SuperSVD, and the density is likely to increase also in the back-end. The number of channels per unit and grouping of repeater and back-end units will be reconsidered once the sensor configuration is frozen.

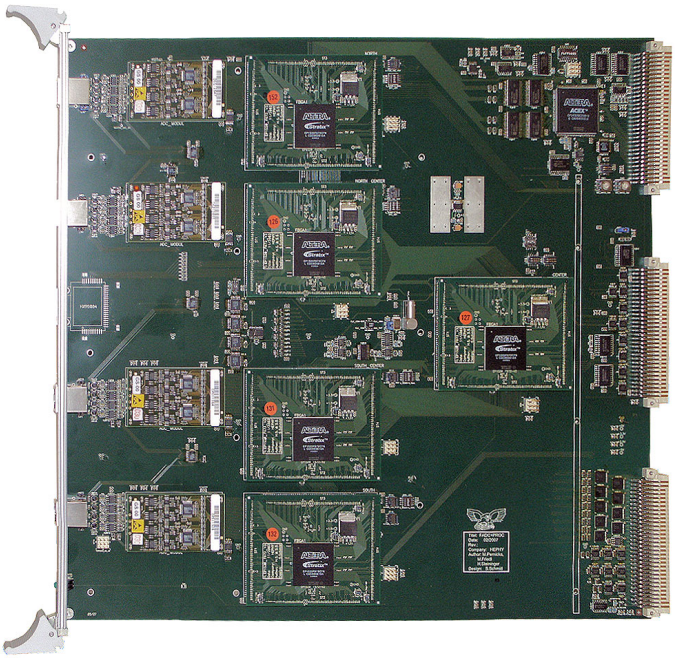

Figure 8: FADC+PROC data processing module.

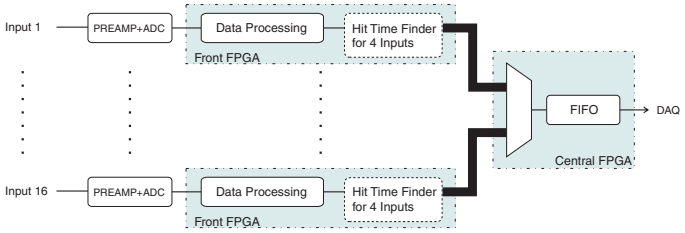

Figure 6: Block diagramm of the data processing chain.

Fig. 6 shows the building blocks of the FADC+PROC devices. At the inputs, there is an adjustable equalizer (to compensate for the limited bandwidth of the $30\,\mathrm{m}$ long cables) and a preamplifier for each channel, followed by a 10-bit FADC and one FPGA for a group of four inputs, coinciding with one side of a silicon sensor. Inside this FPGA, each channel has its

dedicated pipelined processing unit which performs channel reordering (to restore the physical strip order), pedestal subtraction, a two-pass common mode correction and zero suppression (sparsification). In the future, a hit time finder will be implemented after the processing blocks. We will take six samples per trigger, this unit will select the three points around the peak and use an internal look-up table to determine the peaking time and amplitude as well as quality indicators. Computer simulations were performed for such look-up tables, delivering results close to what can be obtained by a numeric fit.

The data of all front-side FPGAs are collected, formatted and buffered in a central FPGA and passed on to the data acquisition system. Presently, this is done through a common platform called COPPER/FINESSE, but in the future we could also implement a Gigabit Ethernet interface directly on the FADC+PROC.

VI. Prototype Results

The prototype system has been extensively tested in the lab and in several beam tests and demonstrated stable, reproducible results with various types of prototype detector modules. The basic functionality of hardware and firmware has been established, yet some details still need fine-tuning. The hit time finding block is being developed but not yet finalized.

So far, the hit time finding was performed off-line by numeric fitting and typically a precision of $2 \ldots 3\,\mathrm{ns}$ could be obtained at a cluster signal-to-noise ratio of $25 \ldots 15$, respectively, when measured against a reference TDC. Fig. 9 summarizes the results obtained with various different prototype modules for the Belle upgrade, depending on the measured signal-to-noise. The accumulated data can be fit by a straight line when plotted in double-logarithmic mode.

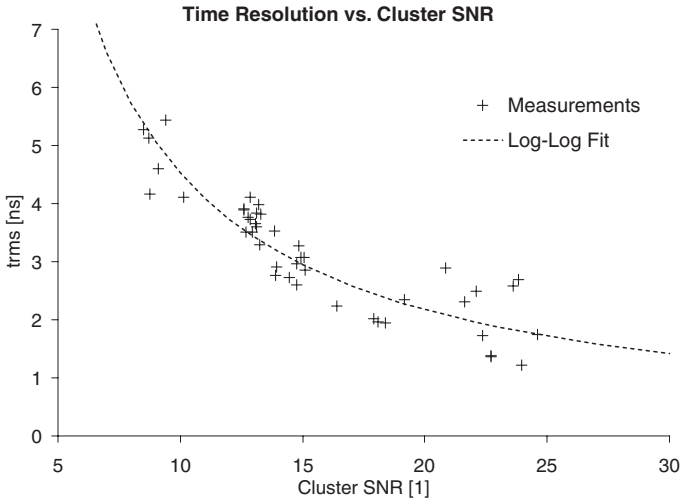

Figure 9: Measured hit time precision versus the cluster signal-to-noise ratio.

The hit time finding can be used to discard off-time background and thus, together with the shorter shaping time of the APV25, reduce the overall occupancy by a factor of up to 100 compared to the present SVD2. [13]

VII. Summary and Outlook

The new Silicon Vertex Detector (SuperSVD) for the future Belle-II is now being designed, based on R&D and experience obtained with prototypes in the past few years. On the silicon detector module level, the Origami chip-on-sensor concept ensures low-mass double-sided readout using thinned APV25 front-end chips with fast shaping and yet excellent signal-to-noise.

Moreover, we have demonstrated a prototype of a fully functional and scalable electronics readout system including voltage level translation, which is achieved by capacitive coupling for analog signals and by optocouplers for the slow control lines. In the back-end, the data are sparsified on-line and hit time finding is used to narrow the acceptance window and thus reduce the overall occupancy considerably. This prototype system yielded excellent results in the lab as well as in several beam tests and is now being scaled up to match the full-sized SuperSVD detector.

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