Novel Charge Sensitive Amplifier Design Methodology suitable for Large Detector Capacitance Applications

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Abstract

Current mode charge sensitive amplifier (CSA) topology and related methodology for use as pre-amplification block in radiation detection read out front end IC systems is proposed[1]. It is based on the use of a suitably configured current conveyor topology providing advantageous noise performance characteristics in comparison to the typical used CSA structures. In the proposed architecture the noise at the output of the CSA is independent of the detector capacitance value, allowing the use of large area detectors without affecting the system noise performance. Theoretical analysis and simulation analysis are performed concerning the operation – performance of the proposed topology. Measurement results on a current mode CSA prototype fabricated with a 0.35 μm CMOS process by Austriamicrosystems are provided supporting the theoretical and simulation results and confirming the performance mainly in terms of the noise performance dependency on the detector capacitance value.

I. Introduction

Noise, power, volume and weight specifications are very stringent in radiation detection applications. Using CMOS technology, that can withstand dose of irradiation, a fully integrated readout front end system can be implemented at low cost. This offers all the advantages of an integrated solution like low power consumption small area and weight. However, the most crucial motivation is that the implementation of readout electronics and semiconductor detectors onto the same chip offers enhanced detection sensitivity thanks to improved noise performances [1]-[6]. Placing the first stage of the front-end close to the detector electrode reduces the amount of material and complexity in the active detection area and minimizes connection-related stray capacitances.

The noise performance of the amplification stage (preamplifier) determines the overall system noise and therefore needs optimization. A folded cascode architecture is commonly used in the implementation of the preamplifier, mainly because of its low input capacitance [6]-[14]. On the other hand a current mode structure could be an attractive alternative to the more typical voltage mode one, since the signal is processed in the current domain, avoiding high voltage swings during charging and discharging of the parasitic capacitance and keeping the internal nodes of the circuit at low impedance values. While many current mode preamplifiers were so far suggested [15]-[19], none has provided any great advantage over the traditional voltage mode structure.

In this work an alternative implementation is presented and configured, providing output noise independent of the detector capacitance thus allowing the use of large area detectors without affecting the system noise performance, high easily adjustable dc gain and satisfactory performance regarding speed requirements.

II. Methodology & Architecture

A current mode approach is used in order to implement an alternative CSA using basically a second generation current conveyor (CCII). A CCII is defined by the following relation between the terminal currents and voltages.

$$\begin{Bmatrix} I_y \\ V_x \\ I_z \end{Bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{Bmatrix} V_y \\ I_x \\ V_z \end{Bmatrix} \qquad (1)$$

where the subscripts x, y and z, refer to the terminals labelled X, Y and Z in Fig. 1. The CCII is defined in both positive and negative version (the +sign is used for the CCII+ type and the –sign for the CCII- type). The current mode preamplifier using a CMOS CCII implementation is shown in Fig. 2. The operation of a CCII cell, it is described using the equations below:

$$i_y = 0,\ i_x = i_z, \text{ and } v_x = v_y, \quad (2)$$

Using the configuration of Fig. 2 a charge signal is fed to the X input node (the detector model is given in Fig. 1, Cd is the detector capacitance) and the output voltage is given by:

$$i_{in} = 0, \text{ and } v_{out} = i_{out} Z_{out} \qquad (3)$$

where the output impedance Zout configured by the parallel connection of Rf, and Cf and using a Laplace representation, is given byUsing the configuration of Figure 2 a charge signal is fed to the X input node and the output voltage is given by (C_d is the detector capacitance):

[1] *Patent pending*

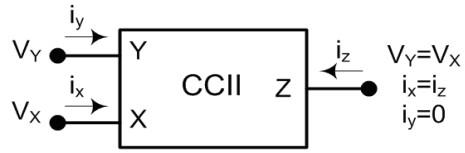

Figure 1: Second Generation Current Conveyor (CCII).

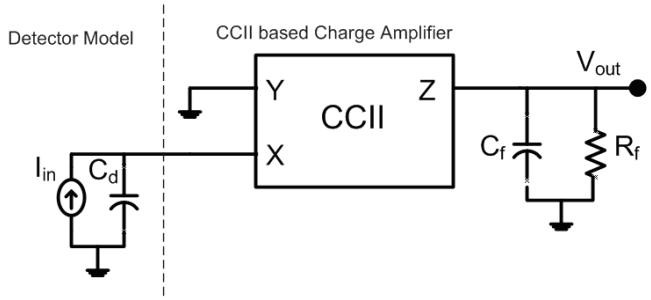

Figure 2: Proposed Current mode CSA architecture

$$Z_{out} = \frac{R_f}{R_f C_f s + 1} \qquad (4)$$

From equations (3) and (4) the transfer function of the circuit is given by:

$$H(s) = \frac{V_{out}}{i_{in}} = \frac{R_f}{R_f C_f s + 1} \qquad (5)$$

The DC gain and the 3-dB frequency of the architecture are $A_{DC}=R_f$ and $\omega_0=1/R_fC_f$ respectively. The particular structure implements a charge amplifier or generally a trans-impedance amplifier function where the gain and the operating bandwidth are determined by the selection of passive elements R_f, C_f. Very important regarding the radiation detection application is the fact that the detector is connected to node X, which is practically a virtual ground since the Y input is grounded. The detector capacitance does not affect the transfer function of the proposed topology.

III. Current mode CSA operation analysis- simulation results

The above alternative CSA was designed and simulated in a 0.35 μm CMOS process (3.3V/5V 2P/3M) commercially available by Austriamicrosystems (AMS) using a previously designed [20] high gain CCII cell. A high gain CCII circuit is similar to a second generation current conveyor but it has a large current gain from X to Z rather than the unity gain of the standard CCII so as to characterize it as a high gain second generation current conveyor [21].This amplifier is constructed by a negative second generation current conveyor and a transconductance output buffer. The CMOS high gain CCII circuit, with a current mirror input stage, was configured in order to implement the particular architecture and it is depicted in Figure 3.

The topology power supplies were VDD = -VSS = 1.65 Volt. The gate of MOSFET Mbias was biased with 970 mV.

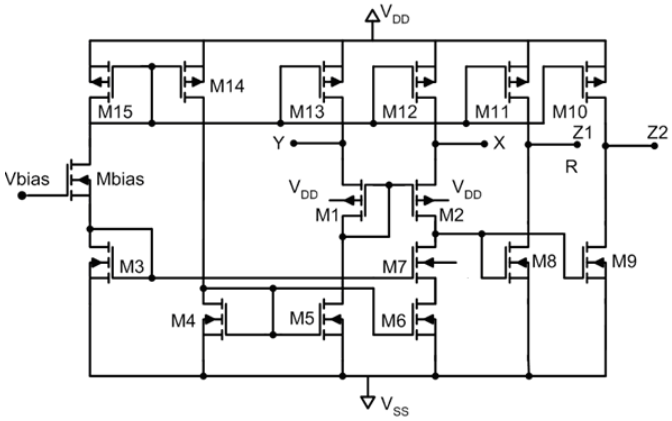

Figure 3: CMOS high gain CCII

All the simulations were performed using HSPICE and SPECTRE simulators and the BSIM3V3.2 MOSFET model (Level 49) at 250C. The simulated AC response of figure 2 charge amplifying topology, for R_f resistor values of 10 kΩ, 32.8 kΩ and 100 kΩ and a capacitance C_f of 20 pF is depicted in Figure 4. Table 1 contains the theoretical and the respective simulated gain and *3-dB* frequency performance parameters. The respective σ% error is below 1% for all three configurations in both gain and operating bandwidth performance, confirming the proposed architecture operation analysis.

Table 1: Current mode CSA theoretical and simulated response

R_f, C_f elements	Gain		3-dB Frequency (kHz)	
	Theory	Simulation	Theory	Simulation
10kΩ & 20pF	80.00	79.98	796.2	795.6
32.8kΩ & 20pF	90.31	90.23	242.8	242.6
100kΩ & 20pF	100 .0	99.76	79.6	79.3

The above analysis confirms the advantageous operation of the proposed architecture since the gain and the operation BW can be easily adjusted selecting properly the passive elements R_f and C_f. In addition, the particular technique provides relatively high gain performance in a wide operating BW. The most important feature of the proposed current mode CSA configuration is that the total output noise and in particular the rms output noise is independent of the detector capacitance value.

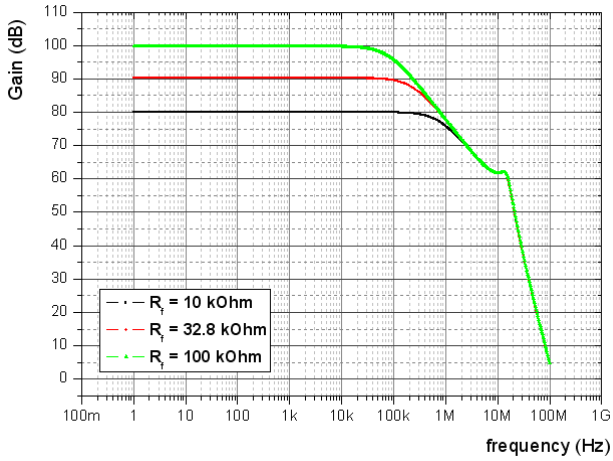

Figure 4: Current mode CSA architecture frequency (gain) response for different feedback resistance R_f values.

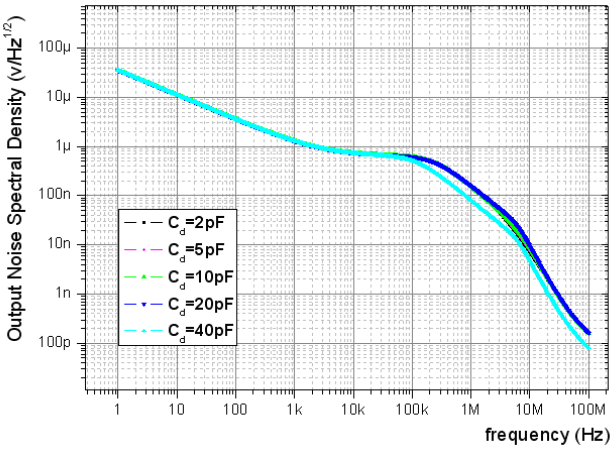

Figure 5: Current mode CSA architecture output noise voltage spectral densities, for different detector capacitance values.

Regarding the noise performance of the proposed topology, a respective simulation is provided in Figure 5. The CCII CSA noise performance was simulated for detector capacitances ranging from 2 pF to 40 pF. The feedback elements R_f and C_f were selected equal to 32.8 kΩ and 20 pF respectively. As it is obvious the noise performance is the same for all the capacitance values in the frequency range up to 100 kHz, which is basically the frequency range of interest.

IV. Measurement Results

The above alternative CSA was fabricated in 0.35 μm CMOS process by Austriamicrosystems (AMS). A photograph (magnified) of the high gain Current Conveyor is shown in Figure 6. The measured input and output signal of the proposed structure for R_f =1 kΩ and C_f = 20pF are depicted in Figure 7 and Figure 8 respectively (transient response), for a detector capacitance value of 2 pF. Regarding the input signal and in particular the detector specifications, the input signal corresponds to a radiation signal of 875Me- charge and time duration of 400 ns (collection of 90% of the total Q). The detector leakage current is equal to 10 pA.

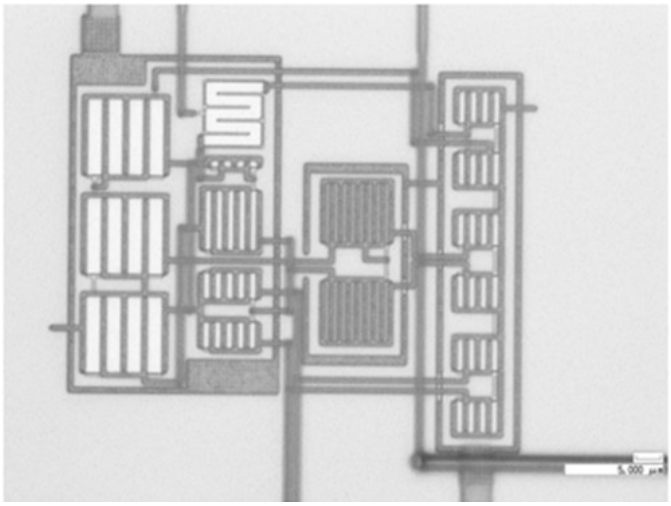

Figure 6: Magnification of the second generation high gain current conveyor circuit.

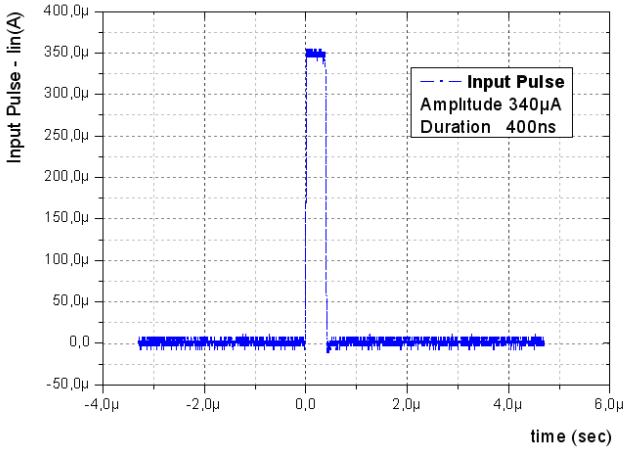

Figure 7: Current mode CSA measured input signal

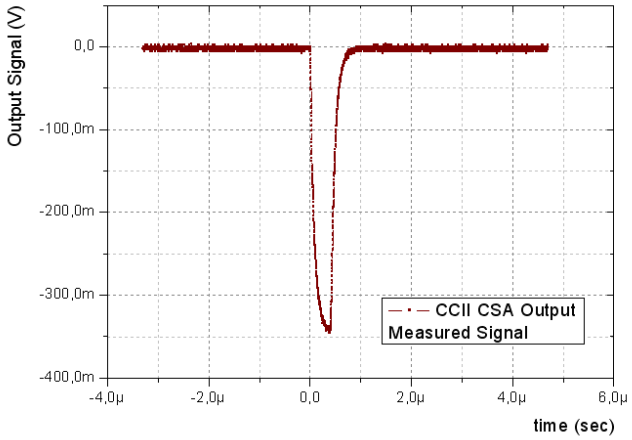

Figure 8: Current mode CSA measured output signal.

The proposed topology can detect and amplify the input signal and implements a charge sensitive pre-amplifier stage providing easily achievable application specified charge and discharge times and high gain performance for a relatively large operating bandwidth. Respective noise measurements in relation to the above noise simulations were also performed. Measurement results are depicted in Fig. 9. These results confirm the theoretical analysis and the simulation results since the output rms noise is independent of the detector capacitance value.

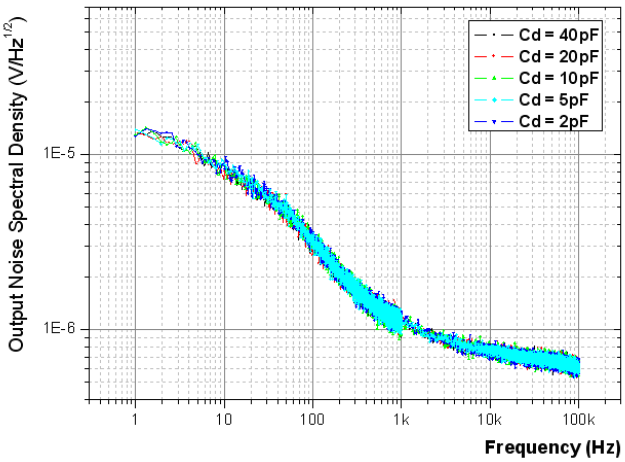

Figure 9: Measurement of the Current mode CSA output noise performance.

V. Summary

An alternative novel current mode CSA topology and a related methodology are proposed, for use in capacitive radiation detection read out front end IC systems. It is based on the use of current mode topologies and in particular on a current conveyor suitably configured. A transimpedance amplifying topology is presented, showing advantage for charge amplification, providing easily adjustable gain and operating bandwidth. The proposed structure is fully integrated and provides advantageous noise performance for large detector capacitance applications since the detector capacitance is not included in the transfer function and does not affect the bias of the input stage. The proposed topology can be implemented using a variety of current mode circuits like CCI and other current mode architectures, suitably configured.

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