Development and commissioning of the ALICE pixel detector control system

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on behalf of the Silicon Pixel Detector project in the ALICE collaboration

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Abstract

The Silicon Pixel Detector (SPD) is the innermost detector of the ALICE Inner Tracking System and the closest one to the interaction point. In order to operate the detector in a safe way, a control system was developed in the framework of PVSS which allows to monitor and control a large number of parameters such as temperatures, currents, voltages, etc.

The control system of the SPD implements interlock features to protect the detector against overheating and prevents operating it in case of malfunctions. The nearly 50,000 parameters required to fully configure the detector are stored in a database which employs automatic configuration versions after a new calibration run has been carried out. Several user interface panels were developed to allow experts and non-expert shifters to operate the detector in an easy and safe way.

This contribution provides an overview of the SPD control system.

I. The Silicon Pixel Detector

SPD is based on a hybrid silicon pixels technology and contains around 9.8 M read-out channels. It is composed of 120 half-staves (HS) mounted on 10 carbon fibre supporting sectors (Fig. 1). Each half-stave is made of two ladders, a Multi Chip Module (MCM) and an aluminium-polyimide multilayer bus. Each ladder consists of 5 front-end chips flip-chip bonded to a 200 microns thick silicon sensor [1].

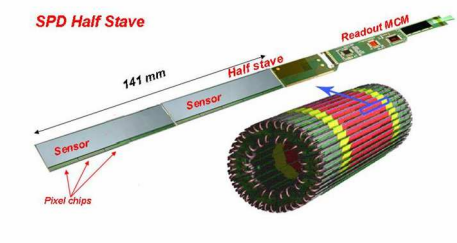

Figure 1: The Silicon Pixel Detector

The MCM constitutes the on-detector electronics and performs operations such as clock distributions, data multiplexing, etc. The multilayer bus provides the connection between the MCM and the front-end chips, while communication between the MCM and the off-detector electronics (Routers) is assured by three single-mode optical fiber links.

The SPD low voltage power supply (PS) system is based on 20 CAEN A3009 dc-dc converter modules (1 for each half sector) housed in 4 CAEN Easy3000 crates located about 40m from the detector. The sensor bias voltage is provided by 10 CAEN A1519 modules (1 for each sector) housed in a CAEN SY1527 mainframe 100 m away from the detector.

II. Overview of the Detector Control System

The DCS plays a leading role in operating the SPD and fulfils very stringent requirements. The ALICE Detector Control System (DCS), as well as all the LHC experiments, is supervised by a SCADA system (Supervisory Control and Data Acquisition) based on a software platform called PVSSII [2].

The aim of every control system is to supervise all the operations carried out in its structure and to react promptly in case of misbehaviors. The ALICE DCS group, in collaboration with every detector, foresaw a series of constrains to integrate the control system of each sub-detector into a unique control system. The DCS of the SPD was designed according to such requirements. Standard components were mainly used to reduce maintenance efforts and, in few cases, dedicated components were developed for specific and innovative tasks.

The block diagram shows the connections between the hardware and software components (Fig. 2).

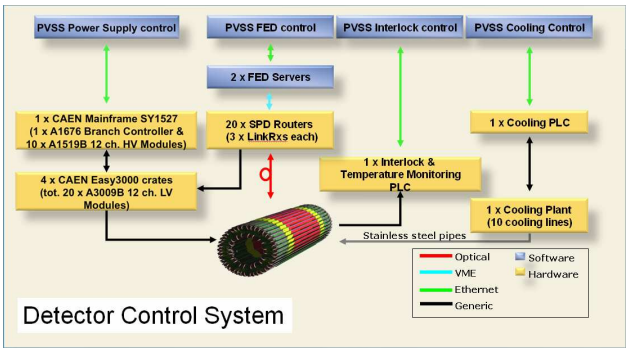

Figure 2: Detector control system scheme

There are 4 sub-control systems: PS control, Interlock control, Cooling Control and the Front-End driver (FED) control. The first three directly communicate with the hardware via Ethernet (TCP/IP, OPC protocol), while the last one uses the same protocol to connect to the FED, which is the driver that communicates with the off-detector electronics (20 routers) via a VME bus.

PVSS provides the interface between the hardware components and the control logic units which are supervised by the Finite State Machine (FSM).

The FSM connects the defined logical states of the detector components and sends macroinstructions (i.e.: Go Off, Go Ready, etc) via PVSS: a macroinstruction is a sequence of operations addressed to the hardware. The correct sequence of actions is checked and possible errors are detected. The FSM also has the task of providing the ALICE DCS with information regarding the status of the SPD (i.e.: Ready for data-taking, calibrating, etc.).

PVSS is designed for slow control applications and it is not suitable for direct control of fast front-end electronics.

The FED was built to interface the PVSS layer with the SPD electronics. It controls two Front-end device servers (C++ based) [3], it receives macroinstructions and autonomously operates the front-end/off-detector electronics. It is provided with an Oracle database interface that operates the whole SPD configuration. The FED can read and save all the required parameters in the Configuration Oracle Database (CDB).

The DCS of SPD is divided into 4 different PVSSII projects which run in 4 computers: 3 working nodes and 1 operator node. These projects constitute a distributed system and they communicate with one another through an Ethernet (TCP/IP) protocol. The working nodes are installed on 3 Windows XP machines, accessible only to expert users; they are the computers used to control the detector. The User Interface (UI) is installed in the operator node where all users can login and it is equipped with a Windows server 2003.

The UI is the graphic interface tool that allows users to monitor and manage the detector in a careful way.

A. *Finite state machine*

The Finite State Machine is based on a State Management Interface (SMI++) [3] and it is the logical part of the DCS (Fig. 3) since it manages the starting, intermediate and final states of the subsystems and it also reacts according to their changes (Ready, McmOnly, Error, Off...).

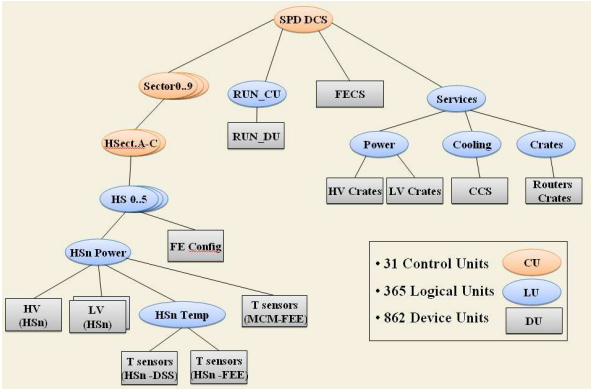

Figure 3: SPD Finite State Machine scheme

The hardware system is represented by the Device Units (DU). It contains 862 DUs which transmit their state to 31 Control Units (CU) through 365 Logical Units (LU). Therefore, any signal is transmitted from the bottom to the top and actions are carried out according to the kind of signal.

All information passes through the Top Node which communicates with the ALICE control system.

The CUs are connected to some background scripts (running) which constantly check the system stability allowing or forbidding to carry out the commands sent by operators. On the contrary, if a DU changes its state, the information is sent to the upper nodes through the LUs and the CUs modify their state accordingly.

The CUs allow to intervene only in the concerned parts of the detector without affecting its global operating state. Further details are available in the bibliography [4].

B. *Cooling system and interlocks*

The cooling system is very important and it must be in full working conditions for SPD to run efficiently. Since every HS dissipates ≈ 12.5 W (corresponding to about 1.5 KW for the whole detector) and having the detector a very low mass, a C_4F_{10} evaporative cooling system was chosen.

The cooling plant is controlled by a PLC. An OPC Server-client protocol is used to communicate via Ethernet (TCP/IP) with the control PC.

Should the cooling system be suddenly switched off, the temperature rise in the half-staves would increase by 1^{o}C/s and this would irreparably damage the detector in a few seconds. Several interlock levels (hardware and software) act in parallel to switch off the power supply in case of misbehavior.

Two redundant chains of 5 temperature sensors (Pt1000) each installed on the upper surface of all half-staves provide the relevant temperature for the interlock system. One chain is directly connected to the PLC analog input modules, while the second one is read-out through the MCM which transmits the temperature values to the routers. In case a half-stave exceeds a threshold temperature value (usually set at 40°C) the above mentioned hardware interlocks act on the Low Voltage (LV) board switching off the concerned half-sector.

The cooling plant is provided with a further interlock system composed of 11 hardware interlock channels. One of them acts on all the low voltage modules and switches off the whole detector in case of cooling plant failure (i.e.: pressure instability, high temperatures in the boosters, etc...). The other ten channels instantly switch off only the corresponding single sector in case the relevant cooling line is faulty.

The main difference between hardware and software interlocks is their reaction time. The hardware interlocks instantly react switching off the power supply of the whole detector or, in case of temperature peak (spike) in a HS, they switch off the power supply of the half sector that hosts it. As regards the software interlocks, two levels were implemented; their reaction time is slower than the hardware ones because they are transmitted through the communication protocols of the control system. Nonetheless they offer a great advantage since they can intervene on single half-staves. The first software interlock level forbids operators to switch on a HS if the measured temperature is higher than 22°C; the second level switches off single HSs in case their temperature

exceeds 38°C. These operations are carried out thanks to a background script that individually intervenes in the channels of the LV supply module.

C. User Interface

Simplified panels, in accordance with the ALICE UI framework, are provided to monitor and operate the detector. The latter is schematically reproduced in the middle of the UI; each color is associated to a hardware condition (Green= Ready state , Red = Error State…).

Detailed panels showing the values of hardware subsystems are also available (Fig. 4).

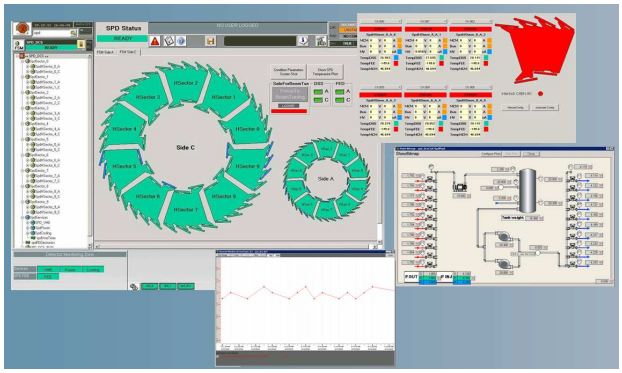

Figure 4: User Interface panels

The temperatures, voltages and currents of the HSs, as well as the main cooling plant operation parameters are archived in a dedicated database and can be displayed in tables and plots or saved in text files for offline analysis.

D. PVSS -Database Connection

The system configurations are stored in an Oracle based Database named Configuration Database (CDB). The ALICE DCS group provides the infrastructure and the CDB maintenance, however every detector can autonomously chose how to manage its own database.

The SPD configurations are stored in the Configuration Database (CDB) and each version contains 52,800 DACs values.

The Database design is an optimized structure that creates new configuration versions without data duplication. When DACs values are changed, the DB generates a new configuration version number and the full configuration is retrieved by the FED through the rearrangement of the pointers (Fig. 5).

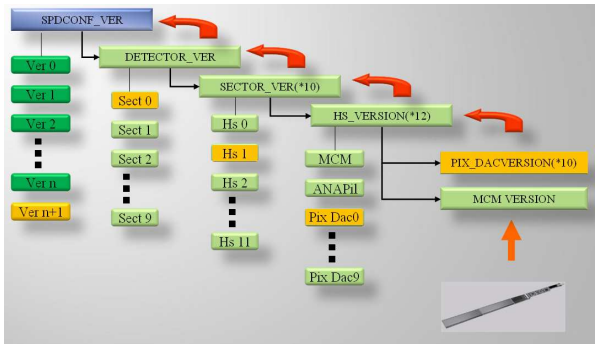

Figure 5: Saving a configuration structure

A direct connection between PVSS and the CDB was implemented to control the working configurations stored in the CDB in a more efficient way (Fig. 6). Making use of library functions in the framework of PVSS and adjusting them to the CDB structure it is now possible to raise predefined queries to the SPD CDB and to show their results in the UI panels. This way we can directly gain access to the several configurations. As a matter of fact, some panels were implemented to compare the configurations of different HSs or the ones of a same HS in order to monitor the way it worked during a slot.

Recently we have developed a hardware system that allows to detect errors coming from the detector (i.e.: optical connection status and data format errors, front-end and back-end errors, wrong trigger sequences, etc.) [5] also while data are being taken. The routers send such errors to the FED which carries out an online pooling operation and stores them in a dedicated table in the DB. As soon as the FED detects any errors in the routers, it generates a signal that is transmitted to the operator via PVSS. Therefore the direct connection between PVSS and the database provides the operator with information concerning such errors without interfering in data taking operations.

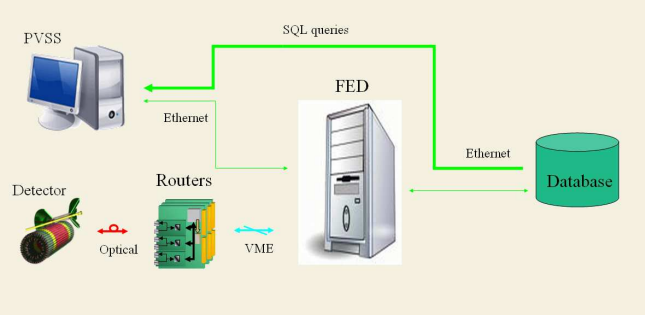

Figure 6: Schematic of the PVSS-DB connection

This improvement made the storing procedure more user friendly. Besides, thanks to the panels containing the predefined queries operators can get real-time information regarding the detector state and therefore be able to monitor it in a more useful and efficient way.

III. Final Commissioning and Tests

In 2007 the DCS pre-commissioning was carried out at the CERN Departmental Silicon Facility (DSF) laboratory.

The control system was moved to the ALICE Control Room (ACR) at the end of 2007 and since then the commissioning has been carried on with improved automatic functionalities that allow experts and shifters to operate and monitor the detector in a more and more effective way.

Since then, any hardware and software further developments are first of all tested in the setup maintained in the DSF.

The efficiency of the interlocks was proven when it promptly reacted by switching off the SPD during normal operations as a consequence of external alarms.

The SPD control system is completely integrated in the ALICE DCS from which the detector can be monitored and directly operated.

During the cosmic runs that took place in 2008, SPD collected data for more than 200 hours. In August 2009 the SPD took part in the ALICE cosmic program with magnetic field providing the L0 trigger signal for about 280 hours.

IV. REFERENCES

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