Smart Analogue Sampler for the Optical Module of a Cherenkov Neutrino Detector

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Abstract

A transient waveform sampler/recorder IC has been developed and realized in AMS C35B4 technology. This chip has been designed to fit the needs of a proposal for a front-end architecture for the readout of the anode signal of the photomultipliers in an underwater neutrino telescope.

The design is based around a 3 channels x 32 cells switched capacitor array unit sampling its voltage inputs at 200MHz external clock rate and transferring the stored analogue voltage samples to its single analogue output at 1/10th of the sampling rate. This unit is replicated inside the ASIC providing 4 independent analogue sampling queues for signal transients up to 32 x 5 ns and a fifth unit storing transients up to 128 x 5 ns. A micro-pipelined unit, based on Muller C-gates, controls the 5 independent samplers.

This paper briefly summarizes the complete front-end architecture and discusses in more detail the internal structure of the ASIC and its first functional tests.

I. Introduction

The use of an analogue sampler/recorder for the purposes of the front-end electronics of a Cherenkov neutrino telescope demonstrated its effectiveness in detectors such as ANTARES, Nestor and IceCube. The readout system of those detectors provides the time-stamping of single photoelectron (SPE in the following) signals produced by photomultipliers (PMTs) while separating them from background and bioluminescence events which mainly contributes to the acquisition dead-time [1].

The solution presented in this paper has been tailored to sustain an event rate of short pulses (namely: PMT events not longer than about 150 ns and with an amplitude not larger than about 600 mV for a SPE) in excess of 300 kHz with a negligible dead-time. At the same time the architecture must also offer the way to record PMT events longer than approximately 500 ns, as observed in physics simulations of a model detector.

This architecture may equip a single PMT and be placed inside the same pressure-resistant container (Optical Module: OM in the following) or externally to it: one key point is the choice of having an analogue treatment of the PMT signals based on commercial components which could be easily changed during prototyping, allowing the use of the same conceptual architecture even if the board containing the front-end electronics is placed at distances in the order of a few metres from the PMT.

This section introduces the main logical blocks inside the proposal and describes the role played by the ASIC (SAS: Smart Analogue Sampler) which has been designed and prototyped in AMS CMOS 0.35 µm technology.

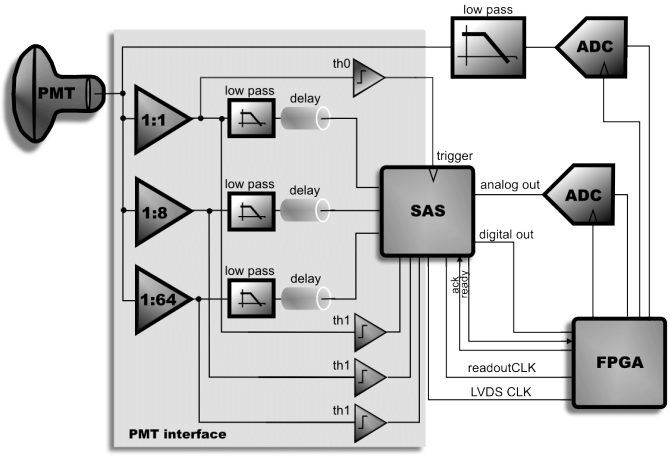

Figure 1: Block diagram of the proposed front-end architecture

A. Optical module front-end

The proposed architecture [2] is based around five main building blocks:

- a mixed-signal ASIC, providing the capabilities of a four layer first-in first-out analogue transient recorder,
- a PMT interface, built with commercial components;
- two commercial ADCs, one providing the digitization of the analogue signals sampled and stored by the ASIC and the other the digitization of a low-pass replica of the PMT output;
- a FPGA, controlling the data transfer between the ASIC and its ADC, the digitization issued by the second ADC and the packing of the digital data into larger frames to be sent to the data acquisition system;

all these functionalities are achieved on the same board constituting the front-end electronics of a single PMT.

Figure 1 shows a functional block diagram summarizing the architecture: it depicts a conceptual view of the PMT interface components and the simplified connection scheme between the SAS the two ADCs and the FPGA.

Two separate prototypes – of the PMT interface and of the ASIC – have been realised: a complete prototype board hosting all the building blocks has been designed and is being produced at the time of writing of this paper.

This board receives the slow control and the synchronous clock (the broadcast distribution of a synchronous protocol for clock and data to all the OMs in the detector is described in [3]) and transmits the collected data out of the OM.

B. Store and forward architecture

The data acquisition provided by the architecture is of the store-and-forward type: the off-shore front-end electronics is clocked synchronously by a broadcast signal distributed to all the OMs and all the stored events are time-stamped at the moment they trigger the acquisition. The timing information is then packed together with the digital data to be sent on-shore.

The digital time-stamp feature is provided by the ASIC which contains a 17 bits counter: its content is stored in the *record* which is built each time that an external trigger arrives. This record is constituted of two parts: a digital part, which is stored inside a digital 4-levels FIFO, and an analogue part, consisting of the analogue voltage samples stored in the memory cells. When a readout is made all this information is transferred from the ASIC toward the FPGA (with a digitization of the analogue samples provided by the ADC), making available again the storage area for the next events.

The main synchronization clock runs at 200 MHz and a re-synch pulse is issued from shore each 500 μs in order to verify the timing integrity of the clocks local to each OM: a synchronizing feature is provided by the ASIC, issuing an external pulse on one of its output pins (not shown in Figure 1) each time that the synchronization input is in phase with the internal counter. A missing pulse on this output indicates that the synchronization has been lost during that particular 500 μs interval: this is monitored through the FPGA and the data collected during this time slice should be discarded.

The trigger signal for the start of the sampling is provided by the PMT interface through a threshold comparator: a transition on this signal is issued each time that the PMT anode signal crosses the level-0 threshold (about 1/3 of single photoelectron). On the rising edge of the trigger and after a short delay produced by the ASIC internal logic, the sampler is then started for a minimum time window length of 160 ns. During this period the permanence of the anode signal over the threshold is checked again: a decision is then taken whether or not continuing the sampling for a larger period of time. This criterion is described in section II.C.

C. The ASIC architecture

The analysis of the transients produced by MonteCarlo simulated events on a model detector led to the adoption of a front-end architecture based around an analogue buffer of four analogue memories, configured in a first-in first-out structure [2] with these memories providing sampling and storing for a foreseen maximum rate of about 300 kHz pulse transients not longer than 160 ns.

The acquired voltage samples would then be serially digitized by an ADC and the digital data transferred to the on-board FPGA. The digital part of the event record, containing the time-stamp, the address of the analogue buffer used for the sampling and the signal classification code, is directly sent to the FPGA, through a serial output, during the readout of the memory content. The latency of this transfer is actually dominated by the analogue part of the record.

Other considerations required the integration inside the architecture also of a larger analogue memory, with the purpose to provide sampling and storing of transients longer than 160 ns (seldom produced by the PMTs). For that reason the architecture also integrates an independent memory offering the same sampling and storing features as the others but 4 times longer (namely, offering storage for transients falling in a time window of 4 x 160 ns). The decision whether to start the sampling of this second unit is taken inside the ASIC during the acquisition of the first 160 ns as described in section II.C.

II. The proposed front-end architecture

The initial considerations which originated most of the design choices of the front-end will be now shortly reviewed and a general description of the architecture will be given. Furthermore, the signal chain – constituting the PMT interface and the basic signal classification scheme used inside the architecture – will be discussed.

A. Considerations on signal range

The analysis of the simulated high energy neutrino events in a model detector showed that events having an amplitude range of about 1000 photoelectrons and lasting less than 500 ns could be produced within the detector and provide useful information for the physics.

At the same time laboratory measurements on a 10" PMT, operating with a gain of 5×10^7, with an anodic load of 50 Ohm (which produces a SPE signal having an amplitude of about 50 mV with a rise time of about 2.6 ns) showed a linear characteristic curve up to about 100 photoelectrons.

Such considerations lead to the observation that, in order to increase the linearity range of the PMT front-end electronics, two strategies could be followed: both increasing the anode load and dividing the amplitude range over multiple input sub-ranges.

The choice of increasing the anodic load also brings the benefit of decreasing the PMT gain, leading to an increase of its average life time.

The second strategy is implemented replicating through different gains the anode signals and then sampling all these replicas: a classification circuit passes to the sampler unit the information relative to the amplitude of the anode signal. Depending upon this classification, only one of the different replicas will be transferred from the sampler to the ADC for digitization.

A signal path from the PMT to the SAS consisting of three channels with three different gains is shown in Figure 1: this path is implemented with commercial components and feeds the input signals of the sampler. The electronics constituting the signal chain, together with the classification circuit, forms the PMT interface block of the front-end architecture [4].

B. Signal input chain

Figure 1 shows that each signal channel inside the PMT interface is made of three logical blocks: a gain block, a low pass filter and a delay block.

The three gains have been selected in order to fully exploit the linearity characteristic of the PMT up to about 500 photoelectrons, providing three sub-ranges of 1 V each. As shown in Figure 1, the first channel is a buffered replica of the anode signals, the second is reduced by a factor 8 and the third by a factor 64. The anode load offered by this PMT interface is 600 Ohm (see [4] for a detailed description).

A sampling rate of 200 MHz has been chosen in order to minimize the amount of data that must be transferred after digitization: a reconstruction algorithm applied to filtered and sampled anode signals already demonstrated an attainable time resolution better than 300 ps with a relative charge error better than 3%. The anode signals are filtered in order to present an attenuation of at least 60 dB at 100 MHz (10b over a 1 V range is the specified resolution of the signal front-end) right after they are attenuated by the three channel gains.

A solid state delay line is also introduced on the signal path in order to take into account the delay needed by the electronics used for the signal classification and inside the ASIC to actually start the sampling after having received the trigger signal. This delay also takes into account the necessity for the timing reconstruction algorithm to have at least a few points of the signal baseline sampled.

C. Signal classification

The architecture classifies input signals following two different criteria: the first is based on the signal amplitude and the second on a time-over-threshold criterion. The classification is made partially within the ASIC (time classification) and partially by a set of comparators on the board. The outputs of those comparators are used by the ASIC to apply both the classification criteria.

Two sets of comparators are shown in Figure 1: the three comparators labelled as *th1* operate with the same threshold and their outputs are the 3 bit classification of the anode signal amplitude. This is the amplitude classification criterion: that code is stored in the event record built when a trigger arrives and is later used, during the readout phase, to decide which one of the three sampled channels will be transferred to the ADC. The choice to transfer toward the external ADC only one channel out of the available three is crucial for the transfer latency of the architecture in the presence of high rates of short PMT signals.

Still referring to Figure 1, the *th0* comparator operates with a 1/3 SPE threshold and produces the trigger pulse, starting the ASIC acquisition. After 100 ns from this start, the SAS stores the amplitude classification code and the status of this comparator output: if this status bit is found high then at the end of the 160 ns sampling period, the signal acquisition will be continued by the longer memory unit described in section I.C. If this unit is still storing samples from a previous acquisition which has not yet being read, the SAS ends its sampling after 160 ns and this condition is signalled to the FPGA. Samples acquired by the 128 cell memory are all converted by the ADC and transferred to the FPGA: the analogue part of the record is stored in this case in a total of 3x128 cells plus the 32 cells of the analogue FIFO.

III. The SAS ASIC

This section discusses in more detail the design choices made for the realization of the ASIC. A basic macrocell has been first designed and used as a building block for the core of the ASIC. A complete library of asynchronous cells has also been realized and used for the design of the digital FIFO and of the ASIC control unit.

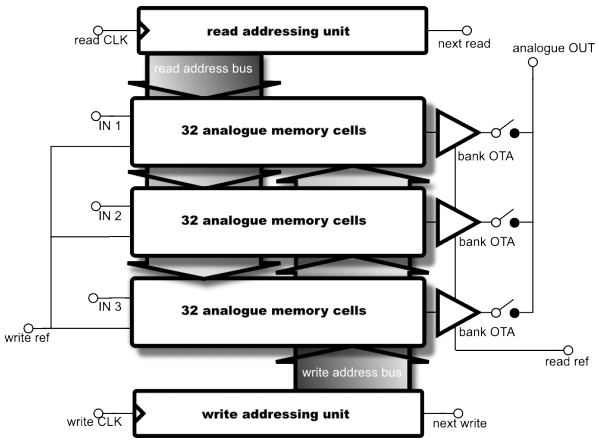

Figure 2: SAS analogue memory macrocell block diagram

A. Analogue memory macrocell

The core of the SAS is built around an analogue memory macrocell. A block diagram of that macrocell is shown in Figure 2. The memory cells are serially addressable using two external clocks: once the addressing units are initialized to the first cell, each pulse issued on one of the two clock inputs shifts the writing or read address to the next cell. There are 96 memory cells inside each macrocell organized in three channels: writing proceeds in parallel along each channel while the readout is always sequential.

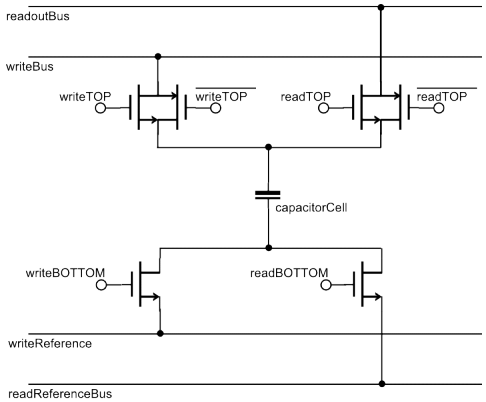

Figure 3: SAS memory cell schematic

Voltage samples stored in the memory cells are shifted through a single output allowing the serial readout of only one channel or of the 32 x 3 cells constituting the memory.

The addressing units are simple linear shift registers with a serial input and 32 parallel outputs: both of them use

additional logic cells in order to properly shape the width of the output signals. In particular, the write address unit must provide two different pulses in order to separately control the opening of the memory cells write switches (see Figure 3).

The timing of the falling edge of those pulses implements the so-called bottom sampling strategy: the opening of the *writeTOP* CMOS switch slightly precedes the opening of the *writeBOTTOM* switch allowing the injected error due to the parasitic charge present in each switch, to be (to first order) signal independent.

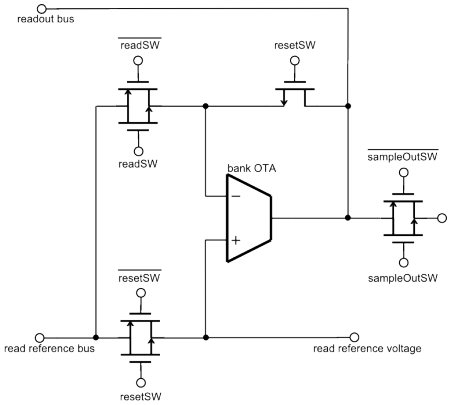

Figure 4: Schematic of the SAS macrocell readout configuration

The write addressing unit uses True Single Phase Clock dynamic flip-flops to attain the sampling speed of 200 MHz while static CMOS flip-flops are used by the read addressing unit which, during the readout, must attain a readout rate of 40 MHz.

The analogue multiplexer shown in Figure 2 on the output of the macrocell controls the readout behaviour of the memory: depending on the state of the amplitude classification only one channel is switched to the single analogue output of the macrocell. The same multiplexer is also used to sequentially switch through the single analogue output all the 3 x 32 cells of the memory: this solution is used during the readout of transients longer than 160 ns. Figure 4 details the readout configuration used in the macrocell [5].

All the *analogue OUT* connections of the 8 macrocells constituting the chip core are routed to a single node: when the macrocell is idling, storing data or waiting for a trigger, all the outputs of the three bank amplifiers are left open, allowing other macrocells to be read out. Each macrocell is strictly a single-port memory: only writing or reading can happen at the same time on the same unit. The output configuration allows indeed the simultaneous serial writing of more than one unit while another is being readout.

The ASIC uses that macrocell to implement the two analogue memories' functionalities described above: the FIFO analogue buffer and the 128 cell unit. Figure 5 shows a block diagram of the SAS ASIC: the same macrocell here is replicated 8 times and 6 different clock domains are shown. Clock domains from *CLK1* to *CLK4* are commuted in sequence each time that an analogue transient must be stored into the analogue FIFO. Clock domain *CLK5* is only commuted after the analogue transient has passed the time classification criterion described in section II.C. The clock domain produced by the internal LVDS clock buffer is always sent to the 17 bits synchronous counter and used by the control unit to derive the other 5 domains. The initialization logic inside each macrocell provides a means to immediately start the sampling of the analogue signals when the first *writeCLK* pulse arrives and to do the same for the readout of the macrocell when a *readCLK* pulse is sensed.

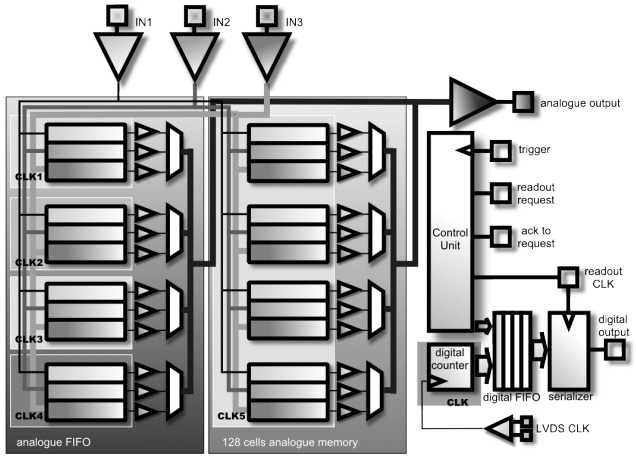

Figure 5: SAS conceptual block diagram

Still referring to Figure 5, we note how all the internally buffered input signals are permanently connected to the eight analogue memory macrocells. The four on the left implement the four level analogue FIFO buffer and are activated in a circular way: each time that the control unit dispatches the 200 MHz clock to one of the *CLK1-4* domains, the sampling starts. Similarly, the four macrocells on the right are all sharing the same clock domain: their acquisition is then started when the control unit commutes *CLK5* on.

The analogue samples stored by each memory are available on the single analogue output pin after the issuing of a *request* action in the SAS *readout request* output pin. The serial shifting of the cell addresses by the read address unit is controlled by the external *readoutCLK* signal: each pulse issues the readout of a single memory cell.

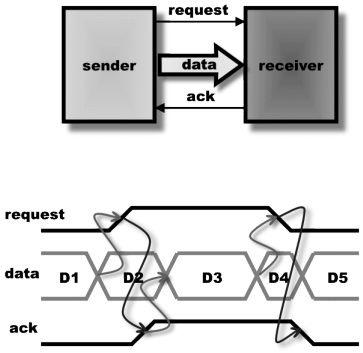

Figure 6: Two-wires asynchronous protocol used in the SAS

B. Asynchronous control unit

The 200 MHz clock is internally produced by a LVDS receiver and used to control the write address units of each sampling macrocell: it only needs to be dispatched to the active memory unit during its sampling window for the sampling to start. The control unit which dispatches this clock to the sampling macrocells doesn't need then to be clocked: a fully asynchronous design has been implemented instead. The

overall synchronization strategy used within the control unit and also at the external chip communication layer is based on a simple two-wires *request-ack* protocol.

In that protocol each block transfers data with its own neighbour based on the approach depicted in Figure 6: when data are ready at the sender output, a *request* action is issued. Then the data are consumed by the receiver block and must remain valid on the sender output until an *ack* action is issued by the receiver: this action allows the production of new data by the sender and the restarting of the cycle. Both actions consist of simple level transitions on the two wires used for flow control (low to high and high to low transitions are equally valid actions).

The implementation of this protocol inside the chip has been accomplished using a design strategy based on transparent latches and a control flow circuit based on Muller C-gates [6]. Figure 7 shows the control flow circuit used for the realisation of the digital FIFO which stores the digital data of the output record.

The same C-gate is at the basis of all the synchronization logic operating within the control unit: this unit is normally idling waiting for a rising edge on the chip trigger input. During idle the 200 MHz clock is only used by the 17 bits synchronous counter: a rising edge on this input makes the control unit copy the counter value into the digital FIFO

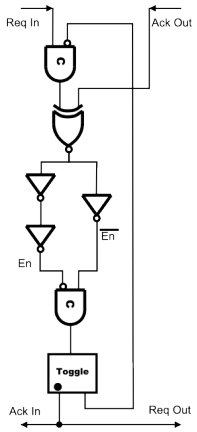

Figure 7: Digital FIFO: control flow circuit

and launch the analogue sampling of the first available unit in the analogue buffer. If all the units contain valid data waiting for a pending readout, then the trigger event is discarded. When the writing address unit of the sampling macrocell reaches its 20th cell, the status of the input trigger is stored into the digital FIFO together with the 3 bits classification code, adding this information to the time-stamp already stored. If the status of the trigger signal is low at this point, the sampling proceeds till the 32nd memory cell of the macrocell and the control unit issues a *request* action on the SAS output pin signalling that a complete record is ready to be read out from the memory. If the status is high, then the sampling of all the input signals is continued by the 128 cell unit. The issuing of the *request* action is then delayed until it reaches the last memory cell.

The same status is checked again before that unit ends its sampling: this will eventually be communicated to the FPGA which then starts the digitization of the signal filtered by the low-pass filter (see Figure 1).

IV. Functionality test and conclusions

The first samples of the SAS ASIC were received before the board containing the PMT interface, the ADCs and the FPGA was designed. The functional test of the chip was then carried out using a two faces board with a socket and the power supply filters: the analogue output was observed with a scope and the digital output trough a state analyser. The trigger as well as the *ack* control signal and the classification status bits are emulated using a pattern generator while the 200 MHz LVDS clock used for the sampling is generated by a free running signal generator. Another signal generator provides the analogue waveforms which are sampled by the analogue memories: controlling the timing delay between the input signal and the trigger starting the SAS acquisition allows the measurement of the actual delay between the external start and the first sample acquired by the analogue memory.

Functional tests conducted with this set-up showed that the desired readout rate of 40 MHz could not be achieved: the origin of this problem has been traced back to a wrong design of the bias network of the macrocell bank amplifiers. Tests have been performed at the degraded readout rate of 5 MHz and showed a good signal reconstruction of fast analogue pulses (50 ns input rectangular pulse with 20 ns rise time) up to a 1.8 Vp-p amplitude. The overall power consumption is less than 170 mW (less than 50 mA at 3.3 V power supply) and somewhat larger than expected: also this problem appears to be bound to the same origin.

Though more extensive tests will be performed when the board integrating the ADC and the FPGA will be available, the mentioned problems clearly require another foundry run.

V. Acknowledgements

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