

Progress on DC-DC Converters for a Silicon Tracker for the sLHC Upgrade

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Abstract

There is a need for DC-DC converters which can operate in the extremely harsh environment of the sLHC Si Tracker. The environment requires radiation qualification to a total ionizing radiation dose of 50 Mrad and a displacement damage fluence of $5 \times 10^{14} / \text{cm}^2$ of 1 MeV equivalent neutrons. In addition a static magnetic field of 2 Tesla or greater prevents the use of any magnetic components or materials. In February 2007 an Enpirion EN5360 was qualified for the sLHC radiation dosage but the converter has an input voltage limited to a maximum of 5.5V. From a systems point of view this input voltage was not sufficient for the application. Commercial LDMOS FETs have developed using a 0.25 μm process which provided a 12 volt input and were still radiation hard. These results are reported here and in previous papers. Plug in power cards with $\times 10$ voltage ratio are being developed for testing the hybrids with ABCN chips. These plug-in cards have air coils but use commercial chips that are not designed to be radiation hard. This development helps in evaluating system noise and performance. GaN FETs are tested for radiation hardness to ionizing radiation and displacement damage and preliminary results are given.

I. INTRODUCTION

The Silicon Tracker of the Inner Detector of Atlas for sLHC presents a difficult environment for electronics and power supply development in particular. With the high 2 Tesla magnetic field all magnetic materials would go into saturation and not be usable. For inductors and transformers this leaves only nonmagnetic cores which greatly increase the size of the components. For a DC-DC converter the most promising approach is a buck converter. It can be constructed with only one inductor, an integrated circuit and a few discrete components.

In addition to the strong magnetic field there is also a harsh radiation environment. The requirement is a Total Ionizing Dose (TID) of about 50 Mrad along with a Non Ionizing Energy Loss (NIEL) requirement of $5 \times 10^{14} / \text{cm}^2$ of 1 MeV equivalent neutrons. This excludes almost all switching devices that could be used in a buck converter and until recently did not have a technical solution.

It is known from previous work at CERN and elsewhere that some small feature CMOS processes are radiation hard. Starting from this point; in February 2007 an Enpirion EN5360 Converter was exposed to 100 Mrads of gammas with no appreciable changes. Many commercial buck converters based on small feature processes were tested for radiation hardness but with one exception (EN5360) the tested converters failed after only a few hundred krad. Investigating this one exception led to the discovery of the foundry that fabricated the device and provided us insight into the radiation hardness process/mechanism.

II. RADIATION EFFECTS IN MOSFETS AND OXIDES

The oxide layers in CMOS technology are known to be affected by ionizing radiation. As implied, ionizing radiation generates electron/hole pairs in the device. Particularly, if there is an electric field across the oxide of the device the electrons which are the more mobile of the two charges are swept from the oxide leaving the less mobile holes behind. The holes migrate through the oxide until they either recombine with an electron or are immobilized in a trap. This trapped positive charge in the oxide creates an electric field which can affect the behaviour of the device by causing voltage shifts or current leakage. Specifically, in gate oxide the positive charge produces a gate threshold shift which can prematurely turn the device on and taken to extremes leaves the device permanently conducting.

Table 1. Known radiation hard processes used at Cern. Note that the oxide thickness is limited to 7 nm or less

IBM Foundry Oxide Thickness			
Lithography	Process Name	Operating Voltage	Oxide Thickness
			nm
0.25 μm	6SF	2.5	5
		3.3	7
0.13 μm	8RF	1.2 & 1.5	2.2
		2.2 & 3.3	5.2

The magnitude of this radiation effect also depends on the thickness of the oxide (t_{ox}). Quantitatively, the voltage shift/unit dose changes approximately proportionally to $(t_{ox})^2$. However, at thicknesses of about 10 nm or less the change/unit dose decreases rapidly until below some threshold the change is negligible [1].

The CERN microelectronics group has used IBM processes that have been shown to be rad hard [2]. These processes along with the oxide thicknesses used in shown in Table 1.

This apparent immunity is consistent with the theory that the trapped positive charge in the thin oxides is neutralized by electrons tunnelling from the SiO_2/Si interface [3]. This prevents any long term build-up of the positive charge in the oxide. In Figure 1 is shown an example of how this could occur [4]. Two regions are defined.

- 1) The volume where charges would recombine (Tunneling Region) would be approximately 5 nm thick. No stable positive charge would remain.
- 2) Oxide farther than 5 nm from the SiO_2/Si interface would define a 2nd region (Oxide Trap Region) where fixed positive charge would remain and shift the gate threshold voltage.

When the thickness of the Oxide Trap Region decreases to near zero only switching states would remain making the oxide resistant to ionizing radiation. This is consistent with the observations we have made on buck converters and single devices from 2 foundries. However devices from another foundry did not survive.

Our conclusion is that the thin oxide is a necessary condition for the functional immunity of CMOS devices to ionizing radiation. However, the thin oxide is not a sufficient condition as the preparation of the oxide; epi-layer and other properties also contribute to radiation hardness. This parameterization would be for future work when a sufficiently large enough sample of higher voltage rated ($> 12\text{ V}$) CMOS devices with thin oxides are obtained from different sources (e.g. foundries).

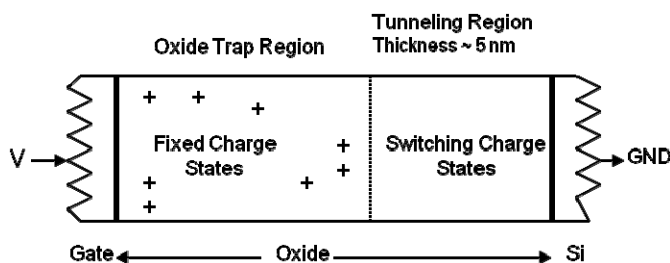


Figure 1: Physical Location of Defects from their Electrical response in CMOS devices;

Some ionizing radiation measurements on LDMOS devices constructed with thin oxides have been made. Some of the results on IHP foundry devices can be found in [5-6]. A more recent result is shown in Figure 2 which shows the ionizing radiation response of a LDMOS FET from another foundry.

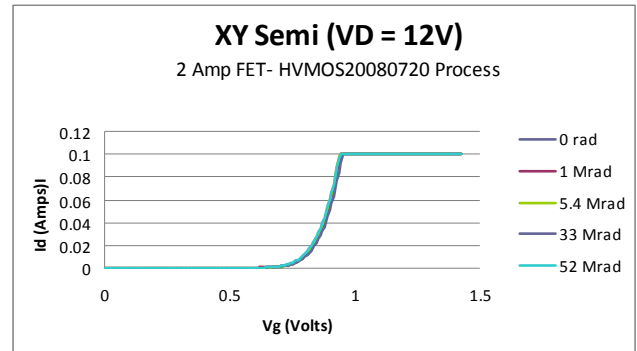


Figure 2: LDMOS N-channel MOSFET constructed with 7nm gate oxide thickness. The device shows exceptional immunity to ionizing radiation effects to the final dose of 52 Mrad.

Table 2 shows a compendium of the radiation measurements made recently with the oxide thicknesses, final dose and state of the device at the end of the test.

Table 2. Compendium of recent radiation measurements made on MOSFETs and Buck Converters

Company	Device	Process	Foundry	Oxide Thickness	Time	Dose before	Observation
		Process Number	Name	Thickness	Seconds	Damage level	Damage Mode
			Country	nm			
IHP	AGC custom	SO2SV/GCD	IHP, Germany	5		53 Mrad	slight damage
XySemi	FET 2 amps	HVMOS20080720	China	7		52 Mrad	in lab damage
XySemi	XP2201	HVMOS20080720	China	7			In Development Synch Buck
XySemi	XP0002	HVMOS20080720	China	7			In Development Synch Buck
XySemi	XP0002		China	12.0	800	44 Mrad	loss of V_{GS} regulation
TI	TPS4600	LMOS 0.35 μm		20	420	23 Mrad	stuck failure
IR	IR3841			9 & 25	220	13 Mrad	loss of V_{GS} regulation
Explosion	EN5305	CMOS 0.25 μm	Donglei HTek, Korea	5	11,500	55 Mrad	Increasing Input Current
Explosion	EN5302	CMOS 0.25 μm	Donglei HTek, Korea	5	2000	111 Mrad	loss of V_{GS} regulation
Explosion	EN5306-F1	SO2SV (IHP)	IHP, Germany	5	22 Days	100 Mrads	In lab damage
Explosion	EN5306-F1	SO2SV (IHP)	IHP, Germany	5	10 Days	48 Mrads	In lab damage

III. PLUG IN CARDS WITH AIR COILS

Yale model 2151 (Figure 3) is designed with two different commercial converters Max8654 and IR3841; the former is monolithic while the IR unit contains three die in a package with optimized top and bottom FETs. The monolithic FETs compromise performance with the controller circuitry requirements.

Figure 3 shows boards with three different air coils that are being developed. The various types are 1) coils embedded in a PCB with 3 Oz copper, 2) copper coils etched from 0.25 mm copper coil and 3) 10 μH solenoid with ferrite rod removed.

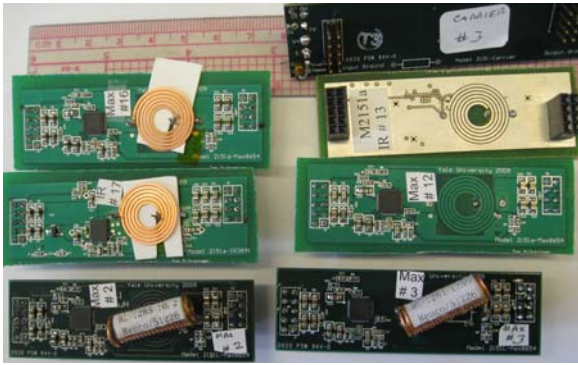


Figure 3: Plug In cards with embedded, copper coil and solenoid air coils. Top right is the Carrier board.

The power in and out are on opposite ends with Kelvin voltage monitoring points on the input connector side. In addition an enable pin can be used to pulse the power on/off. The boards plug in to a carrier board (shown on top right in Figure 3) that can be installed/ wired on the detector under test. This makes it convenient to evaluate the noise studies with different versions of the cards.

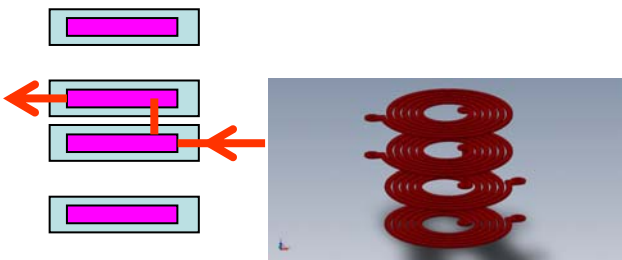


Figure 4: Embedded Coupled Spiral inductor with Inner layers 4 Oz Cu. Outer spiral for shielding

Fig. 4 shows four spirals in a four layer printed circuit board. The outer spirals serve as shield and can be left floating or connected to ground at one end. The inner spirals connected in series have 3 oz copper and are spaced 0.35 mm apart while the outer spirals are much farther separated. This spacing is determined empirically and is a compromise in the desired increased inductance due to mutual inductance coupling between the coil fields. The adverse effect is from the Proximity effect that increases the ac resistance of a coil due to the electromagnetic field choking off a section of coil to current flow in it. This effect is frequency dependent [7-9].

Noise Measurement with Detector

The tests were done in September 2009 at the Liverpool University with a Stave 09 hybrid using ABCN25 readout chips. The detector had a faraday cage made from aluminium foil and the Plug in card was outside but adjacent to it.

The noise measurements with various cards with/ without a clip on common mode choke are shown in the Table 3. For comparison the noise was also measured with readout chips powered by laboratory power supplies. There was no significant difference in noise with various combinations except that the solenoid produced 30% higher noise.

Next a plug card with embedded spiral coil was placed on to top of the hybrid (Fig.5) and a plastic mechanical protection spacer.

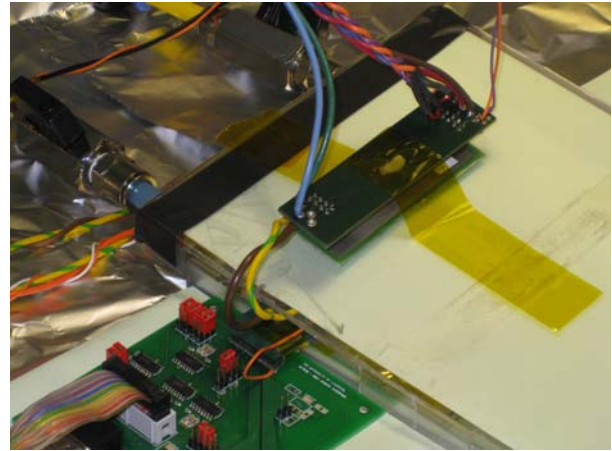


Figure 5: Plug in card on top of readout hybrid. 1 cm above sensor

The latter had a 20 μm Al foil for shielding. A few years ago we determined that this thickness of foil provided sufficient shielding. The embedded coil card was about 1 cm from the silicon sensor. This was the closest that we can place the card. Our conclusions were that the placement of an embedded air coil card 1 cm from sensor had no effect on the noise.

IV. GAN FETS

Other possibilities for radiation hard performance are devices made from III-V technology. One very promising group of candidates for this are High Electron Mobility Transistors (HEMTs) produced in GaN on top of a substrate of sapphire, SiC, or Silicon. Commercial devices are available that operate in a depletion mode (normally on). The gate has significant leakage compared to the oxide in MOSFETs but correspondingly has no possibility of charge trapping causing voltage shifts.

Shown in Figure 6 are the results of irradiating a Nitronex 25015 HEMT with ^{60}Co ionizing radiation. As can be seen the effect is very slight up to the total dose of 17.3 Mrad.

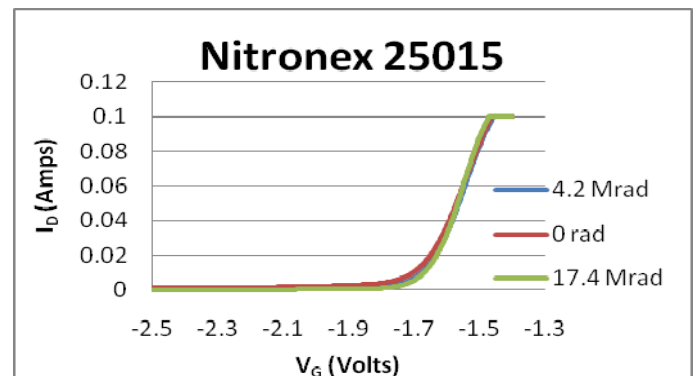


Figure 6: 25015 HEMT irradiated with ^{60}Co gamma radiation

Table 3. Equivalent noise charge of a DC-DC powered hybrid circuit using various buck inductors.

Coil	Board #	Common Mode Choke	Power To DC-DC	Input Noise Electrons rms
Solenoid	Max # 2	No		881
"	"	"		885
Copper Coil	IR # 17	No	Switching	666
"	"	Yes	"	634
"	"	Yes	Linear	664
Embedded	Max 12	No	Linear	686
"	"	Yes	"	641
"	"	Yes	"	648

Three other devices from Nitronex, Eudyna and Cree have been irradiated to doses greater than 25 Mrad (as high as 200 Mrad with protons) with the devices placed in a switching mode during irradiation. In all 3 devices no effect of the ionizing irradiation has been observed except for a small change in drain current during irradiation which reverts when the irradiation is ended. Devices have also been irradiated with neutrons but the measurements are still incomplete.

V. SUMMARY AND FUTURE WORK

The primary goal of this work is to produce a DC-DC buck converter that can be used in the upgraded Atlas Silicon Tracker at the sLHC. It would have to survive a total ionizing radiation dose of 50 Mrad and a displacement damage fluence of $5 \times 10^{14} / \text{cm}^2$ of 1 MeV equivalent neutrons. It would have to operate in a > 2 Tesla magnetic field while providing a 1.2 volt output at several Amperes with a 12 volt or greater input. In 2007 a commercial buck converter (Enpirion) based on a $0.25 \mu\text{m}$ process was found that would survive the ionizing dose requirement although it did not have the input voltage rating. To date this is the only commercial product that has met this requirement. In 2008 the foundry (IHP Microelectronics) that produced the Enpirion converter successfully added a 12 V MOSFET based on a $0.25 \mu\text{m}$ process. This MOSFET also proved to be radiation hard. Since then XYsemi which uses a different foundry than IHP has produced radiation hard MOSFETs on a similar process. No commercial products exist at this time and but the work is ongoing.

In parallel with the above work plug-in power cards with commercial converters are being developed to test upgrade hybrids of the Si Tracker group. Commercial buck converters are used that are unlikely to be radiation hard but will allow testing of the form/fit/function of the buck converters.

Converter chips used for this purpose are the Maxim 8864 and the IR3841 with spiral and spring/solenoid coils.

More recently an investigation has started into the suitability of GaN HEMT devices for these applications. The results to date have been promising. All GaN devices tested to date have survived to 17 Mrad or greater ionizing dose. Displacement damage tests have started and are ongoing.

In the future the efforts described above will be combined into buck converters which will specifically target the electrical, environmental and size requirements of the upgrade Silicon Tracker at the sLHC.

VI. REFERENCES

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