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Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC

A. Macchiolo [a], L. Andricek [b], M. Beimforde [a], H.-G. Moser [b], R. Nisius [a], R.H. Richter [b]

[a] Max-Planck-Institut für Physik, Föhringer Ring 6, D80805, München, Germany
[b] Max-Planck Institut Halbleiterlabor, Otto Hahn Ring 6, D81739, München, Germany

Anna.Macchiolo@mpp.mpg.de

Abstract

We present an R&D activity aiming towards a new detector concept in the framework of the ATLAS pixel detector upgrade exploiting a vertical integration technology developed at the Fraunhofer Institute IZM-Munich. The Solid-Liquid InterDiffusion (SLID) technique is investigated as an alternative to the bump-bonding process. We also investigate the extraction of the signals from the back of the read-out chip through Inter-Chip-Vias to achieve a higher fraction of active area with respect to the present ATLAS pixel module. We will present the layout and the first results obtained with a production of test-structures designed to investigate the SLID interconnection efficiency as a function of different parameters, i.e. the pixel size and pitch, as well as the planarity of the underlying layers.

I. Introduction

An upgrade of the present LHC accelerator, that is designed to reach an instantaneous luminosity of $10^{34}cm^{-2}s^{-1}$, is planned to increase this value by a factor of ten in a two phase process [1].

In Phase 1, an upgrade to a peak luminosity of $(2\text{-}3)\cdot10^{34}$ cm^{-2} s^{-1} is foreseen around the year 2014 without changes to the machine hardware. The Phase 2 upgrade (Super LHC, SLHC) is expected to be realized around 2018 reaching a maximum luminosity of 10^{35} cm^{-2} s^{-1} by modifications to the insertion quadrupoles and changes to the main machine parameters. In this scenario the innermost layers of the ATLAS vertex detector system will have to sustain very high integrated fluences of more than 10^{16} n_{eq} cm^{-2} [2]. The resulting defects in the semiconductor sensors cause higher leakage currents and a reduced charge collection distance. This leads to a higher noise contribution and reduced signals sizes. Thin planar pixel sensors are among the candidate technologies for the replacement of the ATLAS pixel system. At the same applied bias voltage a higher electric field is present across the detector and an increased Charge Collection Efficiency is expected with respect to sensors with a standard thickness of (250-300) µm [3]. Another challenge for the upgraded system is the increased occupancy in the pixel cells due to the higher luminosity. Reducing the pixel size in the inner part of the tracking detectors is a natural choice for decreasing the occupancy and at the same time increasing the spacial resolution. Succeeding the FE-I3 readout chip, the 20.0 × 18.6 mm^2 FE-I4 chip [4] will feature a reduced pixel size of 50 × 250 μm^2 to address these issues for the Phase 1 upgrade and for the outer layers of the ATLAS pixel system at the SLHC. For the innermost pixel layers at the SLHC a still higher rate capability is needed. A possible solution is the development of vertical integrated (3D) electronics, that can lead to an additional reduction of the pixel sizes and hence the cell occupancy. This is because the 3D circuits can lead to a more compact design thanks to multiple tiers. A preliminary version of the FE-I4 chip is already being translated into the 3D technology in a Multi-Project run with Tezzaron-Chartered [5].

A. Vertical Integration for the ATLAS pixel upgrade

The work reported in this paper aims at developing a new detector concept in the framework of the ATLAS Inner Tracker upgrade. In particular, we envisage a demonstrator module composed of pixel sensors, 75 and 150 µm thick, connected to their front-end electronics by the novel Solid–Liquid InterDiffusion (SLID) [6] process developed by the Fraunhofer Institut IZM-Munich. At the moment a chip designed to readout the ATLAS pixel detectors exploiting the 3D integration is not available. As a first step the present ATLAS FE-I3 chip will be used. We explore the SLID interconnection as a possible alternative to the bump-bonding, that resulted to be the main cost driver during the production of the ATLAS pixel modules. We plan to use Inter-Chip-Vias (ICV), a process also developed by IZM, for the extraction of the signals from the ASIC backside. This allows for the design of new four-side buttable devices, without additional space needed for wire bonding. The chip in the demonstrator module will be thinned down to 50 µm.

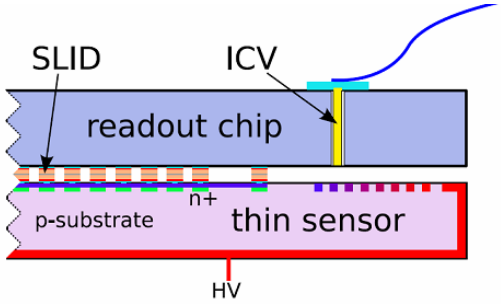

Figure 1: Proposed module layout with thin sensors and the ICV-SLID vertical integration technology.

II. PRODUCTION OF THIN PIXEL SENSORS

The production of n-in-n and n-in-p thin pixel sensors has been completed by the Semiconductor Laboratory (HLL) of the Max-Planck-Institut (MPP). The final active thickness is 75 µm for the n-in-n devices, and 75 or 150 µm for the n-in-p devices. The pixel sensor geometry is such that they can be interfaced to a single FE-I3 chip. The method adopted for the production of these devices, developed at the MPI HLL, allows for the adjustment of the sensor thickness freely down to a thickness of 50 µm [7]. In a first step the backside implantation is performed on the standard wafers. Then the sensor wafers are bonded to a handling substrate and thinned to the desired thickness from the front side. After polishing, the front side processing and passivation are carried out. Finally the handle wafer can be selectively removed by deep anisotropic etching. This procedure allows for frames to be left in the handle wafer to improve the mechanical stability. For the present pixel production the handle wafer has not yet been etched away since it serves as a support during the ASIC interconnection phase. The pre-irradiation characterization has been completed for the p-type wafers [8]. As shown in Fig. 2, very good pixel performances have been achieved, with high breakdown voltages, when compared to the depletion voltages of 40 V for the 75 µm thick detectors and 100 V for the 150 µm thick detectors.

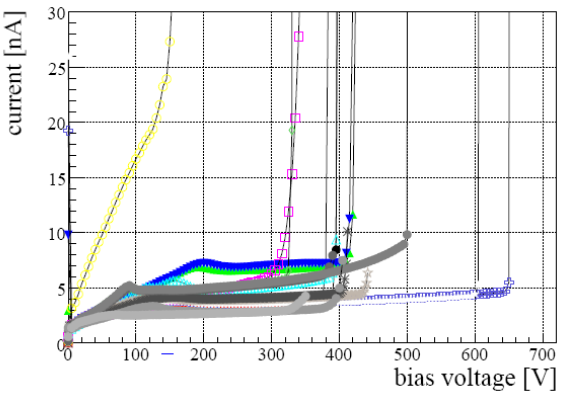

Figure 2: Leakage Current of the p-type pixel sensors. .

III. THE SLID INTERCONNECTION

The ICV-SLID vertical integration technology allows achieving multi-layer semiconductor devices with inter-chip vias (ICV) for vertical signal transport. The SLID process starts with the deposition of a thin layer of TiW on the sensor and electronics surfaces as diffusion barrier for the copper. Then a 5 µm thick Cu layer is applied on both sides, followed by a 3 µm thick Sn layer, which is electroplated only to the sensor. The contact areas where these last processes take place are defined through a mask. Finally the sensor and the ASIC are aligned and contacted at a temperature around 300 °C under a pressure of 5 bar. A Cu_3Sn alloy is formed, that electrically and mechanically connects the two devices. The alloy is stable up to temperatures of 600 °C, allowing the application of the SLID interconnection successively to different tiers. The possible influence of the SLID metal system on the sensor properties has been investigated and no detectable effects have been observed [9].

This technique is a possible alternative to the bump-bonding and, since it consists of less processing steps it has the potential of being cheaper. Moreover the SLID pads can have variable shapes and sizes, adjusted to the sensor geometry and to the requirements on the mechanical stability. A drawack is that reworking, in case of failure, is not feasible, as opposite to bump-bonding.

A. Test production with daisy chains

A test-production with daisy chains has been completed at the MPP. It consists of 6" wafers where both the sensor and chip part have been implemented, mirrored with respect to the horizontal axis. This enables to study the placement precision of the chips and the efficiency of the SLID connection both for a wafer-to-wafer and a chip-to-wafer approach, while using a single set of masks. Different pad sizes and pitches have been implemented to explore the limits of the technology. Aplanarities of the silicon surfaces have been realized by introducing steps in the SiO_2 layer (100 nm) or the aluminum layer (1 µm) below the SLID interconnection pad. Figure 3 depicts the schematics of the daisy chains.

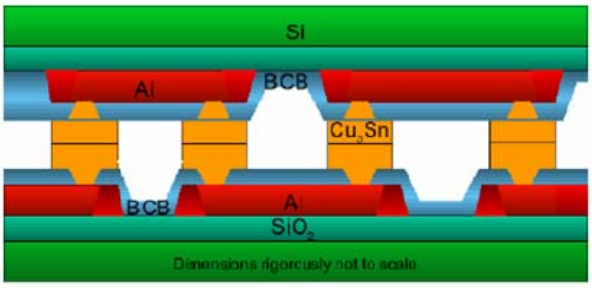

Figure 3: Schematics of the daisy chain design for the SLID testing.

The wafer-to-wafer process has been succesfully achieved yielding an inefficiency of less than 10^{-3} for most of the tested chains. Table 1 summarizes the results of all the daisy chain measurements. The resistance per pad varies between 0.25 and 1.5 Ω in the different chains. The sizeable statistical uncertainties are not due to the limited number of measured connections but to the spread observed among different chains with the same geometry.

In addition, measurements of the misalignment resulted for the wafer-to-wafer interconnection in an average value of less than 5 µm for the first of the two packages tested, and (5-10) µm for the second one. In this kind of assembly the chip wafer is diced after it has been attached to the handle wafer used for the interconnection. A varying misalignment for the different structures present in a

package can arise from the fact that the epoxy-based adhesive used to attach the chips to the handle wafer softens at the temperature needed for SLID before the Cu_3Sn alloy is completely formed.

Observations performed with an infrared microscope revealed in some of the chains with larger pad size (80x80 μm^2) an outflow of the tin layer creating a short with the neighbouring pads. No problems were visible for the chains with smaller pad sizes and in the structures where we have implemented the pad geometry (27x60 μm^2) needed for the interconnection of the ATLAS pixels (Figure 4). The need to optimize the amount of tin according to the pad size and the applied pressure leads to the requirement of limiting the number of different chip geometries in the same package.

A chip-to-wafer assembly using these daisy chain structures is on-going. In this case the chip structures are diced before being placed onto the handle wafer. This will be the method adopted for the face-to-face connection of the FE-I3 chip to the thin pixel sensors.

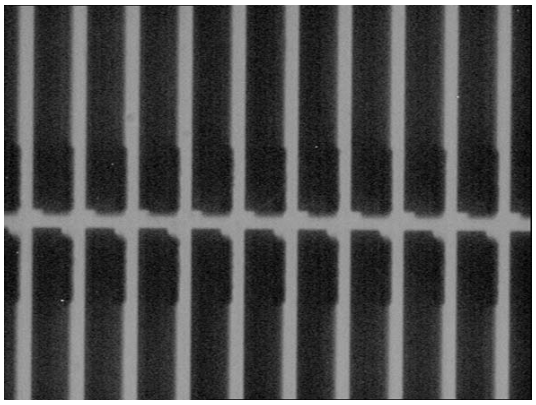

Figure 4: Infrared image of the interconnected daisy chain of the ATLAS pixel geometry. The darker rectangles correspond to the SLID pads.

IV. The Inter Chip Vias

The 3D-interconnection technology also offers the possibility of extracting the signals from the backside of the chip by using the Inter Chip Vias (ICV) process. The ICV technique is being applied for the read-out of the MPP thin pixel sensors connected to the FE-I3 chips.

The foreseen process flow for the FE-I3 starts with the etching of the vias on the chip pads originally designed for the wire bonding, after having removed the last aluminum layer. The vias cross-section is 3x10 μm^2, and the initial depth 60 µm. For lateral via isolation a Chemical Vapour Deposition (CVD) of silicon dioxide is applied and then ICVs are metalized with a tungsten filling.

After this step the electroplating is performed on the front side that is finally passivated. The chip wafer is then bonded to a handle wafer and thinned down from the backside to 50 µm to expose the vias. An isolation layer is deposited on the backside and the metallization needed to create the new contact pads is applied.

The design of the sensor-chip interconnection is at the moment being finalized with the determination of the optimal placement of the SLID pads and the vias.

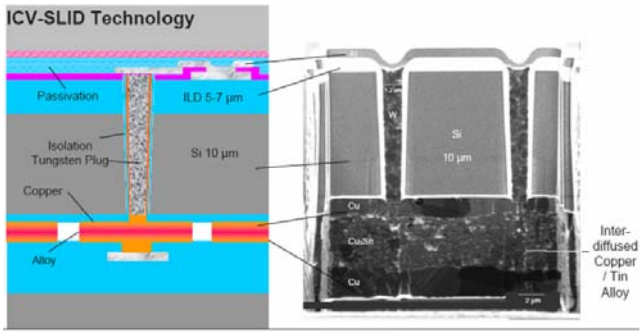

Figure 5: Schematic view of the Inter Chip Vias

V. Conclusions

In the R&D effort towards thin pixel sensors and the ICV-SLID vertical integration, a first production of thin pixel sensors and SLID test structures has been completed. A high efficiency of the SLID interconnection was measured independently of the chosen pad sizes. This activity will proceed with the SLID interconnection of thin pixel structures to the ATLAS FE-I3 chip and the extraction of the signals from the backside of the chip.

VI. References

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Pad Sizes [μm^2]	Pitch [μm]	Aplanarity [μm]	Connection measured	Inefficiency [10^{-3}]
30x30	60	-	8288	<0.36
80x80	115	-	1120	<2.7
80x80	100	-	1288	<2.3
27x60	50,400	-	24160	0.5±0.1
30x30	60	0.1	5400	1.0±0.4
30x30	60	1.0	5400	0.4±0.3

Table 1: Geometrical parameters and performances of various SLID connection options