Design of High Dynamic Range Digital to Analog Converters for the Calibration of the CALICE Si-W Ecal readout electronics

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Abstract

The ILC ECAL front-end chip will integrate many functions of the readout electronics including a DAC dedicated to calibration. We present two versions of DAC with respectively 12 and 14 bits, designed in a CMOS 0.35µm process. Both are based on segmented arrays of switched capacitors controlled by a Dynamic Element Matching (DEM) algorithm. A full differential architecture is used, and the amplifiers can be turned into a standby mode reducing the power dissipation. The 12 bit DAC features an INL lower than 0.3 LSB at 5MHz, and dissipates less than 7mW. The 14 bit DAC is an improved version of the 12 bit design.

I. INTRODUCTION

The increasing number of electronics channels involved in present and future high energy physics detectors leads to integrate in the same chip many different functions of the readout electronics: preamplifier, shaper, ADC. In the International Linear Collider (ILC) project, the design of the front-end electronics for the electromagnetic calorimeter (ECAL) is even more challenging. Due to mechanical constraints, no package will be used for the front-end chip and the dies have to be embedded within the printed circuit board. Consequently the electronics has to be fully integrated and no discrete components can be used. This multi-channel chip also requires a high dynamic Digital to Analog Converter (DAC) dedicated to its calibration [1]. Since calibration process can generally be carried out at intermediate frequency (few ksp/s to few Msp/s), the key issues for such a DAC are the integral non linearity (INL) and the power consumption. Switched Capacitor DACs (SCDAC) are well suited to meet these requirements. The linearity of a design implemented in CMOS process is limited by the matching errors of the analogue components. For more than 12 bits the required matching is difficult to obtain and linearization techniques have to be used. High resolution multi-bit delta sigma converters commonly use the Dynamic Element Matching (DEM) method to cancel the matching errors. The DEM allows such DACs to generate pure sinusoidal waveforms by turning the harmonic distortion into noise, this noise is then reduced by the converter's low pass filter [2]. When used in a calibration process the DAC has to provide a sequence of DC values, each value corresponding to a calibration point. In this case the DEM can be effective if several samples are accumulated for each calibration point. The response of the chip under calibration will be given by the mean value of the resulting distribution. A 12 bit and a 14 bit SCDACs have been designed using a CMOS 0.35µm process. This paper presents, for each chip, the different steps of the design including the choice of the topology, the DAC modelling and simulation, the layout implementation and finally the test of the chip.

II. DESIGN OF A 5MSPS 12 BIT DAC

This first prototype was designed to provide a MEMS sensor with pure sinusoidal waveforms. Since the sampling rate is higher than the Nyquist rate, the DEM should improve the INL and the THD of the DAC.

A. DAC topology

1) Capacitor network:

A linearization based on the DEM implies the DAC to be designed using equally weighted unitary converters (thermometer DAC). A 12 bit design would lead to implement 4095 converters, inducing some difficulties. An alternative scheme is to use a segmented array of capacitors. An example of such a scheme is shown in Figure 1. This 12 bit network is divided into two 6 bit arrays (MSB and LSB) connected together through a segmentation capacitor C_s. Each sub array comprises 63 capacitors on which the DEM can be applied. The network is terminated by a unitary capacitor and the overall capacitance is equal to 64C. Compared to a "full thermometer" topology, this scheme is much easier to implement, but it has to be noticed that the DEM will have no effect on C_s matching error.

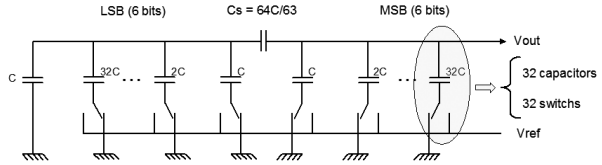

Figure 1: 12 bit segmented array of switched capacitors

2) Operational trans-impedance amplifier:

The other critical sub-circuit of the DAC is the Operational Trans-impedance Amplifier (OTA) used to process the signal provided by the capacitor network. This present work inherits the OTA designed for a 12 bit high speed pipeline ADC [3]. This low power differential OTA, based on a folded cascode architecture, includes four auxiliary amplifiers to increase the open loop gain. Consequently, this 90 dB gain insures the linearity required by a design up to 16 bits. Moreover it can be powered ON/OFF by a dedicated

circuit reducing its power dissipation to a ratio better than 1/1000. This capability is particularly interesting since the calibration process is supposed to represent a small amount of the chip operating time.

3) Direct Charge Transfer:

The OTA is connected to the capacitor array using the Direct Charge Transfer mode (DCT). The DCT principle is illustrated in the Figure 2 for a single-ended amplifier.

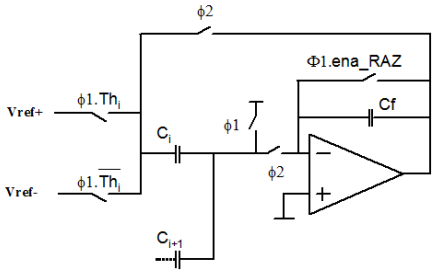

Figure 2: Direct Charge Transfer

The signals ϕ1 and ϕ2 are two non recovering clocks derived from the chip main clock. The signal labelled Th_i is provided by the thermometer encoder and controls the capacitor C_i. During ϕ1 the capacitor C_i is connected to Vref+ or Vref- depending on the state of the Th_i signal. Then, during ϕ2 all the capacitors of the array are connected in parallel with the feedback capacitor C_f to perform charge sharing. The C_f capacitor can be discharged or not, during ϕ1, depending on the state of the signal labelled ena_RAZ. The charge sharing architecture presents two important advantages. At first, the OTA does not have to charge the feedback capacitor C_f and its power consumption can be maintained low even for large values of C_f. Moreover, if the signal ena_RAZ is not activated the charge sharing also acts as a first order low pass filter that reduces the noise induced by the DEM. The filter transfer function and its cut off frequency are given by the following expressions where f_e is the frequency of the DAC main clock.

$$H(z) = \frac{1}{1 + b - bz^{-1}} \qquad (1)$$

$$b = \frac{C_f}{\sum C_i} = 1 \quad \Rightarrow \quad H(z) = \frac{1}{2 - z^{-1}}$$

$$f_{-3dB} = \frac{\ln 2}{2\pi . T_e} \approx 0.11 f_e \qquad (2)$$

4) Differential implementation:

The differential implementation of the DAC is shown in Figure 3. During ϕ1 the network is not connected to the amplifier and stores a charge proportional to the DAC input code. The charge sharing is performed during ϕ2. Another interesting property of this topology is its small sensitivity to the parasitic capacitors. The net labelled Sum_MSB should be very sensitive to capacitive substrate coupling but the OTA open loop gain maintains a DC voltage equal to VMC (OTA Common Mode) on this net. The net labelled Sum_LSB is also sensitive but since it is located on the LSB side of the network, this sensitivity is small. However the network capacitors have to be connected in the right way in order to minimize the substrate coupling on this net. The other parasitic elements are in parallel with each capacitor in the two arrays. They are due to the capacitive couplings between the metallic interconnections and the capacitors themselves, inducing matching errors. The effect of these errors will be turned into noise by the DEM algorithm. Nevertheless, during the layout design, cares are needed to minimize these mismatches in order to reduce the overall noise of the chip. Finally, the sensitive component is the C_s capacitor which is not included in the DEM. This capacitor must match the MSB array mean value.

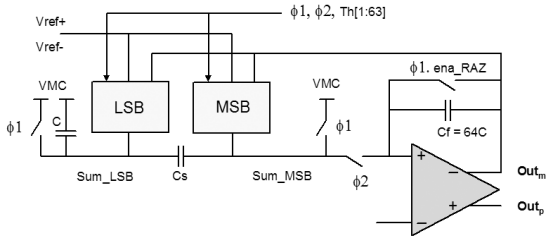

Figure 3: Differential implementation of the 12 bit DAC

5) DEM algorithms:

These algorithms aim to use each unitary converter at the same rate in order to average the matching errors. They can be either stochastic or deterministic. Data Weighed Averaging (DWA) is a deterministic algorithm entirely controlled by the data sequence [4] [5]. It rotates the elements with the maximum possible rate. The average of the errors converges to zero quickly. The Figure 4 shows how this algorithm rotates the elements of a 3 bit DAC. For each sample, the selected sub-array starts at the first previously unused position. This algorithm exhibits two other advantages. Whereas stochastic algorithms induce a white noise, DWA shifts the noise to higher frequencies. Moreover it can be directly describe in VHDL.

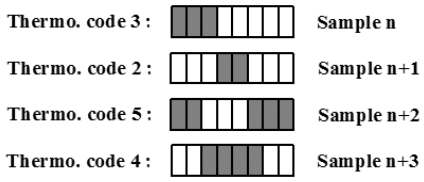

Figure 4: Data Weighted Averaging algorithm

B. DAC modelling and simulation

The DEM efficiency can be demonstrated using either a statistical approach or a spectral analysis. In both cases a large number of samples have to be accumulated. Based on a model of the DAC, the DEM efficiency can be evaluated using high level simulation. The test bench of the chip is based on Labview, this software was also chosen for the simulation. In such a way, data acquisition, simulation and data analysis can be carried out with the same environment. The differential implementation of the capacitor network is shown in Figure 5. The output voltage Vout as a function of the input code is given by expression (3) in the case of ideal capacitors (l and m are the LSB and MSB input code).

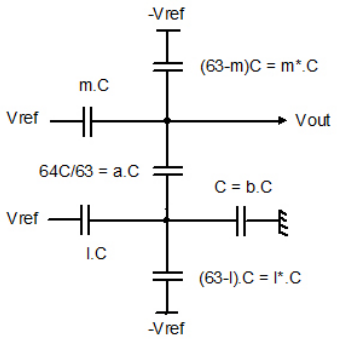

Figure 5: Differential implementation of the 12 bit network

$$Vout = \frac{1}{64}\left(\frac{2l-63}{64} + 2m - 63\right)Vref \qquad (3)$$

For the MSB side of the network, the matching errors can be introduced assuming that a mC (respectively m*C) capacitor is connected to Vref (-Vref). In this case expression (3) becomes expression (4).

$$Vout = \frac{B}{A}Vref = f(m,l,a,b) \qquad (4)$$

$$A = \frac{m + m^* + b}{b} - \frac{b}{l + l^* + a + b} \qquad B = \frac{2l-63}{l + l^* + a + b} + \frac{2m-63}{b}$$

$$m = \sum_{1}^{m} C_i \qquad m^* = \sum_{m+1}^{63} C_i$$

The DEM algorithm has to reorder the arrays before m and m* are calculated. The matching errors of the segmentation and termination capacitors are introduced by the parameters a and b. The block diagram of the Labview program is shown in Figure 6. The pattern generator provides either a sinusoidal waveform or a sequence of DC values. The block labelled DEM & Σ processes the MSB and LSB arrays using a DEM algorithm. The converter's low pass filter (LPF block) can be activated by the ena_RAZ signal. The testing board is equipped with a 16 bit ADC that digitizes the DAC output voltage. The block Q16 performs a 16 bit quantization of the simulated values. Finally, simulated and measured data are processed in the same way by the Data Analysis block. It calculates the DAC non linearity (INL, THD) and the DAC noise (SNR, RMS noise). This block also extracts the matching errors of the capacitors for the two input arrays.

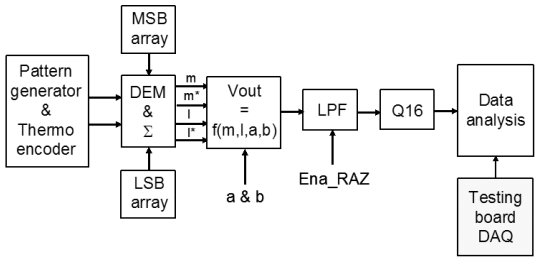

Figure 6: High level simulation block diagram

Electrical simulations have been carried out to study the effect of the parasitic capacitors, for the switches sizing and to check the overall design.

C. Layout considerations

The layout of the MSB network is shown in Figure 7. It includes 63 unitary capacitors (0 to 62) and the segmentation capacitor C_s arranged in a 4x16 array. It also includes 63 switches, their control logic and 2 non recovering clock generators. This layout is not a common centroid design and each unitary element consists in a single 500fF capacitor. The matching errors due to the metallic interconnections (from Analog Extracted View) are lower than 0.1%. The DAC layout is shown in Figure 8. The size of the active part (without pads) is 1.6mm^2. This Figure shows that the low sensitivity to substrate coupling is a critical issue of the design. The connection between the MSBn array and the OTA is about 1 mm long, inducing a large parasitic capacitor.

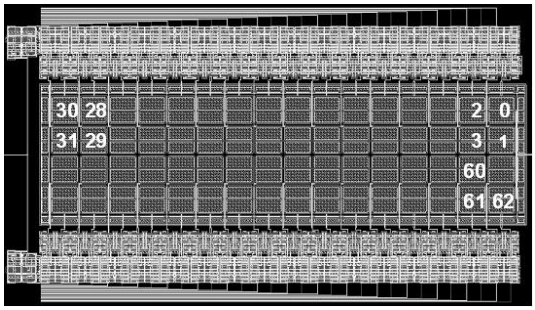

Figure 7: Layout of the MSB array

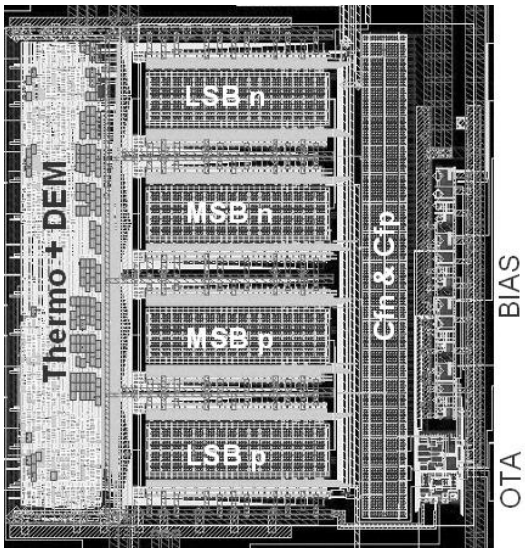

Figure 8: Layout of the active part of the DAC

D. Simulation and test results

The matching errors in the MSB array were recorded for the 15 tested chips. These errors range from 0.8% for the best DAC, to 1.8% for the worst one. The distribution of the errors over the array (normalized to C0) is shown in Figure 9. All the DACs exhibit the same distribution shape. The larger values are located at the centre of the array. The gradient is not constant over the array, so a common centroid design would not have improved the matching. The reliability of the high level simulations can be checked when the matching errors are injected in the simulator. The simulated and measured INL and RMS noise are shown in Figure 10 when

the DEM is not activated. The INL and the RMS noise, when the DEM is activated, are shown in Figure 11. The DEM improves the INL by a factor of 8 (3 bits). The remaining INL (0.3 LSB) is mainly due to the C_s capacitor which does not perfectly match the MSB array mean value. The 70µV RMS noise measured without DEM is dominated by the testing board noise. Without external low pass filter, the DEM induces a 500µV RMS noise (1 LSB).

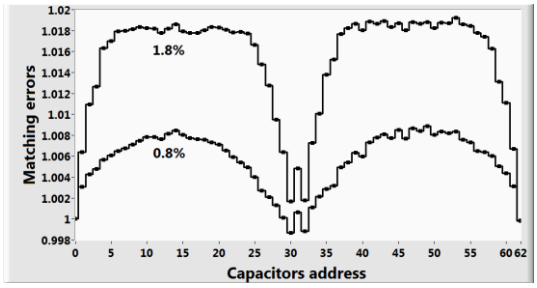

Figure 9: Matching errors in the MSB array

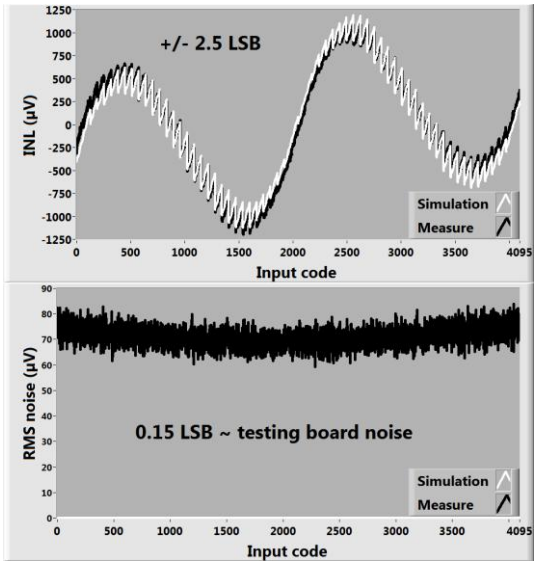

Figure 10: INL and RMS noise without DEM

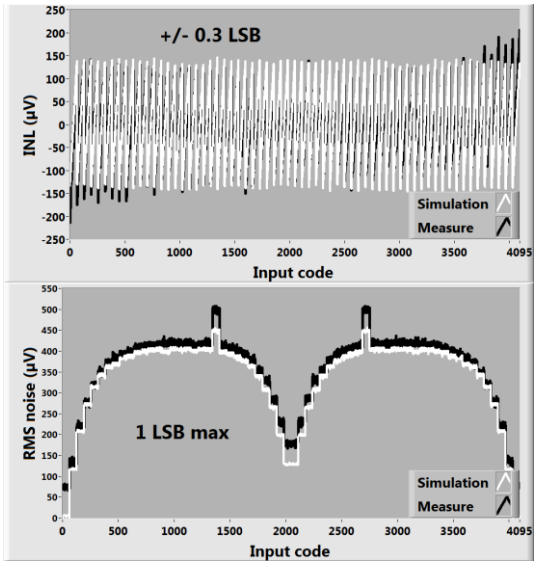

Figure 11: INL and RMS noise with DEM

E. Conclusion

Whereas the matching errors are larger than expected with a 0.35µm process, the 12 bit DAC meets the requirements of the MEMS sensor application for the INL point of view. Since the output voltage will be processed by an external low pass filter, the noise was specified in different frequency bands. Spectral analyses show that the DAC also satisfies these in-band noise constraints. The DEM efficiency was demonstrated with this first prototype and higher resolutions can be foreseen (14 bits). The high level simulation was also validated and appears to be a fast and reliable tool that dramatically reduces the amount of time required for the design.

III. DESIGN OF 5MSPS 14 BIT DAC

This section presents the design and the test results of a 14 bit SCDAC dedicated to the CALICE ECAL FEE calibration. This chip was designed using the OTA and the DEM algorithm implemented in the 12 bit DAC. The DAC modelling and simulation were carried out in the same way.

A. Block diagram

A 14 bit design segmented into two sub-arrays would lead to implement at least 127 capacitors in an array. The chip area, the overall capacitance and probably the matching errors would be dramatically increased. Consequently this 14 bit DAC relies on a 3 segment network. In such a case the intermediate segment (ISB) is very sensitive to substrate coupling. A solution to overcome this difficulty is to use a second OTA. The block diagram of the 14 bit DAC is shown in Figure 12. The MSB, ISB and LSB arrays contain respectively 31 (5 bits), 31 (5 bits) and 15 (4 bits) capacitors. The simulation shows that the matching for Cf1, Cs2 and MSB array mean value must be better than 0.3%. For the layout point of view, these 3 components are located in the same 64 capacitor array. The ISB-LSB network is located in another 48 capacitor array. Taking into account the poor matching obtains for the 12 bit DAC, a trimming capability was implemented for the Cf1 capacitor. A 0.1C trimming step allows the 0.3% matching constraint to be reached.

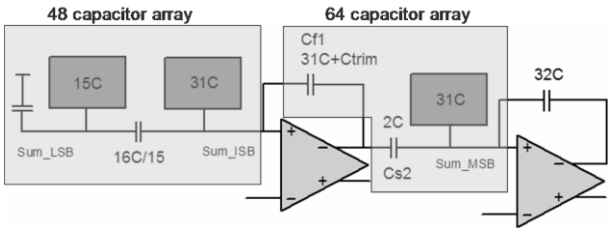

Figure 12: 14 bit DAC block diagram

B. Layout

The layout of a capacitor array is similar to the layout used in the 12 bit DAC. The size of the dummy capacitors that surround each array has been increased. The layout of the active part of the DAC is shown in Figure 13 (area=1.45mm^2). Its topology is also similar to the topology of the 12 bit DAC layout.

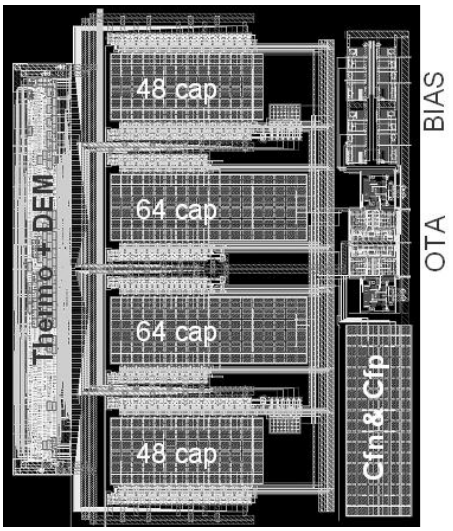

Figure 13: Layout of the active part of the 14 bit DAC

C. *Simulation and test results*

The matching errors in the MSB array for the 9 tested chips range from 0.25% to 0.4%. No particular shape appears in the distribution over the 31 capacitor sub-array. The mismatch is entirely due the difference between inner and outer rows in the 4x8 sub-array. The matching errors due to metallic interconnections are lower than 0.1% (from Analog Extracted View). The INL and RMS noise without DEM (respectively with DEM) are shown in Figure 14 (Figure 15). Since the capacitors matching is better for this DAC, the DEM improves the INL by a factor of 2 (1 bit) and induces a small effect on the noise. This noise is dominated by the testing board contribution (about 50µV). The remaining INL (0.5 LSB) is mainly due to the 0.1C trimming step. The optimal trimming value is the same for the 9 chips. The same value is also found with the simulation. The trimming values that surround the optimal one also lead to a 14 bit resolution:

Copt : THD = -95dB

Copt+/-1: THD = -89dB

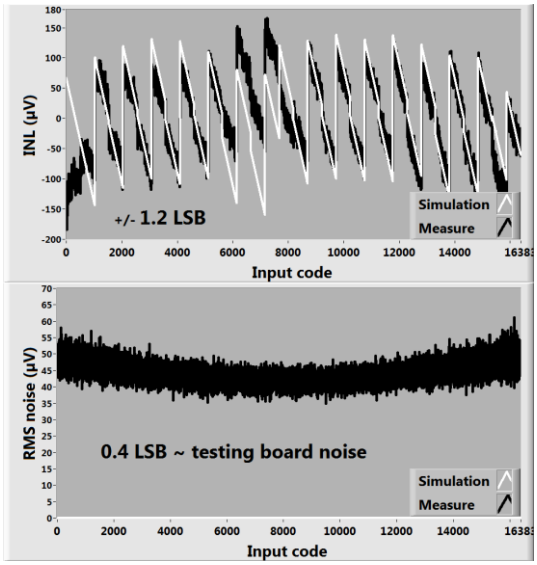

Figure 14: INL and RMS noise without DEM

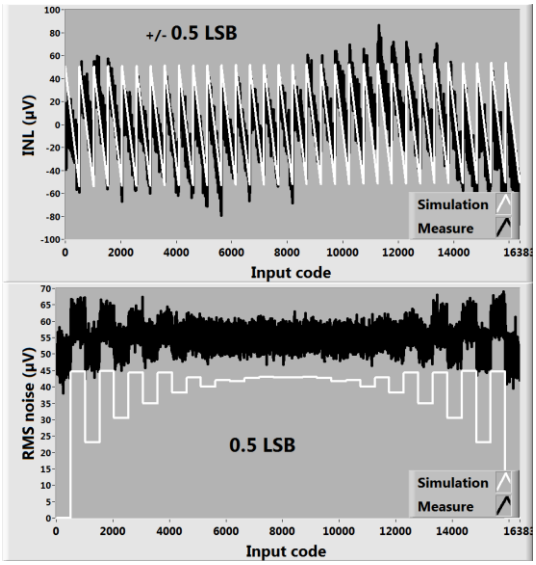

Figure 15: INL and RMS noise with DEM

D. *Conclusion and perspectives*

The matching errors are much smaller in the 14 bit DAC compared to the 12 bit DAC, whereas the capacitor arrays are similar (larger dummies in the 14 bit DAC). The spread of the oxide thickness for the 12 bit DAC run is twice the spread for the 14 bit DAC run and is the worst among the chips submitted by LPSC in 2008/2009 with the same process.

For this prototyping run, the DAC satisfies the constraints of a 14 bit design even without the trimming capability (the optimal trimming value can be predicted in simulation). But theses results may vary from a run to another depending on the process reliability. The DAC aims to be included in the ECAL Front End Chip (SKIROC chip) and consequently its trimming process may induce some constraints to the other parts of the FEE electronics.

A self trimmed version of the 14 bit DAC will be submitted in 2010.

IV. REFERENCES

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