HARDROC, Readout chip of the Digital Hadronic Calorimeter of ILC

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Abstract

HARDROC (HAdronic Rpc Detector ReadOut Chip) [1] is the very front end chip designed for the readout of the RPC or Micromegas foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider.

The very fine granularity of the ILC hadronic calorimeters (1cm^2 pads) implies a huge number of electronics channels (4 10^5 /m^3) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption to 10 µW per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of data acquisition for 199 ms of dead time).

HARDROC readout is a semi-digital readout with three thresholds which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

The overall performance of HARDROC will be described with detailed measurements of all the characteristics. Hundreds of chips have indeed been produced and tested before being mounted on printed boards developed for the readout of large scale (1m^2) RPC and Micromegas prototypes. These prototypes have been tested with cosmics and also in testbeam at CERN in 2008 and 2009 to evaluate the performance of different kinds of GRPCs and to validate the semi-digital electronics readout system in beam conditions.

I. REQUIREMENTS

A. "Imaging calorimetry" at ILC

Imaging calorimetry consists of reconstructing each particle individually using the Particle Flow Algorithm (PFA). The calorimeters have to be highly granular and segmented.

To address efficiently the R&D developments for calorimeters, the CALICE collaboration [2] has been created in 2003. This collaboration gathers around 280 physicists and engineers, 11 countries and 42 labs. CALICE has chosen to separate 2 axes of R&D. It was first decided to build "physics prototypes" in order to study the PFA, validate the simulation and check the performance of the detectors in test beam. The Electromagnetic Calorimeter (ECAL) made of W-SI and the Analog Hardronic Calorimeter (AHCAL) made of scintillating tiles readout by Si PM have been tested in testbeam at CERN, DESY and FERMILAB since 2003 up to last year, providing good physics data.

The CALICE collaboration then decided to move to large scale "technological prototypes" funded by the EUDET European program [3]. The aim of these prototypes is to study the feasibility of large scale, industrializable modules.

B. Electronics requirements

Electronics requirements are very stringent. Hundred millions of large dynamic range channels have to be read out: on chip zero suppress and auto trigger on ½ MIP or on few fC must be performed with ultra low power: < 25µW/channel.

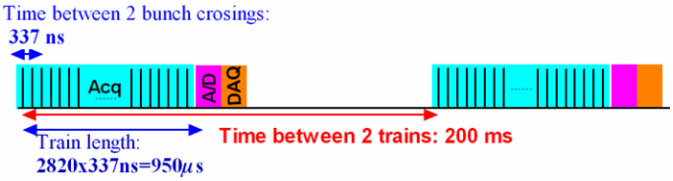

Figure 1: ILC bunch pattern

Moreover for compactness, chips have to be embedded inside the detector without any external circuitry.

To minimize the data lines and the power consumption, the readout architecture [4] is common to all the calorimeters and based on a daisy chain using a token ring mode as shown in Figure 2. This readout matches the ILC beam shown in Figure 1.

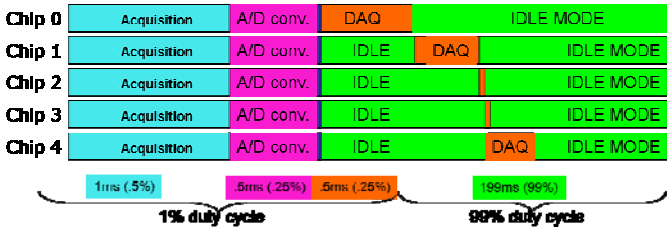

Figure 2: Common readout architecture

C. DHCAL, Digital Hadronic Calorimeter

There are 2 options for the ILC hadronic calorimeter. The conservative analog option (AHCAL) using an analog readout and the Digital option (DHCAL) well dedicated to the PFA and

the high granularity of the detector and which allows a "semi-digital" readout.

D. *Technological prototype*

The absorbers are made of 40 steel plates of 20 mm (~1X0). As for the active medium, 2 options are also studied: Gaseous Resistive Plate Chambers or GRPC [5] and Micromegas [6].

In both cases, the granularity is high (1x1 cm^2) as well as the segmentation (5 10^7 channels for the entire HCAL).

II. HARDROC

HARDROC is the name of the chip designed in SiGe 0.35µm technology to readout the DHCAL. There have been 2 versions of this chip (Hardroc1 and 2). The main difference between these 2 versions is the package which is a plastic thin 160 pins package for Hradroc2 (Figure 3), more suitable to be embedded inside the detector.

Figure 3: TQPF160 package

The HARDROC readout is a semi-digital readout with two or three thresholds which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

The 64 channels of HARDROC2 (Figure 4) are made of:

- Fast low impedance preamplifier with a variable gain over 8 bits per channel
- A variable slow shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC, only used for diagnostic
- 3 variable gain fast shapers followed by 3 low offset discriminators to auto trig down to 10 fC up to 10pC. The thresholds are in a ratio 1-10-100 for better physics performance of the semi digital and are set by 3 internal 10 bit- DACs. The 3 discri outputs are encoded in 2 bits
- A 128 deep digital memory to store the 2*64 encoded discriminator outputs and bunch crossing identification coded over a 24 bits counter.
- Power pulsing and integration of a POD (Power On Digital) module for the 5MHz and 40 Mhz clocks management during the readout [4], to reach 10µW/channel

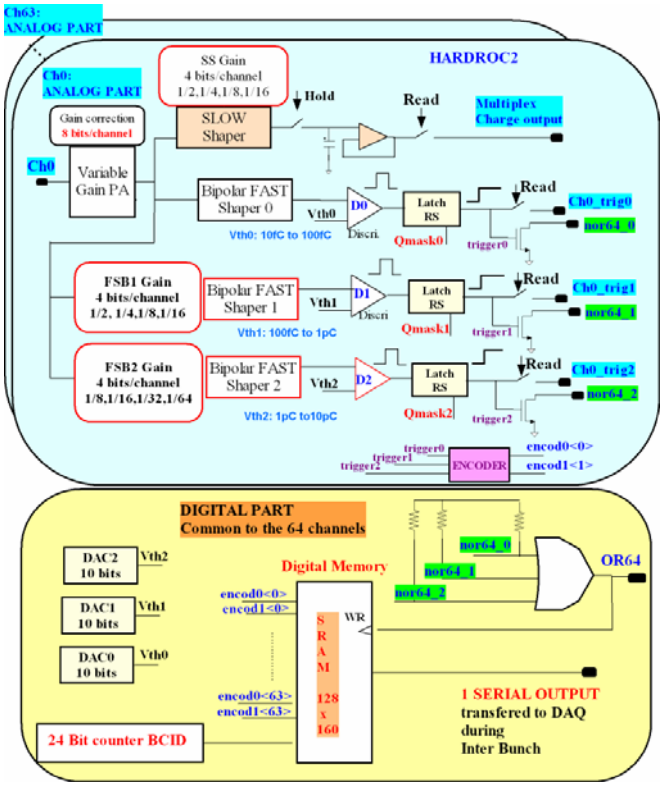

Figure 4: Simplified schematics

872 Slow Control registers with default configuration are integrated to set the required configuration.

III. MEASUREMENTS

Measurements have been performed using a test board without any decoupling capacitors on bias and reference voltages as they slow down the power pulsing.

A. *Trigger path*

There are 3 variable CRRC fast shapers. The network feedback of each preamp can be changed independently thanks to the SC parameters. The peaking time is ≈ 20-25 ns.

The gain of FSB1 and 2 (Figure 5) can be varied thanks to a 4 bits current mirror gain. FSB0 is dedicated for input charges varying from 10fC up to a few hundreds of fC, FSB1 for input charges from 100fC up to 1pC, and FSB2 for input charges from 1 pC up to 30pC.

The gain of FSB0 is 2mV/fC with the typical Slow Control parameters selected as Rf=100K, Cf=100fF and Gain_preamp=128. This can be varied by a factor of 10 thanks to the Slow Control parameters.

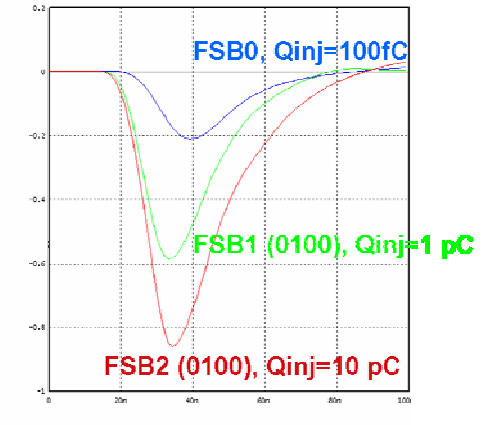

Figure 5: Fsb0,1 and 2 waveforms

The threshold of each discriminator is set by a 10 bit-DAC. The residuals to a linear fit are within ±5 mV over a 2.2V dynamic range (Figure 6). The slope is 2.1mV/DAC unit which corresponds typically to 1fC/DAC unit for FSB0.

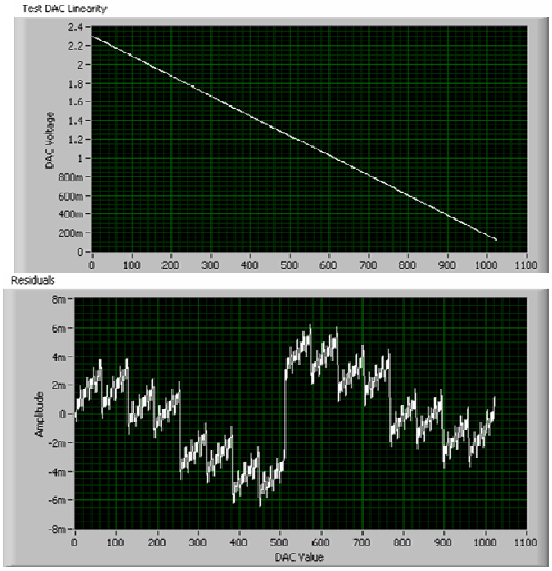

Figure 6: 10 bit-DAC linearity

B. *Trigger efficiency measurements:*

The Figure 7 displays trigger efficiency measurements performed on FSB0 when no signal is injected (pedestal measurements) and when 100 fC are injected. The 10% dispersion between the 64 channels is explained by the mismatch of the current mirrors of the variable gain preamp.

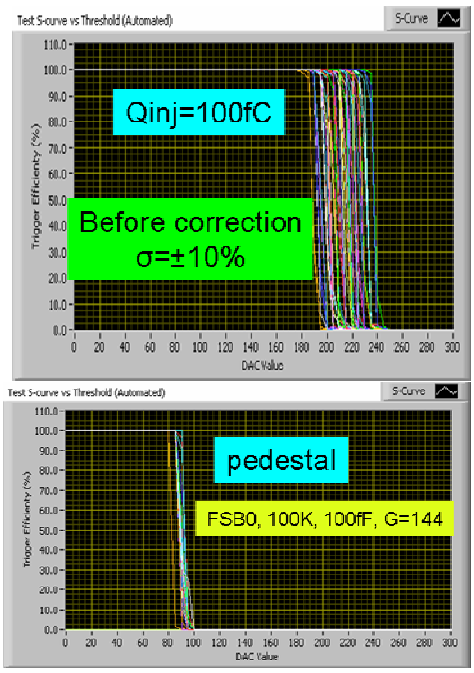

Figure 7: Scurves measurements on FSB0

This non uniformity can be corrected by adjusting the gain preamp for each channel. This gain adjustment is performed over 8 bits allowing a 1.5 % adjustment. The Figure 8 exhibits trigger efficiency measurements after gain correction and for small injected charge. The dispersion is within 1.5% after correction. This plot also shows that each channel of hardroc can easily trigger on 10fC.

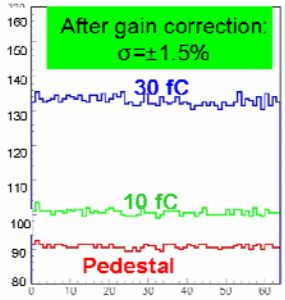

Figure 8: Uniformity after gain correction

Figure 9 which displays the threshold as a function of the input injected charge shows that each channel can also auto trigger down to 4fC which corresponds to the 5σ noise limit.

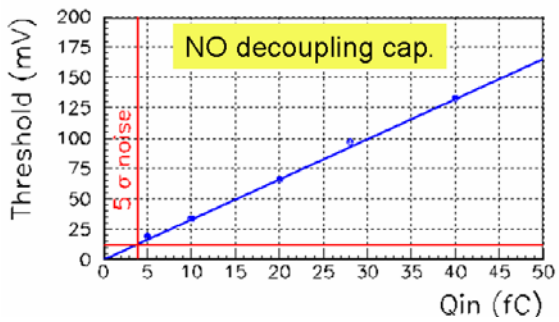

Figure 9: 5σ noise limit

C. *Analog and digital crosstalk*

The analog Xtalk has been measured (Figure 10). This 1% crosstalk is well differentiated and it has been checked that there is no long distance Xtalk.

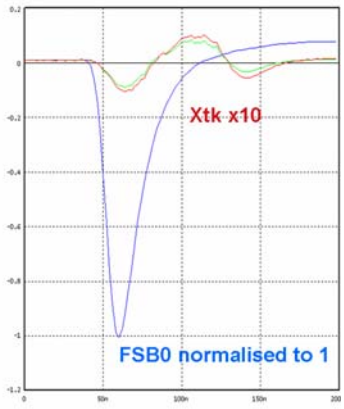

Figure 10: Crosstalk measurement

The discriminator couples to the inputs through the ground or substrate (Figure 11). It corresponds to 8mV or 3fC, which is smaller than the noise (5fC).

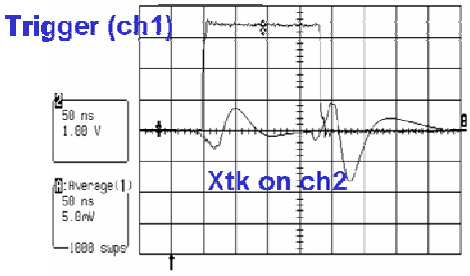

Figure 11: Discriminator coupling

D. *Power consumption*

The maximum available power is 10µW/channel, which corresponds to 180µA for the entire chip. The ASIC is power pulsed to achieve this requirement. All the bias and reference voltages are switched OFF during the interbunch of the ILC beam. The static power consumption of the chip is 100 mW ie 1.5mW/ch and so 7.5µW/ ch with a 0.5%beam duty cycle.

There are 3 independent signals of power-on: Analog, Digital and DAC. Each stage can be forced by slow control, overruling the power on pulse.

The "awake" time has been measured on the analog part and on the DAC part. It takes 2µs for the analog part to be operational and provide a discriminator output and 25µs for DAC part (Figure 12) to reach its nominal value within a few mV. The DAC is slower to settle as it is filtered internally to minimize its noise and inter channel coupling.

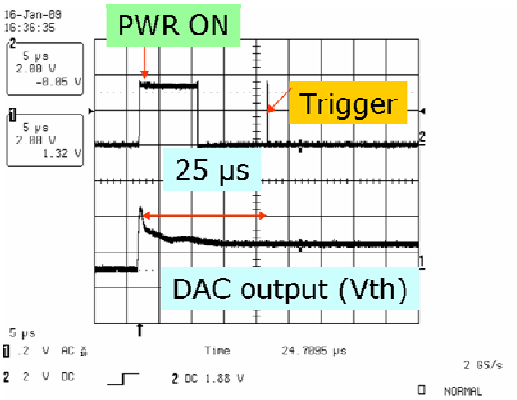

Figure 12: Crosstalk measurement

IV. TEST BEAM MEASUREMENTS

A. *Small prototypes*

8x32cm^2 PCBs hosting four HARDROC (Figure 13) have been designed by IPNL Lyon and LAPP Annecy to study the signal connection between the different chips before extracting it through a USB device. The PCB boards have been associated to both RPC and µMEGAS detectors in order to validate the whole concept (semi digital readout, daisy chain, stability, efficiency) through exposure first to cosmics and then to beam test at CERN.

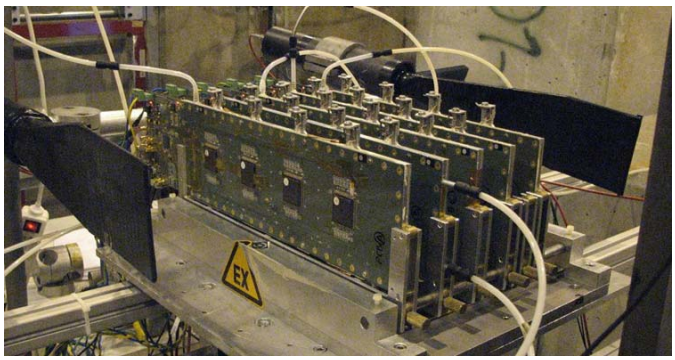

Figure 13: 5 RPC plans of 32x8 cm^2 at CERN

The RPC detector shown in Figure 13 has been used in test beam at CERN in 2008 and 2009. It was the first time that the readout could be tested in real conditions and good data have been obtained allowing detector characterisation.

B. *Towards technological prototypes*

The good results obtained with the 8x32 cm^2 detector and Hardroc pushed for moving to the square meter, scalable prototype in order to address large dimensions issues, as much for the detector as for the readout electronics. Such a prototype made of 6 boards of 32x48 cm^2 readout by 96 HARDROC (Figure 14) has been designed by the IPNL electronics group and associated to GRPC detector to be tested in test beam at CERN during the 2009 summer (Figure 15). The full scale readout has been exercised and up to 93% efficiency has been obtained with this 1m^2 PCB associated to GRPC detector.

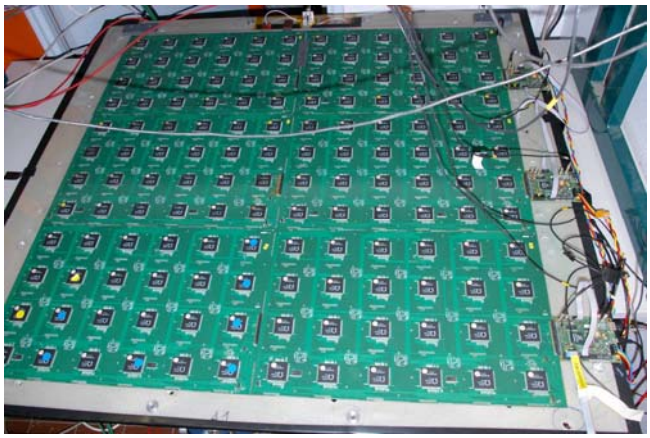

Figure 14: 1m^2 GRPC prototype

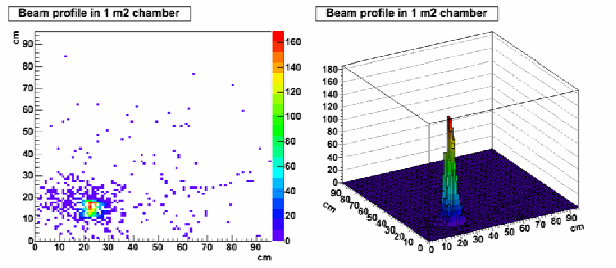

Figure 15: Beam profile in a 1m^2 GRPC chamber (©IPNL)

In parallel two 32x48 pad PCBs equipped with HARDROC and associated to micromegas have been tested under ^{55}Fe irradiation (Figure 16). A 1m^2 micromegas detector readout by 144 hardrocs will be tested under test beam this autumn.

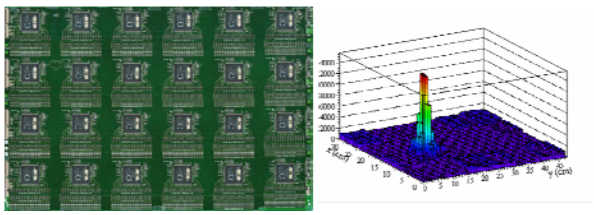

Figure 16: 32x48 cm^2 micromegas chamber under ^{55}Fe irradiation (©LAPP)

V. SMALL PRODUCTION TEST

To equip large detectors, 300 hardroc chips have been tested using a testboard and a dedicated Labview program (written by IPNL Lyon).

DC levels, power consumption, DACs linearity, memory test and trigger efficiency measurements have been performed.

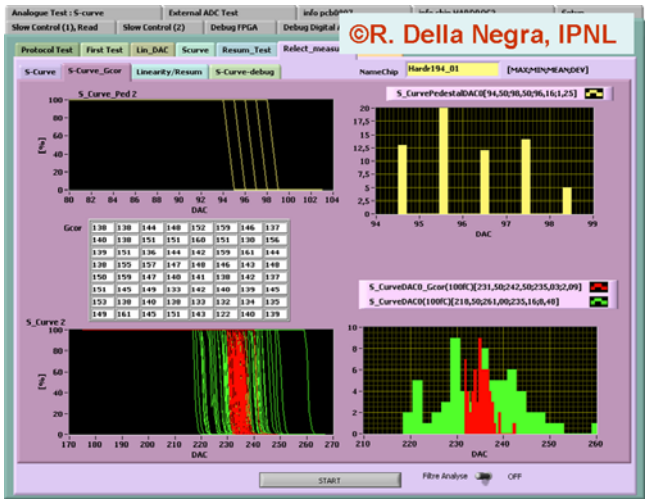

Figure 17: Labview program (©IPNL)

VI. CONCLUSION

Hardroc exhibits good performance and is ready for production. The semi digital readout and the daisy chain have been tested on large prototypes in test beam. The power pulsing, tested on test bench, has to be validated in test beam. The production of 5000 chips to equip a 1m3 prototype is foreseen in 2010.

VII. REFERENCES

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[4] Presentation of the "ROC" chips readout, poster by F. Dulucq.
[5] GRPC activities led by I. Laktineh *et al*, IPN Lyon
[6] Micromegas activities led by C. Adloff *et al*, LAPP Annecy