Commissioning and performance of the Preshower off-detector readout electronics in the CMS experiment

G. Antchev [a,b], D. Barney [a], W. Bialas [a], R.S. Bonilla Osorio [c], K.-F. Chen [d], C.-M. Kuo [e], R.-S. Lu [d], V. Patras [f], S. Reynaud [a], J.S. Rodriguez Estupinan [c], P. Vichoudis [a]

[a] CERN, 1211 Geneva 23, Switzerland,
[b] INRNE-BAS, Sofia, Bulgaria
[c] Universidad de los Andes, Bogotá, Colombia
[d] National Taiwan University, Taipei, Taiwan
[e] National Central University, Chung-Li, Taiwan
[f] University of Ioannina, Ioannina, Greece

Paschalis.Vichoudis@cern.ch

Abstract

The CMS Preshower is a fine grain detector that comprises 4288 silicon sensors, each containing 32 strips. The data are transferred from the detector to the counting room via 1208 optical fibres producing a total data flow of ~72GB/s. For their readout, 40 multi-FPGA 9U VME boards are used.

This article is focused on the commissioning of the VME readout system using two tools: a custom connectivity test system based on FPGA embedded logic analyzers read out through JTAG and an FPGA-based system that emulates the data-traffic from the detector. Additionally, the performance of the VME readout system in the CMS experiment, including the 2009 Cosmic ray at Four Tesla (CRAFT) run, is discussed.

I. INTRODUCTION

A. The detector

The CMS Preshower [1] is a fine grain detector located in front of the endcap Electromagnetic calorimeter. Its primary function is to detect photons with good spatial resolution in order to perform π^0 rejection. The detector comprises 4288 63mm x 63mm silicon sensors, each of which is divided into 32 strips. Fig.1 shows the location of the Preshower in the CMS experiment.

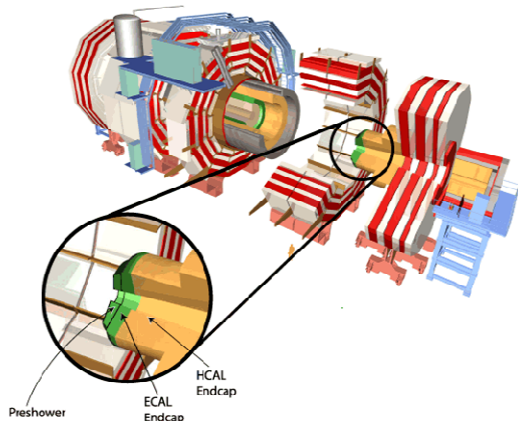The micromodule [1] (see Fig.2), building unit of the CMS Preshower detector, comprises a silicon sensor DC-coupled to a PCB hybrid containing the PACE3 [2] front-end electronics, all mounted on ceramic and aluminium support structures. The signals from the 32 strips of the micromodule are amplified, shaped and sampled continuously every ~25ns and temporarily stored in an analogue memory by the PACE3.

On reception of a level-1 trigger, three consecutive time samples (on the baseline, near the peak and after the peak) per strip are multiplexed, driven out of the micromodule and digitized by a 12-bit AD41240 ADC [3] on the Preshower 'system mother-board' (SMB).

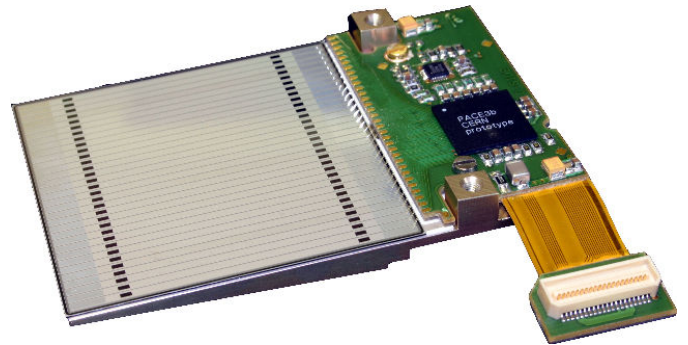Fig.3 illustrates a signal at the output of the preamplifier/shaper.

Figure 2: The micromodule.

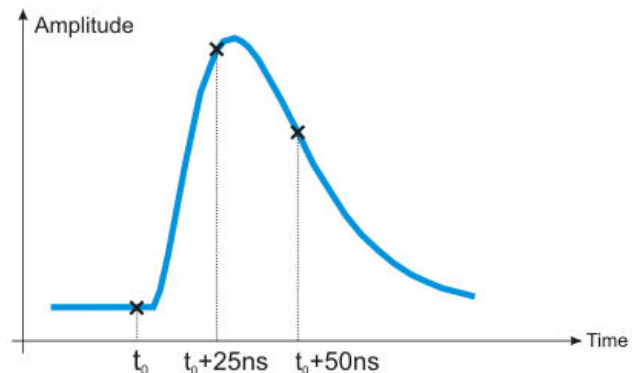Figure 1: The CMS experiment & the location of Preshower.

Figure 3: The preamplifier/shaper output signal.

The digitized data from up to 4 micromodules are multiplexed and organized in a 600-byte packet by a K-chip [4] ASIC and transmitted through an optical link via the GOL [5] serializer ASIC to the Counting Room. The K-chip and GOL ASICs are also located on the SMB. Fig. 4 illustrates the on-detector readout scheme.
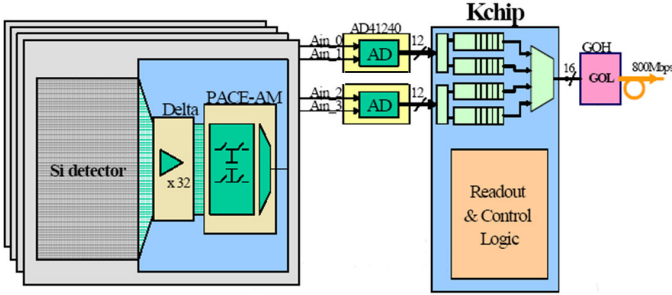

Figure 4: The on-detector data readout scheme.

B. The off-detector readout scheme

The data transport from the 4288 micromodules of the on-detector system is achieved by 1208 optical channels. Since the maximum average level-1 trigger rate is 100kHz, the total data flow from the detector to the off-detector electronics reaches ~72GB/s (1208 x 600B/event x 100k events/s).

For the readout of the Preshower, 40 off-detector electronic cards, namely the CMS Preshower Data Concentrator Card (ESDCC) [6] are used. Each ESDCC reads out 24 to 36 optical channels and interfaces with a CMS DAQ link having bandwidth of ~200MB/s (~2kB/event).

Although the total downstream bandwidth of ~8GB/s (40links x 200MB/s) is one order of magnitude lower than the total data flow from the detector, the Preshower can be read out without problems since significant online data reduction is performed in the ESDCCs. The data reduction includes pedestal subtraction, inter-channel gain calibration, common mode noise rejection, bunch crossing identification & threshold application [7].

It is worth mentioning that this level of data reduction (by a factor of ~10 or more) is feasible since the occupancy is relatively low in the Preshower - an average of about 2% at high luminosity.

C. The ESDCC

The ESDCC is a 9U-VME system based around eight high-density FPGAs.

Three of these FPGAs, incorporating embedded hardware deserializers, receive the serialized data streams from the detector and perform the on-line data reduction algorithms. Each of these FPGAs (will be referred-to as 'reduction FPGAs') can treat up to 12 input data streams. The zero-suppressed data coming from the reduction FPGAs are merged by another FPGA (will be referred-to as 'merger FPGA') that also serves as the interface with the central CMS data acquisition system.

Additionally, an FPGA (will be referred-to as 'vme FPGA') is used as an interface with the VME bus while another three FPGAs (with sufficient memory) receive the non-processed (often referred-to as 'raw') data from the

reduction FPGAs for event monitoring through the VME bus (these FPGAs will be referred-to as 'spy FPGAs').

A simplified block diagram of the ESDCC highlighting the data paths is shown in Fig. 5.
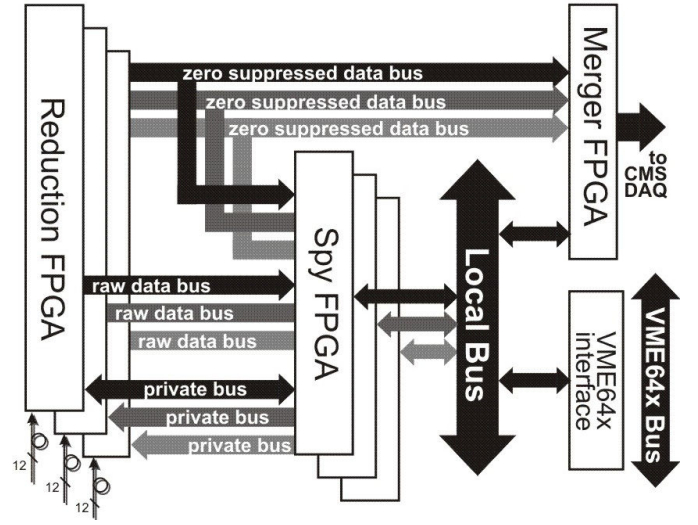
Figure 5: Data Paths of the ESDCC.

For the implementation of the ESDCC, the idea of a modular architecture has been adopted. The modularity allows the re-use of the modules by other systems [8][9]. The two modules the ESDCC is based around are:

- The optical receiver plug-in module.
- The VME 'host board'.

The optical receiver plug-in module, named the 'OptoRx' [10], is a daughter-board that hosts one reduction FPGA and the associated optical components while the VME host board is a motherboard in 9U VME format that incorporates the remaining FPGAs (merger, vme and spy FPGAs) as well as OptoRx sockets and other auxiliary components.

Fig.6 shows a picture of the ESDCC where three OptoRxs are plugged-in to a VME host board.

Figure 6: The ESDCC.

II. COMMISSIONING

This article is focused on hardware and software tools & methods developed for the commissioning of a complex system: the ESDCC. The concept behind this development was to have a system able to verify the ESDCC system in three steps:

- Verification of the hardware production of the OptoRx and the VME host board modules that have been produced separately in different sites. This step involves only the hardware modules of the ESDCC.
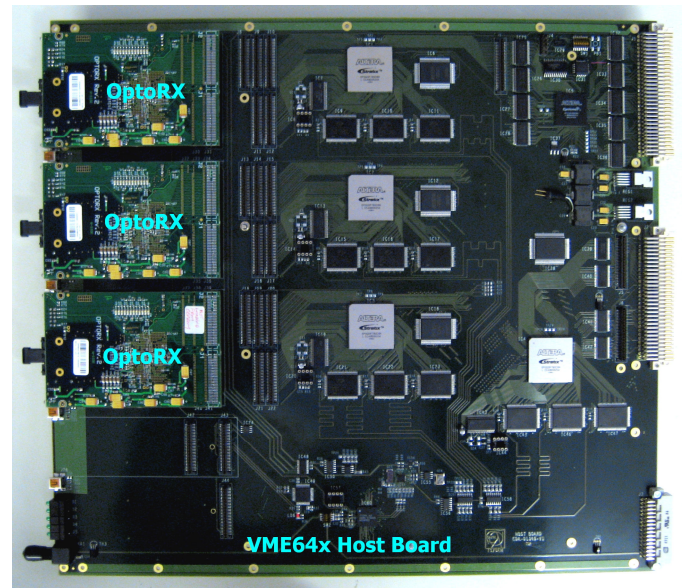
- Verification of the functionality of the ESDCC as a whole. This step involves both the hardware and firmware of the ESDCC.

- Verification of the compliance of the ESDCC with the central CMS data acquisition and in-situ performance. This step involves the hardware, firmware and software of the ESDCC.

This chapter describes the first two steps of the commissioning while the last step is described in chapter III.

A. The hardware commissioning

The hardware commissioning tools developed were targeted both for after-production tests at the production site and for reception tests at CERN. Experience with systems comprising high-density FPGAs (~1000pin BGA packages) has shown that performing connectivity tests between components on-board (after the typical production tests e.g. thermal stress/cycling, burn-in tests etc) is essential for the verification of the production. The fact that these tests had to be performed also in the production sites outside CERN added an extra complication in the development of the commissioning tools. The main problems were:

- Difficulty in transportation of heavy hardware equipment (e.g. VME crates etc) that would normally simplify the testing procedure.

- Software licensing complications of commercial JTAG boundary scan testing applications that would normally simplify the testing procedure.

In order to override these difficulties in the development of the hardware commissioning tools, a different strategy has been followed. The hardware commissioning system is a custom connectivity test bench based on FPGA embedded logic analyzers. The concept of the testing method is the following: In order to verify one connection line, the line must be toggled from one end and read/verified at the other end. To do so, one or more FPGAs of the unit under test generate certain patterns that are received by other FPGAs of the same unit. In case of open connections (e.g. from an FPGA to a connector), special PCBs are attached to the connectors and redirect the signals to other FPGA I/O lines. The patterns trigger the embedded logic analyzers in the receiving end and are recorded and readout through JTAG. A LabVIEW application compares the expected results with the ones received from the unit under test. It also presents the pin locations of the faulty connections for ease of debugging. To cover all interconnections of a module, a series of different tests is performed, where the transmitting and receiving ends

are defined accordingly (by configuring the FPGAs with different firmware). An example of this method is shown in Fig.7 and Fig.8. Fig.7 illustrates the interconnections of the VME host board whilst Fig.8 shows a diagram of a test setup that covers the connections to/from the VME connectors. At the right of the VME host board under test, a special PCB (see Fig.9) is attached to the associated connectors to redirect the signals to FPGA I/O lines that can capture them.
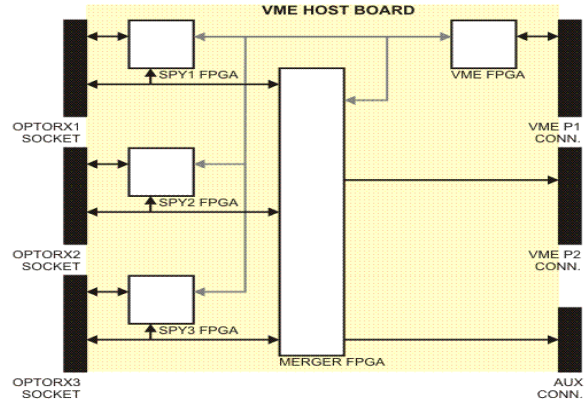
Figure 7: The interconnections of the VME host board.
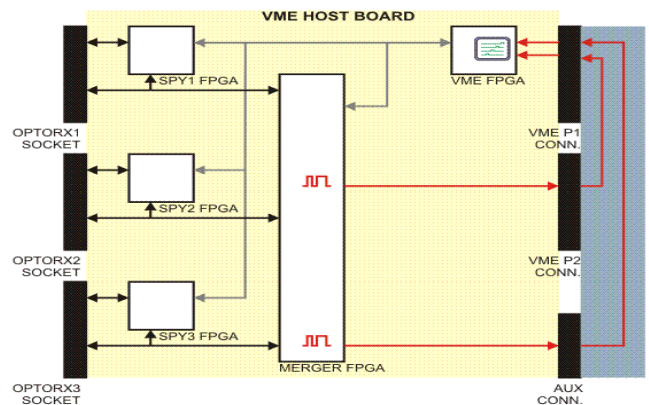
Figure 8: Setup for testing the lines from/to the VME connectors.
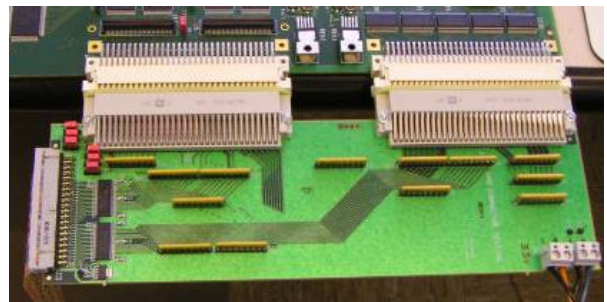
Figure 9: The special PCB used for the VME connector tests.

Fig.10 shows a pattern captured by the embedded logic analyzer whilst Fig.11 shows the front panel of the LabVIEW application developed for analyzing recorded patterns.

The test system described above was used extensively at the production site of the VME host board. Indeed the tests (about 5 minutes per board) revealed serious soldering problems throughout the first production batch. Subsequent improvements to the production process were verified using this test system, with the result that the boards now being produced are far more reliable.

Figure 10: Pattern captured by the embedded logic analyzers.

Figure 11: The front panel of the LabVIEW application.

The OptoRx, contrary to the VME host board, consists only of open connections from the FPGA I/O to the socket and from the optical receiver to the FPGA hardware deserializer inputs. Therefore, special PCBs are again needed for its hardware commissioning. Although the concept of the test is the same as with the VME host board, the implementation of the special PCBs is slightly different. A module, namely OptoTx, has been developed based on the OptoRx: the only difference between these pin-to-pin compatible modules is that the optical receivers have been replaced by optical transmitters. Fig.12 shows a diagram of the test setup. Both the OptoTx and OptoRx are plugged-in to a motherboard that interconnects the sockets of the two modules. For the optical loopback, optical fibres are used. Fig.13 shows a picture of the OptoRx test setup.

By using this fast (1 min) but extensive test system, ~5% defective OptoRx modules (out of ~150) have been found after production.

Figure 12: Diagram of the OptoRx test setup.

Figure 13: The OptoRx test setup. The motherboard, the OptoTx module and the socket for the unit under test are shown.

B. The hardware & firmware commissioning

For the hardware & firmware commissioning, a second FPGA-based test system known as the "ESDTE" (Preshower Data Traffic Emulator) has been developed by combining existing modules. As its name suggests, the ESDTE emulates the front-end of the Preshower, providing user-programmable data patterns combined (or not) with real previously recorded data from the detector.

The implementation of the ESDTE is based on existing components - the VME host board and the OptoTx mezzanine. The ESDTE operates like an 'inverted' ESDCC, downloading through VME data packets to the on-board memories that are then read by the FPGAs, serialized and transmitted optically.

The ESDCC functionality can thus be verified in the laboratory without the need for the real detector hardware as a data source. In addition, the ESDTE is able to generate rare (but possible) error conditions that are not easily reproducible with the real detector, such as the following:

- Data integrity errors
- Synchronization problems
- Interrupt packet transmission
- Do not send a packet (emulate missing triggers)
- Send a packet w/out trigger (emulate spurious triggers)

Flexible software tools have been developed to accompany this hardware, enabling easy control of both the ESDTE and ESDCC (C++ programs) as well as the subsequent data analysis (based on MatLab) avoiding in this way the use of the complex CMS DAQ software in this stage. The duration of the functionality test is about 60 min per ESDCC.

The ESDTE played an essential role both in the firmware development and debugging and in a second stage of hardware debugging of problems not spotted in the previous commissioning phase.
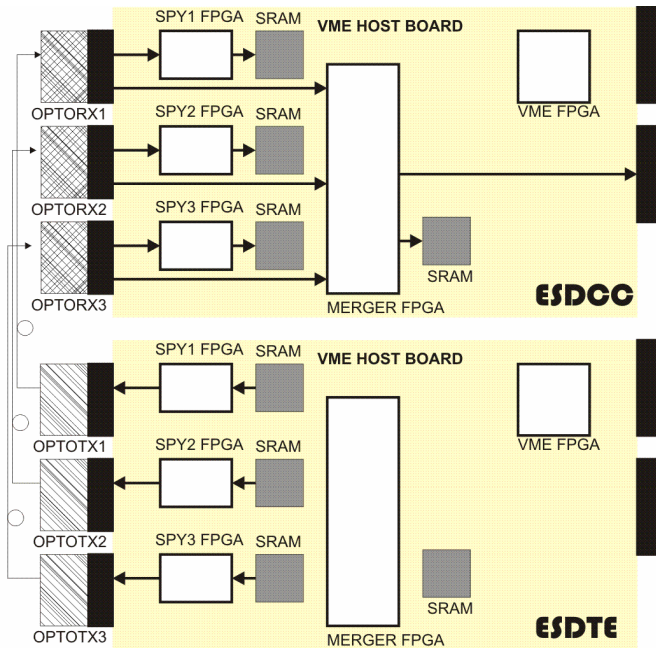
Figure 14: ESDCC functionality test setup.

The firmware of the ESDCC is expected to evolve with time, depending on the real conditions experienced within CMS. The ESDTE will thus form an important part of the development and debugging throughout the lifetime of the Preshower.

III. INSTALLATION AND FIRST USE OF THE ESDCCs IN CMS

The Preshower detectors were installed in CMS in spring 2009. Shortly afterwards the first 20 ESDCC boards (from a required total of 40) were installed in their VME crates (10 per crate) and commissioned using the ESDTE. The filled crates were then installed in their final locations underground - one for the ES+ endcap and the other for the ES- endcap - and used to perform a first in-situ commissioning of the Preshower. Each crate was used twice: once for each plane of each endcap.

At the beginning of August CMS began operating 24/7 for 6 weeks with the magnet at full power - the so-called "CRAFT09" (Cosmic Ray At Four Tesla). During this period the Preshower included one ESDCC crate (front-plane of ES+) in the central CMS DAQ system whilst the other crate was used for debugging purposes. The first in-situ cosmic rays were seen in the Preshower in the middle of August. Near the end of August the remaining 2 crates were commissioned and installed and a day later all 40 ESDCCs were successfully included in the CMS DAQ system for the first time. The time between reception of these final cards from the producer and having them operating in CMS was about a week. This was only possible because of the fast but extensive test systems described earlier in this note.

IV. SUMMARY

For the commissioning of the ESDCC readout system of the CMS Preshower subdetector, various test systems have been developed at CERN. These systems were targeted for the verification of the hardware production and the functionality of the ESDCC.

The hardware commissioning tools have been deployed both at the producer sites and at CERN. By using these systems, many faults have been found, both "batch-wide" (soldering problems) and on individual boards that lead to actions being taken at the producer such that the final boards installed in CMS meet the specifications and are reliable.

The ESDTE functionality verification system has contributed significantly to the development of the ESDCC firmware and to the fast and efficient commissioning of the readout VME crates at CMS. The ESDTE will continue to be used for future firmware development.

Currently, all 40 ESDCCs are installed and operational at CMS.

V. REFERENCES

[1] The CMS collaboration "The CMS experiment at the CERN LHC", 2008 JINST 8 S08004.

[2] P.Aspell et al "PACE3: A large dynamic range analog memory front-end ASIC assembly for the charge readout of silicon sensors", IEEE Nuclear Science Symposium Conference Record, 2005 Vol.2, 904.

[3] G. Minderico et al "A CMOS low power, quad channel, 12 bit, 40MS/s pipelined ADC for applications in particle physics calorimetry", 9th Workshop on Electronics for LHC Experiments Conference Record, 2003, pp. 88-91.

[4] K.Kloukinas et al "Kchip: A radiation tolerant digital data concentrator chip for the CMS Preshower detector", 9th Workshop on electronics for LHC Experiments Conference Record, 2003, pp. 66-70.

[5] P. Moreira et al "G-Link and Gigabit Ethernet compliant serializer for LHC data transmission", IEEE Nuclear Science Symposium Conference Record, 2000, Vol. 2, pp. 9/6-9/9.

[6] G. Antchev et al "A VME-based readout system for the CMS Preshower sub-detector", IEEE Trans Nucl Sci 54 623.

[7] D. Barney et al "Implementation of on-line data reduction algorithms in the CMS Endcap Preshower data concentrator card", 2007 JINST 2 P03001.

[8] G. Antchev et al "The TOTEM Front End Driver, its Components and Applications in the TOTEM Experiment", Proceedings of the Topical Workshop on Electronics for Particle Physics, 2007, pp.211-214.

[9] W. Beaumont et al "Design of the CMS-CASTOR sub detector readout system by reusing existing designs", presented at the Topical Workshop on Electronics for Particle Physics, 2009.

[10] S. Reynaud, P. Vichoudis "A multi-channel optical plug-in module for gigabit data reception", Proceedings of the 12th Workshop on electronics for LHC and future experiments, 2006, pp.229-231.