Reduction techniques of the back gate effect in the SOI Pixel Detector

R. Ichimiya [a], Y. Arai [a], K. Fukuda [b], I. Kurachi [b], N. Kuriyama [c], M. Ohno [d], M. Okihara [c]
for the SOI Pixel collaboration

[a] Institute of Particle and Nuclear Studies, High Energy Accelerator Research Org., KEK, Tsukuba 305-0801, Japan
[b] Oki Semiconductor Co. Ltd., 2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
[c] Oki Semiconductor Miyagi Co. Ltd., 1, Okinodaira, Ohira-mura, kurokawa-gun, Miyagi 981-3693, Japan
[d] National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba 305-8568, Japan

ryo@post.kek.jp

Abstract

We have fabricated monolithic pixel sensors in 0.2 µm Silicon-On-Insulator (SOI) CMOS technology, consisting of a thick sensor layer and a thin circuit layer with an insulating buried-oxide, which has many advantages. However, it has been found that the applied electric field in the sensor layer also affects the transistor operation in the adjacent circuit layer. This limits the applicable sensor bias well below the full depletion voltage. To overcome this, we performed a TCAD simulation and added an additional p-well (buried p-well) in the SOI process. Designs and preliminary results are presented.

I. INTRODUCTION

A Silicon-on-Insulator (SOI) CMOS technology has a lot of advantages to realize a high-speed and low-power LSI circuit. Nowadays, SOI CMOS technology is widely used for commercial and industrial production. SOI technology enables a monolithic pixel detector by bonding thick high-resistivity silicon for sensor and thin low-resistivity silicon for readout electronics interleaved with an insulating buried oxide layer (BOX). Contacts between the sensing nodes of the sensor layer and the readout circuitry are made through the BOX layer [1-3]. Compared to conventional bulk CMOS pixel sensors, SOI pixel sensor has following advantages:

- No mechanical bump bonding is required; minimizing multiple scattering in the detector and making smaller pixel size is possible.
- Small parasitic capacitance (~10fF) of sensing nodes gives a large conversion gain and lower noise.
- Small active volume in each transistor ensures latch-up immunity and high radiation tolerance.
- Both sensor and readout electronics can be fabricated with the industry standard SOI process; further progress and lower cost are expected.
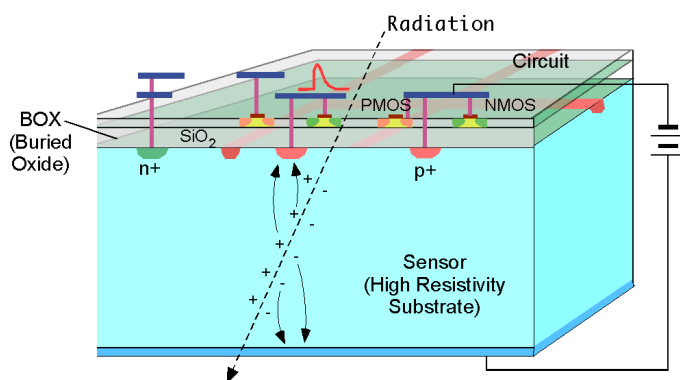

Figure 1: Cross-sectional view of the SOI pixel detector

We have been developing an SOI pixel process based on OKI Semiconductor Co. Ltd., 0.2 µm CMOS fully-depleted (FD-) SOI commercial mass-production process [4].

II. SOI PIXEL PROCESS

Figure 2 shows a simplified procedure for the fabrication process of the SOI pixel detector. After etching BOX layer, implantation of p+/n+ to handle wafer is performed, then contacts between the p+/n+ wells and the 1st metal layer are formed.

After wafer processing, the wafer backside is ground mechanically from 725 µm to 260 µm, then sputtered with 200 nm of aluminum. The detector bias voltage can be applied from the backside and also from the top pads which are connected to a high voltage n+ ring.

Characteristics and SOI process parameters are summarized in Table 1. Three types of transistors, Metal-Insulating-Metal (MIM) capacitors, depletion MOS (DMOS), lateral diodes and several kinds of resistors are provided.
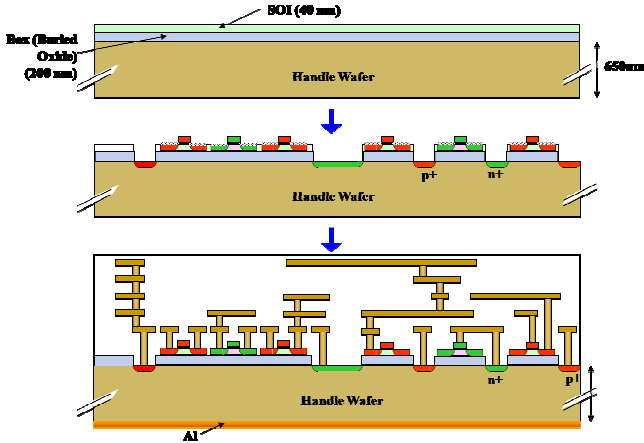
Figure 2: Conceptual SOI pixel detector process flow.

Table 1: SOI pixel process specifications.

Process	0.2 μm Low-Leakage Fully-Depleted SOI CMOS, 1 poly, 4 Metal layers, MIM cap., DMOS option, Core (I/O) voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mm φ Top Si: Cz, ~18Ω-cm, p-type, ~40nm thick Buried Oxide: 200 nm thick Handle wafer: Cz n-type 700Ω-cm, 725 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm)
Transistor	Normal and low threshold transistors are available for both core(1.8V) and IO(3.3V). Three type of structure (body-floating, source-tie and body-tie) are available.
Optional process	Buried p-well (BPW) formation.

We have been organizing Multi Project Wafer (MPW) runs periodically to reduce development cost and share knowledge. We have three MPW runs in 2009. In each MPW run, we have about 15-20 designs from SOI pixel collaborators [5-7]. This MPW runs are open to any academic users.

III. BACK GATE EFFECT REDUCTION TECHNIQUE

While the SOI structure is ideal for realizing the monolithic pixel detector, applied electric field in the sensor layer also affects transistor operation in the adjacent LSI circuit layer (back gate effect). Due to this phenomenon, sufficient bias voltage to make the sensor fully depleted could not be applied. To understand the back gate effect in detail, we performed a TCAD simulation. Figure 3 shows the TCAD simulation result of the electron current density distribution of a core NMOS transistor. When a backside bias voltage $V_{back} = 30V$ is applied, a current path is formed (back side channel) below gate at lower surface of the SOI layer (displayed in orange color). During the back side channel is open, the transistor remains ON even if negative gate voltage is applied.
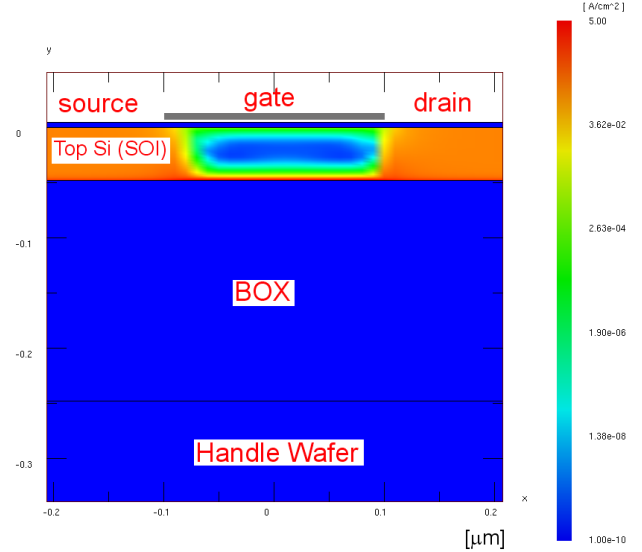

Figure 3: A TCAD simulation result of electron current density distribution of a core NMOS transistor is displayed. (V_d=0.1V, V_g=V_s=0V) Under a backside bias voltage $V_{back} = 30V$ is applied, a current path is formed (back side channel) below gate at lower surface of the SOI layer (displayed in orange color). Note that the gate electrode (gray) in this plot is not in scale.

Based on this TCAD simulation study, we have introduced buried p-well (BPW) implantation process in the handle wafer. A p-type dopant is implanted through the top Si layer to form a p-well just below the buried oxide (BOX) layer (Figure 4). The doping level of BPW is about three orders lower than that of the p+ sensor node and source/drain region, so it does not affect transistor's characteristics. We have optimized the implantation energy by a TCAD process simulation so that the peak density is located under the BOX region.

Figure 5 (6) shows the I_d-V_{gs} curve of an NMOS (PMOS) transistor of a TEG chip when the backside bias voltage is applied. Especially NMOS transistor is affected by applied backside bias voltage. However, by introducing BPW, the back gate effect is effectively suppressed for both NMOS and PMOS transistors.
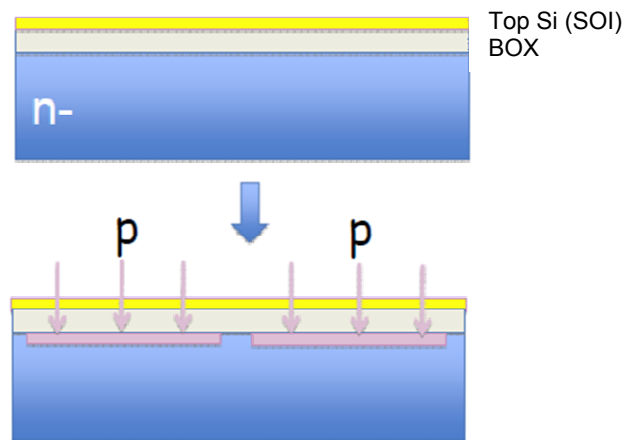

Figure 4: Buried p-well (BPW) implantation method is shown. By implanting light p-type dopant under the BOX layer, the back gate effect is effectively suppressed. In the pixel, BPW can be used to extend the sensor node.
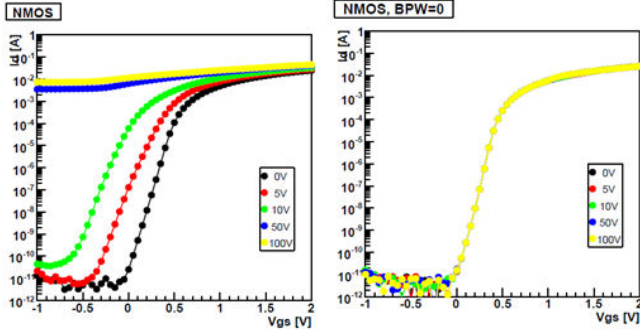
Figure 5: Measured NMOS I_d-V_{gs} curves without BPW (left) and with BPW (right) shown for various backside bias voltages.
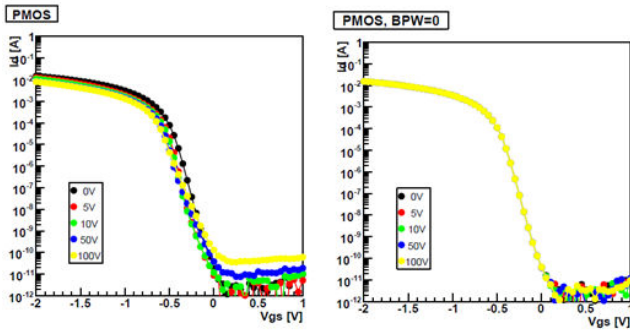

Figure 6: Measured PMOS I_d-V_{gs} curves without BPW (left) and with BPW (right) shown for various backside bias voltages.

IV. PIXEL DETECTOR TEST RESULTS

Figure 7 shows the SOI pixel sensor I-V characteristics. The break down voltage depends on the guard ring geometry and the BPW layout. The BPW layer reduces electric field gradients at critical points, so it increases the break down voltage.

We are developing two kinds of pixel detectors. One is integration type pixel detector named INTPIX. The other is counting type pixel detector named CNTPIX.
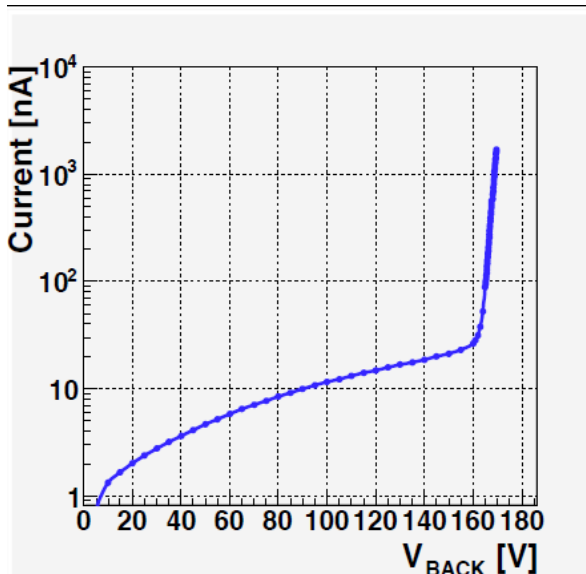

Figure 7: I-V characteristic of SOI pixel sensor (INTPIX3).

A. Integration type pixel (INTPIX)

The integration type pixel (INTPIX) has 5 mm by 5 mm chip size and 128 x 128 pixels each 20 μm square. Figure 8 shows a readout circuit implemented for each pixel. The detector signal is buffered by a source follower and then stored in a 100 fF capacitor (C_{store}). When read_x is asserted, V_{store} is readout by an external ADC.

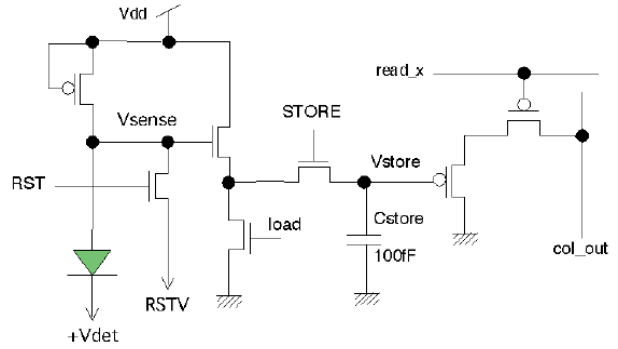Figure 9 shows a visible light image taken by the INTPIX detector.

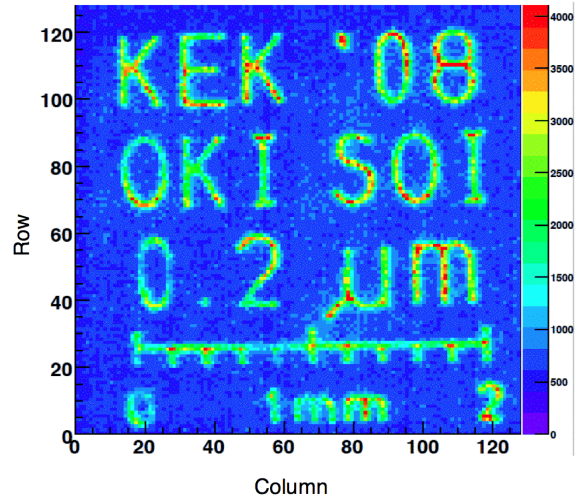Figure 8: Readout circuit of integration type pixel (INTPIX).

Figure 9: A visible light image taken by the INTPIX detector with a mask.

B. Counting type pixel (CNTPIX)

Figure 10 shows a readout circuit for each pixel of the counting type pixel (CNTPIX). The preamplifier circuit is based on the design proposed by Krummenacher [8] which contains leakage current compensation circuitry. It is equipped with low and high threshold discriminators so that window comparator mode is possible. Discriminator output is fed to a 16-bit counter. The size of a pixel is about 60 μm square.

Figure 11 shows an 8 keV X-ray image taken by the CNTPIX detector with a brass mask in front.
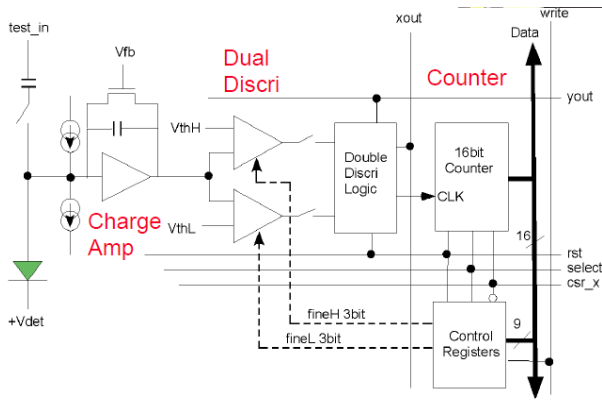
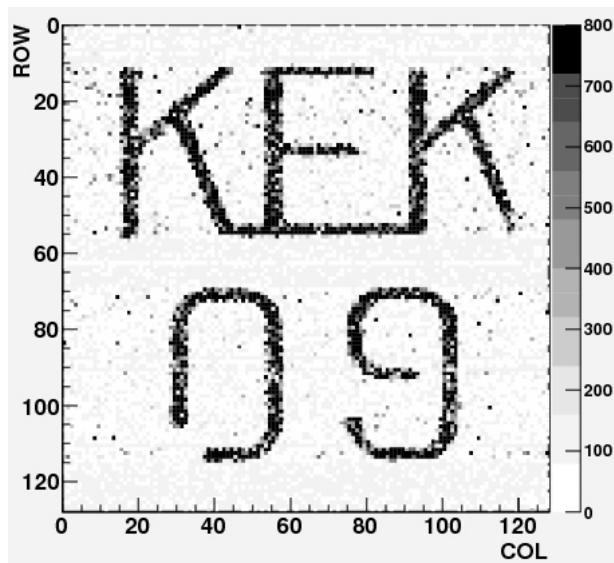Figure 10:   Readout circuit of counting type pixel (CNTPIX).

Figure 11:   X-ray image taken by counting type pixel (CNTPIX).

V. SUMMARY

We are developing SOI pixel detectors based on 0.2 µm OKI Semiconductor FD-SOI commercial mass-production process. While the SOI structure is ideal for realizing the monolithic pixel detector, the back gate effect caused by applied bias voltage has to be overcome. We have developed a BPW implantation technique and confirmed it to suppress the back gate effect effectively.

We have been organizing MPW runs to share runs with designs from SOI pixel collaborators. Two types of SOI pixel detector (integration type and counting type) has been developed and confirmed of their functionality.

VI. ACKNOWLEDGEMENTS

VII.   REFERENCES

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