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# Front End Electronics for Pixel Detector of the PANDA MVD

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*Abstract*

ToPix 2.0 is a prototype in a CMOS 0.13 $\mu m$ technology of the front-end chip for the hybrid pixel sensors that will equip the Micro-Vertex Detector of the PANDA experiment at GSI. The Time over Threshold (ToT) approach has been employed to provide a high charge dynamic range (up to 100 fC) with a low power dissipation (15 $\mu W$/cell). In an area of $100\mu m \times 100\mu m$ each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the time and charge information. The ASIC includes 320 pixel readout cells organized in four columns and a simplified version of the end of column readout.

## I. Introduction

PANDA [1] will be one of the main experiments at FAIR, the future facility for antiproton and ion research under construction at Darmstadt, Germany.

PANDA will exploit antiproton-proton and antiproton-nucleus reactions for precise QCD studies. Its physics program includes the spectroscopy of charmonium states and investigation of open charm production, the search of glueballs and hybrids, the study of the behavior of hadrons in nuclear matter, and precise $\gamma$ ray spectroscopy of hypernuclei. The PANDA experiment will be located in the High Energy Storage Ring (HESR), which will provide a high quality antiproton beam (see Table 1).

Table 1: HESR working modalities

| Modality | High luminosity | High resolution |
|---|---|---|
| Luminosity | $2 \times 10^{32} cm^{-2} s^{-1}$ | $10^{31} cm^{-2} s^{-1}$ |
| Resolution ($\delta p/p$) | $\sim 10^{-4}$ | $\sim 10^{-5}$ |
| Cooling | stochastic cooling | electron cooling |
| Momentum range | $1.5 GeV/c$-$15 GeV/c$ | $1.5 GeV/c$-$8.9 GeV/c$ |

PANDA is a fixed target experiment, the experimental apparatus is divided in two parts: the target spectrometer which surrounds the interaction point and the forward spectrometer to cover the angular region below $10°$.

The Micro Vertex Detector (MVD) [2] is located in the innermost part of the experimental apparatus and will consist of silicon pixel and silicon strip detectors to obtain precise tracking of all charged particles. Since the MVD tracks a high number of low momentum particles [3] it is possible to achieve a particle identification trough the measurement of the energy loss per unit path-length (dE/dx). Physics simulations show that an accurate measurement of an energy loss up to $2.3 MeV$ allows the separation of different particle species (protons, kaons, pions/muons/electrons).
Figure 1 shows the present design of the MVD:

- Four Barrels
  Two inner layers: Hybrid pixel
  Two outer layers: Double sided strip
- Six Forward Disks
  First four disks: Hybrid pixel
  Last two disks: Pixel + Strip

The MVD requires 11M pixel readout channels covering $0.14 m^2$, and 70k strip readout channels covering $0.5 m^2$.
The custom solution for the readout of the pixel detector is motivated by the high track density (up to $12.3 Mhit/(s \cdot cm^2)$) and the absence of a trigger signal.

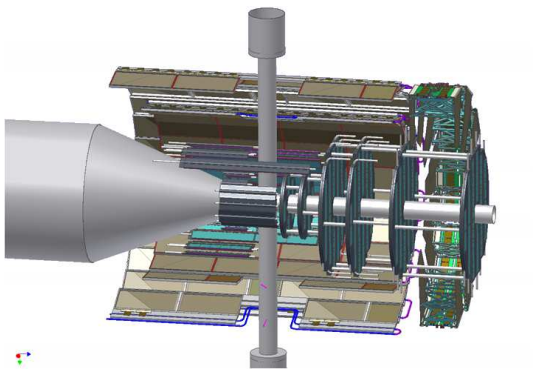

Figure 1: The PANDA MicroVertex Detector (MVD)

## II. Pixel ReadOut Chip

The specifications for the readout electronics are given by the PANDA radiation environment and the close proximity of the MVD to the interaction point. Table 2 summarises the specifications for the pixel readout cell.

Table 2: Pixel specifications

| | |
|---|---|
| Pixel Size | $100\ \mu m \times 100\ \mu m$ |
| Noise Level | $200\ e^-$ rms |
| Linear dynamic range | Up to 100 fC |
| Power consumption | $< 20 \mu W$ |
| Input polarity | Selectable |
| Leakage compensation | Up to 50 nA |

The ASIC has to give simultaneous time stamping and charge measurement. Table 3 shows the ASIC specifications.

Table 3: ASIC specifications

| Trigger | Self Triggering |
|---|---|
| Active area | $O(1cm^2)$ |
| Data rate | $O(0.8Gbit/s)$ |
| Radiation tolerance | $10Mrad$ |
| Time resolution | $6ns$ ($50MHz$ clock) |

## A. Time over Threshold Technique

The pixel readout architecture is based on the Time over Threshold technique [4] [5] which makes possible a low power charge digitization. The value of the injected charge is measured through the time needed to discharge a capacitor with a constant current.
The output voltage of a Charge Sensitive Amplifier is given by:

$$v_{out}(t) = \frac{Q_{in}(t)}{C_f} = \frac{1}{C_f}\int_0^t I_{in}(t') - I_{dis}(t')dt'$$

where $Q_{in}(t)$ is the collected charge at the input node, $C_f$ is the feedback capacitance, $I_{in}(t)$ the injecting current and $I_{dis}(t)$ the discharging current.
It is possible to assume the charge injection as instantaneous: $Q_{inj} = \int_0^{\epsilon} I_{in}(t')dt'$.
The discharging current is constant: $\int_0^t I_{dis}(t')dt' = I_{dis}t$.
With these assumptions the output voltage can be written as:

$$v_{out}(t) = \frac{Q_{inj} - I_{dis}t}{C_f}$$

When $t = ToT$ the voltage output is 0:

$$v_{out}(ToT) = \frac{Q_{inj} - I_{dis}ToT}{C_f} = 0$$

and the linear relationship between the injected charge and the ToT is thus obtained:

$$ToT = \frac{Q_{inj}}{I_{dis}}$$

The ToT allows to achieve good linearity and excellent resolution even when the preamplifier is saturated, thus allowing an high dynamic range of the charge measurement.

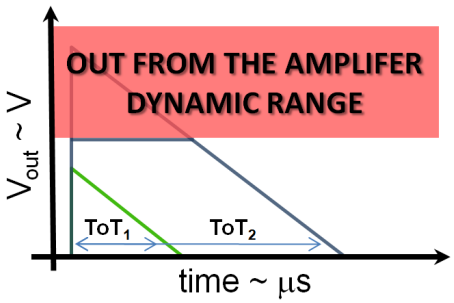


Figure 2: Output ToT signals

## B. Analog Front End

The analog front end generates a pulse which width is proportional to the charge injected by the pixel detector. It is made by a Charge Sensitive Amplifier with feedback, a leakage compensation system and a comparator with tunable threshold via a 5 bit DAC.

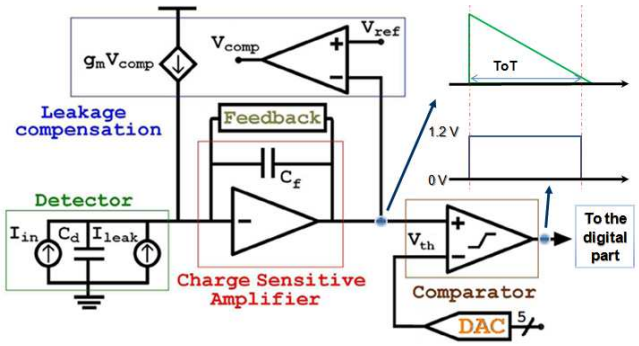


Figure 3: Analog ReadOut Channel

### 1) Charge sensitive amplifier

The charge sensitive amplifier is the core component of the ToT stage.
The input stage is a gain enhanced cascode amplifier with capacitive feedback, its input DC level is fixed by the input transistor current bias.
The output stage is made by a source follower with selectable polarity in order to maximize the output dynamic range, the output DC level is regulated by the leakage compensation system.

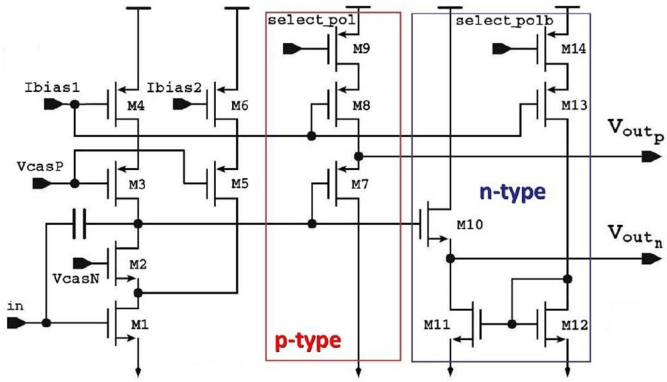


Figure 4: Charge Sensitive Amplifier

### 2) Feedback circuit

The feedback circuit generates a constant current to discharge the charge deposited on the input node. It is made by a differential stage which receives at the input the output signal of the CSA and the reference voltage, and injects the discharg-

ing current at the input node of the CSA ($I_{dis} = 5nA$). At the equilibrium provides an equivalent $8M\Omega$ feed-back resistor.

*3) Leakage compensation*

The pixel sensor leakage current may be up to 50nA. If the leakage current is smaller than the designed discharging current ($5nA$), it generates a voltage offset which unbalances the differential stage and the the effective discharging current depends on the leakage current. If the leakage current is larger than the discharging current, the extra current charges the feedback capacitance ($C_f$) quickly saturating the Charge Sensitive Amplifier.
In the upper part of the dynamic range the Time over Threshold can be very long, reaching up to $20\mu s$ for a 100 fC input. Therefore, a very low cutoff frequency is necessary in order to prevent these long signals from being clipped by the leakage compensation circuit. This would introduce a nonlinearity which is not desirable, because the resulting compression curve might depend on the value of the leakage current.

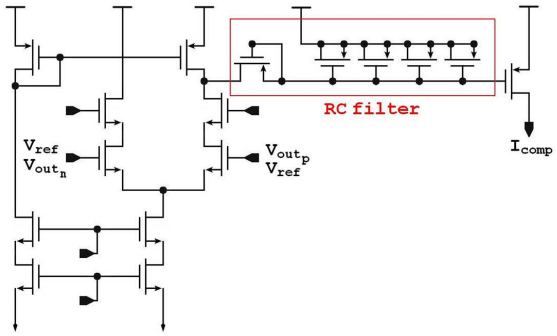


Figure 5: Leakage compensation stage

A compact filtering resistor with very high value is implemented through a PMOS with the gate shorted to the source. The filtering capacitor is implemented through MOS devices.

*4) Comparator*

The comparator has a folded cascode input stage with two CMOS inverters.

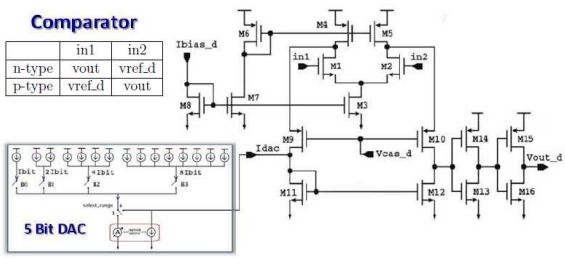


Figure 6: Comparator with 5 bit DAC

To mitigate the threshold dispersion a local five bit DAC is added in each pixel, to allow a fine tuning of the threshold on a pixel by pixel basis.
The DAC can sink or source current to a low impedance node, 1 bit selects the polarity and the other 4 the current value. The DAC full scale range is set by an external component on the PCB.

## C. Saturation and Cross Talk

When the CSA is not saturated the charge is collected on the feedback capacitance $C_f$, while it is saturated the extra charge is collected on the input capacitance $C_{in}$: the gain of the CSA drops and the input can not be considered anymore as a virtual ground.

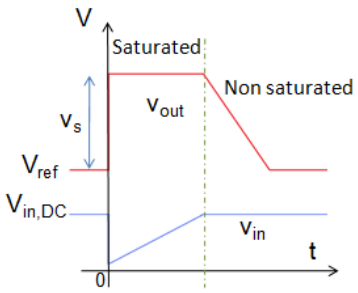


Figure 7: Saturated and linear mode

Table 4: CSA modes

| Modality | Non Saturated | Saturated |
|---|---|---|
| Charge collection | on $C_f = 24fC$ | on $C_{in} \approx 200fC$ |
| CSA gain | $1/C_f = 41.7mV/fC$ | drops |
| $v_{out}$ | $\frac{Q_{inj} - I_{dis}t}{C_f}$ | $v_s$ |
| $v_{in}$ | 0 | $-\frac{Q_{inj} - v_s C_f - I_{dis}t}{C_{in}}$ |

Due to the inter-pixel capacitance a voltage signal at the input of one channel induces a spurious signal at the input of the adjacent pixel. When the CSA saturates a voltage signal at the input node is present and the cross-talk effect is greatly magnified.

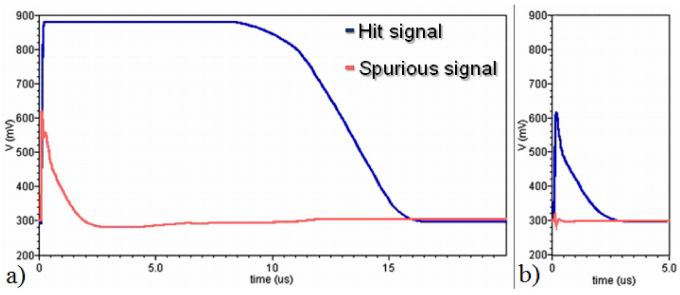


Figure 8: Cross talk effect

Figure 8 shows the result of two simulations performed to estimate the cross talk effect with an inter-pixel capacitance of $100fF$. In the first simulation (8.a) the injected charge is 90fC, the ToT signal saturates the preamplifier (dark line), and a spurious signal is present in the adjacent channel due to the cross talk (light line). In the second simulation (8.b) the injected charge is 5fC, the ToT signal does not saturates the preamplifier and the cross talk is negligible.

### D. Digital Readout

In each pixel the control logic receives the signal from the comparator and stores the value on the time stamp bus at the rising and falling edge in the 12 bit leading edge and trailing edge registers. It is also present a 12 bit configuration register. The registers are based on the DICE cells [6] in order to be Single Event Upset tolerant.
The pixels are arranged in columns, each column has a readout logic made in a fixed priority scheme to read the timestamps of the pixel cells and to read/write the configuration bits.

## III. ASIC Floorplan

Each readout cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information (Fig. 9). In each cell it is present a calibration circuit. When it is enabled it makes possible the injection of a test current pulse. Moreover 16 readout cells have an external connection to the wirebonding pads in order to connect a sensor or inject an external calibration signal.
ToPix 2.0 [7] has 320 pixel readout cells arranged in four columns: two short columns with 32 pixels and two folded column with 128 pixels. In the final version of ToPix the length of each column will be $\approx 11mm$. In this prototype folded columns are employed to estimate the effect of the column length on the data transmission. In this way it is possible to implement a long column in a limited area thus saving on the cost. Each column has a simplified readout logic.

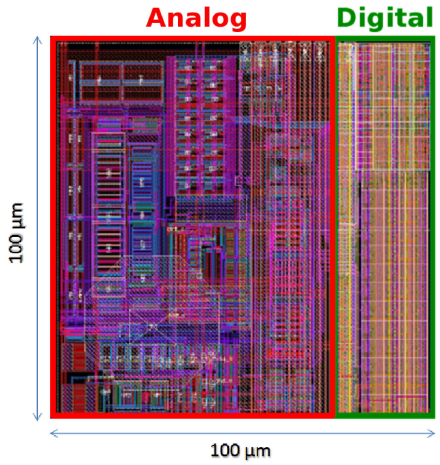


Figure 9: Layout of the readout cell

Fig.10 shows a photo of the chip, its size is $5mm \times 2mm$.

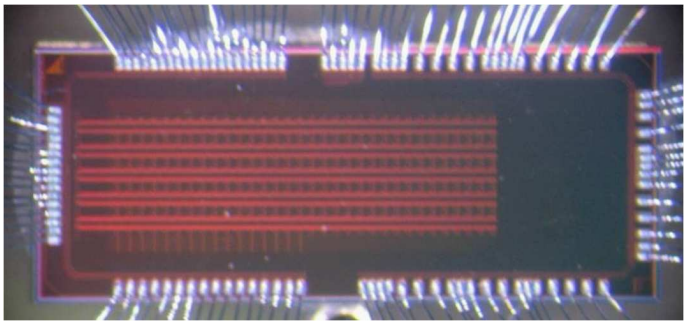

Figure 10: ToPix 2.0 Photo

The final version of ToPiX will consist of a matrix of $116 \times 110$ cells with a pixel size $100\mu m \times 100\mu m$, thus covering a $1.28cm^2$ active area.

### A. Test Results

#### 1) ToT Linearity

Figure 12 shows the result of ToT linearity simulation and and measurement on two readout pixels (p-type sensor signal). The result of the fit on the simulated values is :

$$ToT_p = 188\frac{ns}{fC}\,Q_{inj} + 300ns$$

The two measurement are compatible with this linear fit.

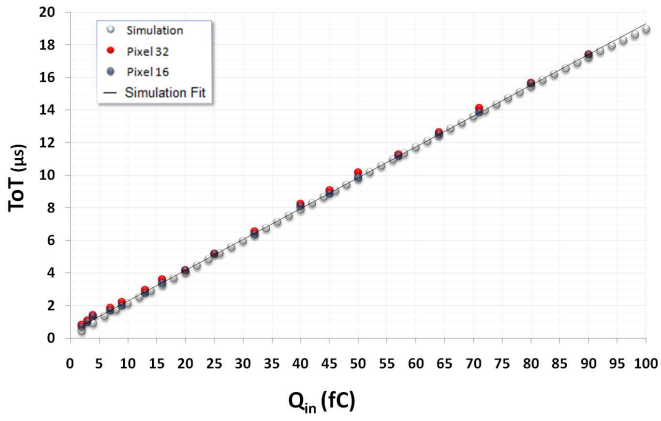


Figure 11: ToT linearity for a P-Type sensor

#### 2) ToT dispersion

The channel to channel ToT dispersion is $\frac{\Delta ToT}{ToT} \approx 10\%$. The discharging feedback current has minor implication on the uniformity between the different channels (Figure 12).

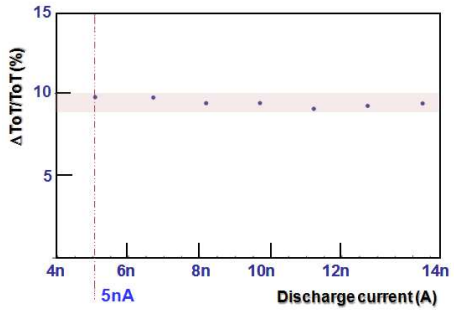


Figure 12: ToT dispersion

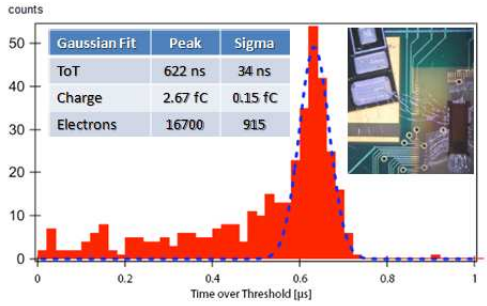


Figure 14: Epitaxial sensor measurement with a $^{214}Am$ source.

This result shows that the current source that biases the feedback stage does not give the major contribution in the ToT dispersion. The other blocks that contribute to the ToT dispersion are the differential pair of the feedback stage and the differential pair of the leakage compensation. Montecarlo simulations have been done to understand how to improve the ToT uniformity. The critical block is the leakage compensation stage, where the mismatch effects on its input transistors creates an offset that unbalance the feedback circuit changing the effective discharging current value.

*3) Threshold dispersion*

The local 5 bit DAC in each pixel for the threshold dispersion mitigation has been tested. Figure 13 shows the dispersion of the threshold values before the correction (light curve) and after the correction (dark curve).

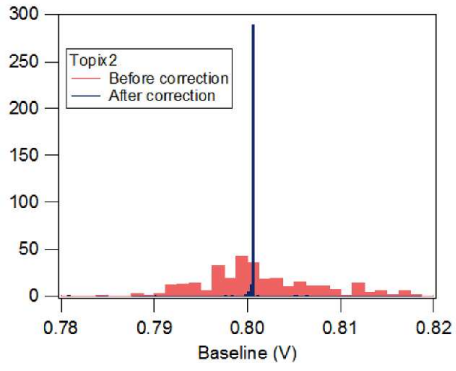


Figure 13: Threshold dispersion

*4) First spectra with an epi-sensor*

ToPix 2.0 has been tested with an epitaxial sensor (thickness: $50\mu m$, size: $125\mu m \times 325\mu m$) connected by wire bonding to the external pad of chip. Figure 14 shows the spectra obtained using a $^{214}Am$ source ($60keV$ $\gamma$ photons).
In this case the signal to noise ratio is limited by parasitics capacitance due the external connections: bonding pad, wire bonding and protection diodes.

## B. Conclusions

Tests show good agreement between specifications and measurements. An upgrade of Topix 2.0 is currently under design. ToPix is designed to work with a clock of $50MHz$, the clock of PANDA experiment has been fixed recently at $160MHz$ and the new version has to be compatible with the new clock. In order to keep the same $clock\_cycles$ to $injected\_charge$ ratio of ToPix 2.0, the discharging current value has to be proportionally increased from $5nA$ to $16nA$.
The chip will be designed using a different flavour of the process, which allows a more robust power supply distribution at the expense of the increased pitch of some of the metal layers. Moreover the sensitivity of the digital logic to the SEU has to be decreased. Consequently, the area reserved to the digital part must be increased. To comply with the new, more stringent space requirement the layout of the analog part has to be partially revised. Since the leakage compensation circuit is the analog block occupying the largest surface, a more compact design of this part is underway.

## References

[1] PANDA-Technical Progress Report, February 2005. http://www-panda.gsi.de/archive/TPR2005/panda_tp.pdf

[2] T. Stockmanns [PANDA Collaboration], "The micro-vertex-detector of the PANDA experiment at Darmstadt", Nucl. Instrum. Meth. A 568 (2006) 294.

[3] Physics Performance Report for PANDA: "Strong Interaction Studies with Antiprotons" March 2009, http://arxiv.org/abs/0903.3905v1

[4] I. Kipnis et al., "A time-over-threshold machine: the readout integrated circuit for the Babar silicon vertex tracker", IEEE Transactions on Nuclear Science 44, 3 (1997) 289.

[5] I. Peric et al., "The FEI3 readout chip for the ATLAS pixel detector", Nucl. Instr. and Meth. A 565 (2006) 178.

[6] T. Calin, M. Nicolaidis and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology", IEEE Trans. Nucl. Sci., vol. 43, pp. 2874-2878, Dec 1996

[7] D. Calvo, et al., "The silicon pixel system for the Micro Vertex Detector of the PANDA experiment", Nucl. Instr. and Meth. A (2009), doi:10.1016/j.nima.2009.09.043