A ten thousand frames per second readout MAPS for the EUDET beam telescope

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Abstract

Designed and manufactured in a commercial CMOS 0.35 µm OPTO process for equipping the EUDET beam telescope, MIMOSA26 is the first reticule size pixel sensor with digital output and integrated zero suppression. It features a matrix of pixels with 576 rows and 1152 columns, covering an active area of ~224 mm^2. A single point resolution of about 4 µm was obtained with a pixel pitch of 18.4 µm. Its architecture allows a fast readout frequency of ~10 k frames/s. The paper describes the chip design, test and major characterisation outcome.

I. INTRODUCTION

EUDET is a project supported by the European Union within the 6th Framework Programme structuring the European Research Area, with the aim to support the detector R&D in Europe for the next large particle project, the International Linear Collider (ILC).

Within the EUDET collaboration, a high resolution beam telescope [1] is being developed. It consists of 2 arms of 3 measurement planes (Fig.1). The latter are equipped with MAPS (Monolithic Active Pixel Sensors) providing excellent tracking performances [2]. An impact position resolution of ~2 µm is delivered by the beam telescope on the surface of the Device Under Test (DUT). It will be operated at DESYII 6 GeV electron beam facility like initially expected, and at CERN-SPS 120 GeV/c pions beam facility as well as.

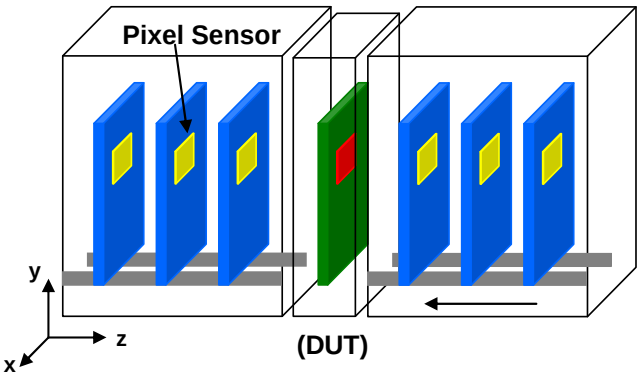

Figure 1: Schematic of the pixel telescope layout

In order to accelerate its commissioning, the construction of the telescope was organised in two stages. In the first stage, a demonstrator telescope, exploiting the existing CMOS MAPS sensors with analogue readout (MIMOSA17), has been realised. It has been successfully operating since 2007 [3]. In 2009, the final telescope is being equipped with the sensors presented in this paper: MIMOSA26. It provides an active surface exceeding 2 cm², which is 4 times larger than MIMOSA17. The readout time (~100 µs) is about an order of magnitude shorter [3] than with the previous sensor.

The design of the architecture of MIMOSA26 optimised for the EUDET beam telescope is discussed in this paper, followed by the preliminary test results obtained in the laboratory and with particle beams.

II. MIMOSA26 ARCHITECTURE

MIMOSA26 is a full scale sensor, designed in 2008 and fabricated at the beginning of 2009, in a CMOS 0.35 µm OPTO technology. It combines the architecture of MIMOSA22 and SUZE-01, already validated by two separate prototyping lines [4]. MIMOSA22 [5, 6] is composed of 128 columns of 576 pixels, each column being ended with a discriminator [7]. The pixel contains a pre-amplifier and a Correlated Double Sampling (CDS) circuitry. The matrix is read out in rolling shutter mode. SUZE-01 [8], a reduced scale prototype chip, incorporates the zero suppression logic, the memory buffers and the serial transmission. The measured Temporal Noise (TN) of MIMOSA22 (the pixel array associated with the discriminators) is about 0.6-0.7 mV, corresponding to ~12 e$^-$, while the Fixed Pattern Noise (FPN) is ~0.3 mV, corresponding to ~6 e$^-$. The detection efficiency is close to 100% up to a threshold value of the discriminators of ~6 times the noise standard deviation (6N), with a fake hit rate below 10^{-4} and a spatial resolution better than 4 µm [6]. These performances were obtained with the 120 GeV/c pion beam at CERN-SPS.

Figure 2 shows the block diagram of MIMOSA26. It features 1152 columns of 576 pixels with a pixel pitch of 18.4 µm, covering a 224 mm^2 wide active area.

The voltage signal induced by the charges collected through an Nwell/P-epi diode is amplified in each pixel by a preamplification stage [5]. The signal from two successive frames is extracted by the clamping technique (in-pixel CDS [7]). In the rolling shutter read-out mode, the 1152 pixel signals of the selected row are simultaneously transmitted to

the bottom of the pixel array where 1152 column-level, offset compensated discriminators perform the analogue-to-digital conversion. A second double sampling, implemented in each discriminator stage, removes pixel to pixel offsets introduced by each in-pixel buffer [7]. In principle, that allows using a common threshold for all discriminators. However, in order to minimise the charge injection coming from the thousands of switches of discriminators during the calibration and the read-out phases, the 1152 discriminators are sub-divided into 4 groups of 288 discriminators. Each group has its own threshold provided by a separate bias DAC.

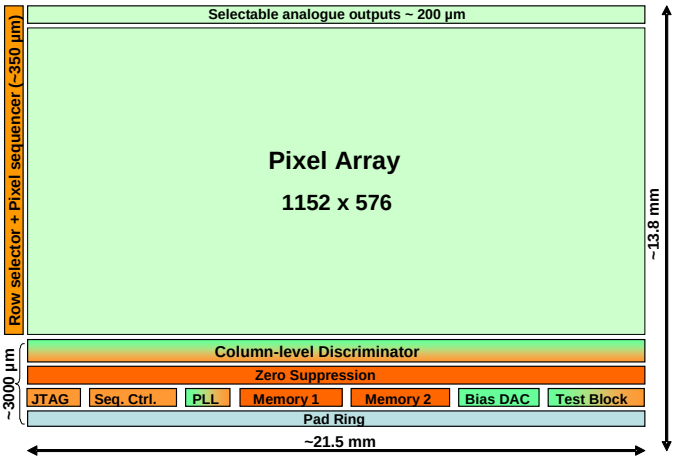

Figure 2: MIMOSA26 block diagram

The discriminator outputs are connected to a zero suppression circuitry [8], organised in pipeline mode, which scans the sparse data of the current row. It skips non-hit pixels and identifies contiguous hit (signals above the threshold) pixels (string). The length and address of the beginning of the strings are stored successively in two SRAM allowing a continuous read-out. A data compression factor ranging from 10 to 1000, depending on the number of hits per frame, can be obtained. The collection of sparsified data for a frame is then sent out during the acquisition of the next frame via (one or) two 80 Mbits/s LVDS transmitters.

An optional PLL module, allowing a high frequency clock generation based on a low frequency reference input clock, and a 8b/10b encoder for high speed data transmition with clock recovering, are implemented in the design. The on-chip programmable biases, voltage references and the selection of the test mode are set via a JTAG controller.

The possibility to test each block (pixels, discriminators, zero suppression circuit and data transmission) is an important aspect of the chip: DfT (design for testability). This capability is implemented in the MIMOSA26 design.

III. Test & Evaluation in Laboratory

MIMOSA26 sensors were tested extensively in the laboratory. The tests were first performed with the analogue part from pixel outputs in order to check the responses of all pixels. Next, the digital outputs were tested, in 4 different configurations:

- 1152 discriminators alone (isolated from the pixel array)
- all discriminators connected to the pixel array
- zero-suppression circuitry alone
- full chain including the pixel array, the discriminators and the zero-suppression logic.

A. *Tests of the analogue part of the pixel array*

The analogue response was studied on 8 different sensors in order to evaluate the pixel noise, the charge collection efficiency and the uniformity of the response over the sensitive area. All sensors exhibited very similar performances.

The result of the pixel noise measurements is illustrated by Figure 3, which displays the noise level of all pixels composing one of the sensors. One can see that the noise is uniformly distributed and that there are no dead pixels. The average noise value amounts to <~14 e^- ENC at a read-out clock frequency of 80 MHz.

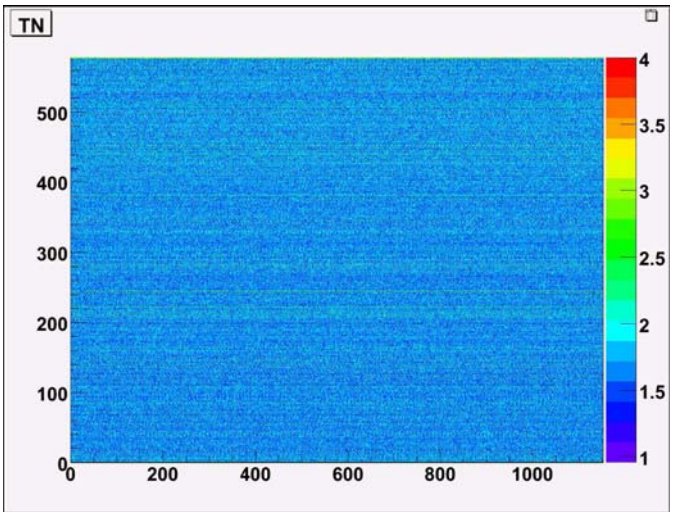

Figure 3: Distribution of the pixel noise of MIMOSA-26 at the nominal frequency (80 MHz).

The charge collection efficiency (CCE) was investigated by illuminating the sensors with a ^{55}Fe source. The CCE was derived from the reconstructed clusters generated by the 5.9 and 6.49 keV X-Rays. The measured values are shown in Table 1, where they are compared to the CCE values observed with MIMOSA22. The latter are well reproduced with MIMOSA26, which validates the extension of the MIMOSA22 pixel design to full scale.

Cluster Size	seed	2x2	3x3	5x5
MIMOSA26	22 %	55 %	73 %	83 %
MIMOSA22	22 %	58 %	75 %	86 %

Table 1: MIMOSA26 CCE measurements compared to those of MIMOSA22.

B. *Tests of the digital part*

The behaviour of the discriminators isolated from the pixel array was studied on 15 unthinned and 6 thinned (~120 µm) sensors. The noise performance was estimated for each discriminator group separately. The measurement consisted in estimating the response of the discriminators to a fixed voltage by raising progressively their threshold.

The outcome of the study is illustrated in Figure 4, which displays the response of a group of 288 discriminators as a

function of the threshold value – S curve. The slope of the transition and its dispersion were interpreted in terms of temporal (TN) and fixed pattern noise (FPN). The TN is ~0.4 mV and the FPN is ~0.2 mV. These results reproduce well the observations made with MIMOSA22 [6], and show that all discriminators are fully operational at nominal read-out frequency.

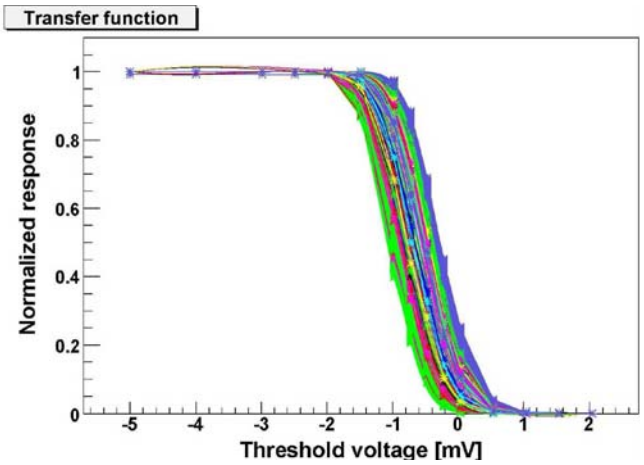

Figure 4: Response of a group of 288 isolated discriminators.

On the next step, the discriminators were connected to the pixel array. The chip response was assessed at 80 MHz (112.5 µs frame read-out time) with the 15+6 sensors mentioned earlier. 4 sensors were also studied at a read-out clock frequency of 20 MHz. The noise measurements performed with isolated discriminators were repeated with each group of 288 connected discriminators. The values observed are shown for one group in Figure 5.

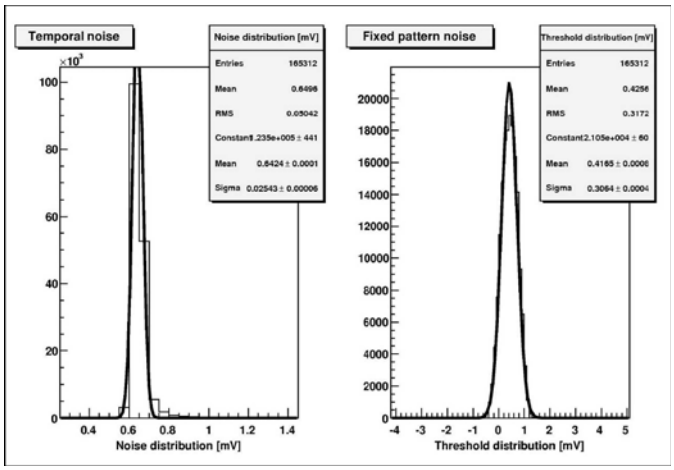

Figure 5: Response of a group of 288 discriminators connected to the pixel array.

The total TN amounts to ~0.6-0.7 mV, which is basically the value of the pixel TN. The total FPN amounts to ~0.3-0.4 mV, which is dominated by the FPN of the 1152 discriminators. These values remain nearly constant when varying the read-out clock frequency from 80 to 20 MHz. The conclusion of the tests at this stage is that the complete array reproduces the performances extrapolated from MIMOSA22 [6].

Next, the zero-suppression logic, disconnected from the rest of the chip, was investigated. Various patterns were emulated with a pattern generator, and ran through the logic millions of times without any error up to frequencies of 115 MHz (i.e. 1.4 times the nominal frequency). All critical configurations, e.g. with strings overlapping two contiguous blocks, were checked repeatedly to be treated properly.

Finally, the signal processing of the complete chain, ranging from the pixel array to the output of the data transmission, was characterised on several different sensors. Their outputs were studied in the absence of any radiation source in order to evaluate the ratio of noisy pixels to all pixels, corresponding to the fake hit rate. The ratio of fake hits is a function of the discriminator threshold. Table 2 summarises the results. One observes that the discriminator threshold values ranging from 5 to 5.5 times the noise value allow maintaining the fake hit rate at a level of 10^{-4} (i.e. < 70 pixels per frame). This result remains essentially unchanged when varying the operation temperature from +20°C to +40°C. It was also checked that multi-hit frames translate into the right output memory patterns.

Discriminator Threshold	4 N	5 N	5.5 N	6 N	8 N	10 N
(Npix>Vth) (10^{-4})	< 8	~1.5	~1	~0.5	0.1	0.03

Table 2: Fake hit rate of a MIMOSA-26 sensor measured as a function of the discriminator thresholds.

Finally, the power consumption of the sensor was measured and found to be ~750 mW for the whole chip. This value agrees well with the one simulated, and corresponds to ~250 mW/cm² and to ~640 µW per column. This latter value reflects consumptions of ~250 µW per pixel and ~350 µW per discriminator.

IV. Beam Test Results

From July to October 2009, MIMOSA26 was operated 3 times on particle beams at the CERN-SPS. Parts of these beam periods were devoted to the integration of the sensors in the EUDET beam telescope, where they are supposed to equip all planes of the final telescope version. Separate beam tests were performed to evaluate the sensor performances.

The tests started with a set of 3 sensors introduced as Device Under Test (DUT) in the EUDET telescope demonstrator. The 3 sensors were operated synchronously and the track reconstruction was running smoothly after only a few days of run. The next step of the EUDET programme consisted in replacing all 6 analogue output sensors composing the telescope demonstrator with MIMOSA26 chips. The complete telescope was commissioned in September 2009 with ~120 GeV/c pions at the CERN-SPS.

Six other sensors, some of them thinned to 120 µm, were combined to build another telescope, which was installed at the CERN-SPS for the sensor assessment. They were operated during about 10 days with ~120 GeV/c pions and their response to the beam particles were studied as a function of the discriminator threshold value.

A discriminator threshold scan was performed, similar to those performed in the laboratory, in order to derive the value of the total noise. The TN was found to be ~0.6-0.7 mV and the FPN was observed to be ~0.3-0.4 mV. These values reproduce well those observed in the laboratory.

Next, the rate of fake hits was determined (at room temperature and at 80 MHz). Table 3 summarises the results for two different sensors, illustrating the spread of the responses between chips. One observes that a threshold slightly above 5 times the noise value allows to keep the fake hit rate in the order of 10^{-4} or below.

Discriminator threshold	5 N	6 N	7 N	8 N	10 N	12 N
Fake rate of chip Nr. 24 (10^{-4})	1.6	0.6	0.24	0.095	0.026	0.017
Fake rate of chip Nr 1 (10^{-4})	3.3	1.2	–	0.23	0.054	–

Table 3: Values of the average fake hit rate due to pixel noise fluctuations as a function of the discriminator threshold.

The characteristics of the noise of the pixel array were studied in some detail in order to evaluate its impact on the occupancy of the zero-suppression logic. Figures 6 and 7 display the number of times each pixel exhibits a noise fluctuation above a threshold of 6 times the average noise (6N) based on ~40,000 frames test without beam.

Figure 6 shows also the distribution of the number of pixels per frame with noise fluctuations above this threshold.

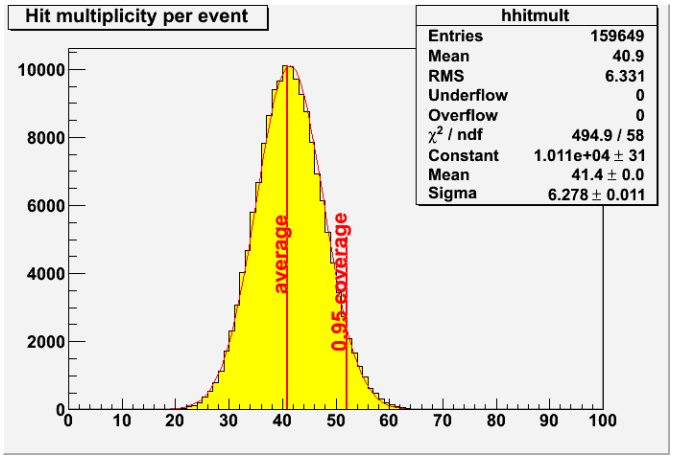

Figure 6: Number of pixels per frame with a noise fluctuation passing a discriminator threshold of 6N.

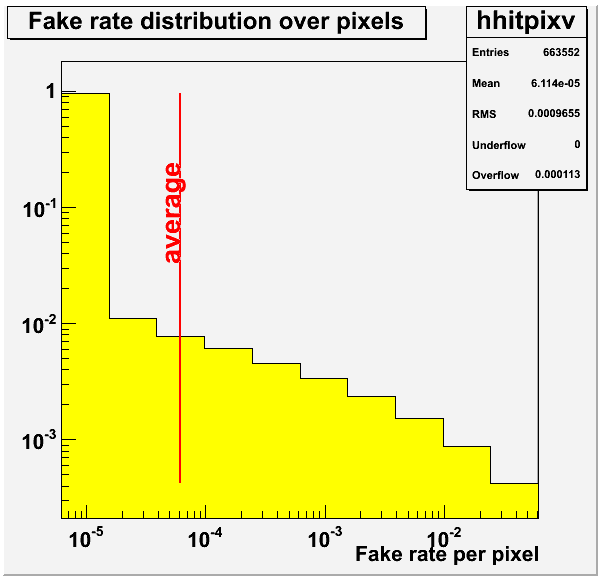

Figure 7: Distribution of fake rate per pixels with a noise fluctuation at the threshold of 6N.

One observes that the average value of fired pixels per frame is about 40. Compared to the total number of pixels composing the sensor (~660,000), this corresponds to a rate of ~0.6x10^{-4}. The noise fluctuations above the threshold follow a Gaussian (more precisely a Poisson) distribution, with a standard deviation equal to the square root of the mean value.

Figure 7 shows whether the noise fluctuations are rather concentrated in a few pixels firing frequently or if they are more distributed among a large number of pixels firing from time to time. One observes that a relatively modest fraction of the pixels generates most of the fake hits. For instance, 0.2 % of the pixels fire at least once every 100 frames due to their noise fluctuation. More statistics needs to be accumulated in order to evaluate in how far these values vary from one sensor to another.

The detection efficiency was evaluated for different threshold values and on different sensors, as well as the cluster multiplicity distribution and the single point resolution. The events collected were triggered with a 7×7 mm² scintillator slab. Good quality tracks were reconstructed through the telescope for ~80 % of the triggers. Figure 8 represents the distribution of the particles' impacts in each of the 6 MIMOSA26 sensors, which gives an image of the beam spot. The correlation between impacts in different planes is clearly visible.

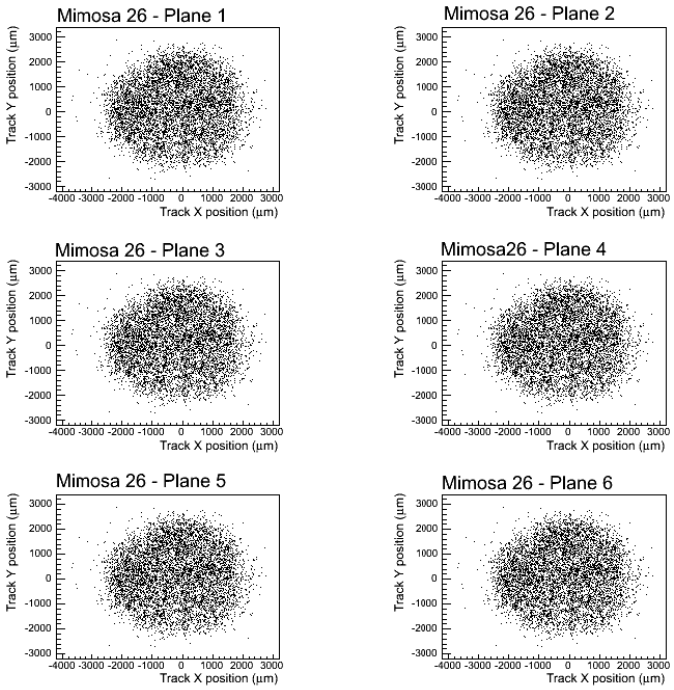

Figure 8: Beam spot derived from about 10^4 beam particle tracks reconstructed through the telescope (6 planes of MIMOSA26).

A detection efficiency of ~99.5±0.1% was obtained for a fake rate of ~10^{-4} (Fig. 9). This very satisfactory performance is however slightly below the one observed with MIMOSA22. Besides the preliminary aspect of the analysis, which may be partly at the origin of the difference, the latter is also suspected to follow from the large number (1152) of discriminators integrated in MIMOSA26, translating into threshold dispersions which are also limiting the sensor performance. Solutions to this feature exist, which will be

implemented in the next real scale sensor, to be fabricated in Spring 2010 for the STAR vertex detector.

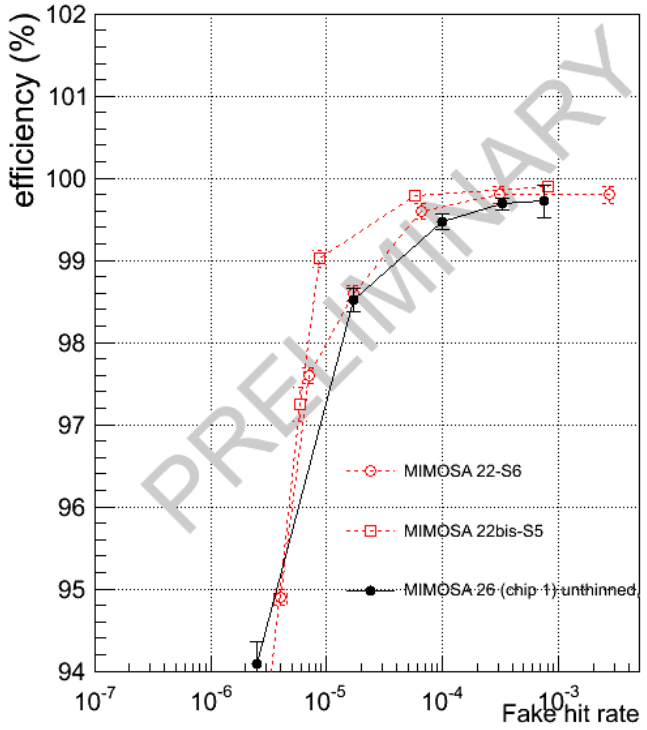

Figure 9: Variation of the detection efficiency with the fake hit rate.

The threshold dependence of the cluster multiplicity was also evaluated. Figure 10 shows the cluster multiplicity for 3 different threshold values.

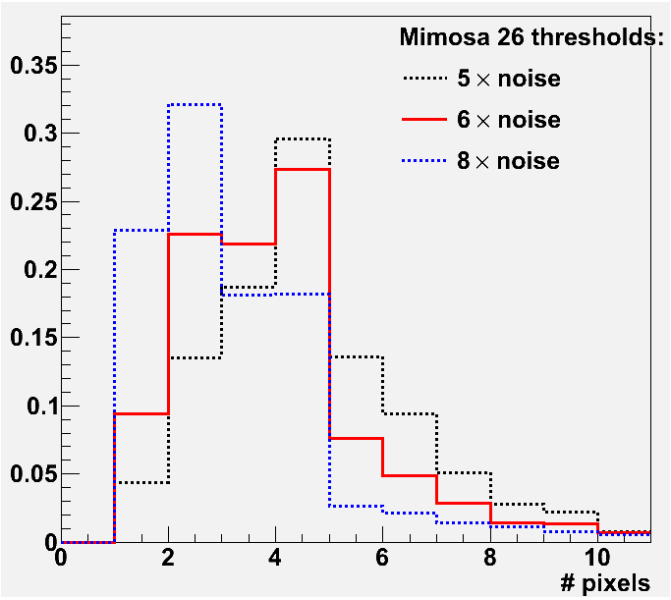

Figure 10: Cluster multiplicity for different threshold values.

Figure 11 summarises the variation of the resolution with the discriminator threshold. Its value varies around 4.5 µm, which is exceeds the values observed with MIMOSA22/-22bis by >~0.5 µm. This feature is not consistent with the observed cluster characteristics of MIMOSA26, which can be considered as identical to those of MIMOSA22/-22bis. The investigation of this inconsistency is still on-going.

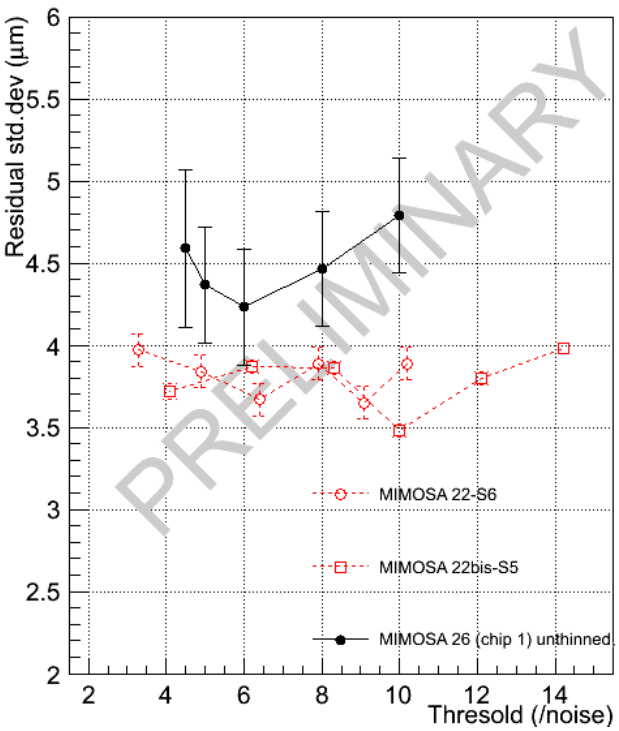

Figure 11: Variation of the single point resolution with the discriminator threshold value.

V. Conclusion & Perspectives

MIMOSA26 is the first reticule size, fast readout, MAPS which integrates on-chip data sparsification for the EUDET beam telescope. The assessment of MIMOSA26 is not yet completed but the preliminary conclusion is that its architecture provides the expected tracking capability needed for this telescope.

The fast readout architecture of MIMOSA26 will serve as base line architecture for vertex detectors of several experiments, such as the STAR Heavy Flavor Tracker (HFT) upgrade. It will also be extended to the CBM Micro Vertex Detector (MVD) (SIS-100) and is proposed for the ILC vertex detector.

VI. References

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