The ATLAS RPC ROD for Super LHC

A. Aloisio, L. Capasso, F. Cevenini, M. Della Pietra, R. Giordano and V. Izzo
Presented by V. Izzo

***Abstract*— The number of interactions per bunch crossing for the upgrade of the Large Hadron Collider is expected to be ten times greater than the actual one. As a consequence, the ATLAS detector for SLHC foresees the use of a larger number of readout channels and also a new trigger level is under development. In order to face with such issue, we developed a new architecture for the Read Out Driver (ROD) for the ATLAS RPC Muon Spectrometer in the barrel region. Presently, each ROD board receives ATLAS RPC Muon readout data and arranges all the data fragments of a sector of the spectrometer in a unique event, sending it to the next acquisition systems. Our new design is based on the new generation Xilinx Virtex5 FPGA and it works with a clock frequency six times greater than the actual bunch crossing rate of the LHC. We also implemented the output channel of the ROD, presently based on S-Link protocol, by using the GTP transceivers inside the FPGA. We present an overview of our design, focusing on the newly added hardware features.**

***Index terms*— Data acquisition, Event building**

ATL-DAQ-PROC-2009-036
18 November 2009

I. Introduction

THE Large Hadron Collider (LHC) is a proton-proton collider which will start operation in Nov. 2009 at *CERN (European Centre for Nuclear Research)* in Geneva, Switzerland. The LHC design [1] foresees a luminosity of 10^{34} cm^{-2} s^{-1}; the protons are grouped in bunches, interacting (*Bunch Crossing*) every 25 ns, with a centre of mass energy of 14 TeV. All these parameters will reach their design value gradually. In the first period of operation, the centre-of-mass collision energy will be around 7 TeV and the bunch crossing time will be 75 ns, with the luminosity expected to be between 10^{29} cm^{-2} s^{-1} and 2×10^{31} cm^{-2} s^{-1}. Then, over several years, the bunch crossing time will be shortened to 25 ns and the centre-of-mass energy will be raised to 14 TeV. Also the number of bunches in the beams will be increased, leading to the design luminosity of 10^{34} cm^{-2} s^{-1} in 2012.

A luminosity upgrade of the LHC is already under development, in order to expand the LHC's discovery potentials and to accumulate enough statistic on the physics researches at the LHC. The upgrade plans of the LHC collider are focused on the main bottlenecks of the proton-injection and accelerator systems, that include elements built in the 50s.

The luminosity upgrade of the LHC is made of two main phases [2]. In the Phase 1 the proton injection system will be modified in order to obtain an expected luminosity of 3×10^{34} cm^{-2} s^{-1}, presumably in 2014. The Phase 2 foresees to reach a luminosity of 10×10^{34} cm^{-2} s^{-1} by 2019, by using a new synchrotron.

Presently, the bunch spacing separation is 25 ns. This value will be still used also in the Phase 1. For the Phase 2, three scenarios are considered. The bunch spacing can be shorter (12,5 ns), remain the same or can be doubled to 50 ns. The pros and the drawbacks of each scenario are still to be investigated.

In the following paragraphs we describe the current layout of the ATLAS experiment and the consequences on it of the LHC upgrade.

II. The Trigger System of the Atlas Experiment

The ATLAS [3][4] experiment has been installed at one of the four LHC's beam interaction points. ATLAS is an "all-purpose" detector that aims to discover the Higgs boson, the missing element of the Standard Model of particles and interactions, and to find evidence of the Super-Symmetric particle theory. The ATLAS apparatus is designed to have almost a 4π geometry around the interaction vertex and it has a cylindrical symmetry along the beam axis; it is made of different sub-detectors, each with its own dedicated read-out electronics. Its inner tracking detector is located inside a 2 T axial magnetic field; outside there is a liquid argon electromagnetic calorimeter and a hadronic calorimeter. In the outer region, the muon spectrometer is instrumented with precision measurement chambers and trigger chambers. The bending magnetic field in the muon spectrometer is generated by an air-core toroid made by 8 coils.

Resistive Plate Chambers (RPC) are used both for trigger and readout purposes in the barrel region. The RPC chambers

Manuscript received November 10, 2009.

Alberto Aloisio (e-mail: aloisio@na.infn.it), Luciano Capasso (e-mail: lcapasso@na.infn.it), Francesco Cevenini (e-mail: cevenini@na.infn.it) and Raffaele Giordano (e-mail rgiordano@na.infn.it) are with I.N.F.N. Sezione di Napoli and Università di Napoli "Federico II", Dipartimento di Scienze Fisiche, Via Cintia - 80126 Napoli, Italy.

Massimo Della Pietra is with I.N.F.N. Sezione di Napoli and Università di Napoli "Parthenope", Dipartimento per le Tecnologie, via Medina 40 – 80133 Napoli, Italy (e-mail: massimo.dellapietra@na.infn.it).

Vincenzo Izzo (e-mail: izzo@na.infn.it) is with I.N.F.N. Sezione di Napoli, Dipartimento di Scienze Fisiche, Via Cintia - 80126 Napoli, Italy.

are arranged in projective towers to form three cylinders concentric with the beam axis and have a 16-fold segmentation in the azimuthal plane, following the eightfold azimuthal symmetry of the magnetic structure. The whole Muon Spectrometer barrel is divided into 32 physical sectors (16 within each half barrel).

In order to reduce the interaction rate from 1 GHz to 100 Hz, the ATLAS trigger has been designed with a three level architecture [5]. The raw rate of 1 GHz proton-proton interactions is reduced to 75 kHz by the Level-1 trigger system [6], that also flags interesting events with a *Level-1 Accept* signal (L1A) generated by the Central Trigger Processor (CTP) with a fixed latency of 2.5 μs.

The ATLAS trigger system is a synchronous system working at the *bunch crossing* frequency of the LHC. All the trigger electronics are driven by a common clock signal, synchronized with the *bunch crossing* frequency of the collider.

Data in each event are associated to a number identifying the bunch crossing that generated the collision (*Bunch Crossing Identifier*, or BCID) and to a unique progressive number (*Event Identifier*, or EVID) identifying that event. *Front End* electronics takes care of associating each event data to the corresponding EVID and BCID. When the trigger processor generates a L1A pulse, the EVID value is incremented. The BCID value is increased every LHC's clock cycle. Both EVID and BCID are managed by counters on the front end boards synchronously to the LHC's clock. In order to initialize and handle these two identifiers (i.e. EVID and BCID), two signals are transmitted: the *Event Counter Reset (ECR)* is issued on request by one of the subsystems of the ATLAS apparatus, if a malfunction has occurred; the *Bunch Counter Reset (BCR)* is transmitted periodically after every orbit, in order to rewind the BCID counters.

The reference clock, the L1A, the ECR and the BCR signals have to be transmitted to the whole detector, over distances up to hundreds meters. In order to allow the synchronization of the DAQ systems with the machine clock, a physical layer has been chosen, able to distribute the clock and control signals to all elements of the ATLAS apparatus, with programmable *skew* and low *jitter*. This is made by the *Trigger Control System* (TCS) [7] and the *Timing Trigger and Control* (TTC) system [8].

All these signals are coded and optically transmitted, over a tree structure. At the destination, the receiver board TTCrq [9] reconstructs the signals and adapts them to the protocols of every sub-detector.

III. The ATLAS Muon RPC Read-Out System

The ATLAS muon trigger and RPC readout system is split between on-detector and off-detector sections. The level-1 muon trigger in the barrel region is based on a fast geometric coincidence [10] between different planes of the RPC detectors. On-detector electronics carry out the trigger algorithm every 25 ns and forward the event data to the Central Trigger Processor across optical fibre.

During the decision time of the CTP, with a fixed latency of 2.5 μs, data produced by the RPC detectors are kept in *FIFO* memories on the *on-detector* electronics. If an event is accepted by the first level trigger, a *L1A* pulse is generated and transmitted across the TTC system together with the pertinent EVID and BCID. After the arrival of the L1A pulse, data stored in the *FIFO* buffers are transferred to the off-detector electronics over the same optical link used to transmit trigger information. Trigger and read-out data of each of the 32 sectors of the spectrometer are managed by a *Read Out Driver* (ROD) crate (see fig.2).

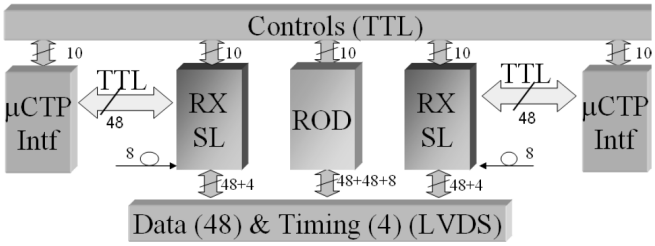

Fig. 2. Scheme of the crate that hosts the ROD board.

Each *RX-SL* board receives and elaborates trigger and *read-out* data from the on-detector electronics. The *RX/SL* boards pre-process the trigger information and sent them to the Trigger Processor through an interface to the Muon Central Trigger Processor Interface board (μCTPI) [11], across a custom backplane. The *RX/SL* boards also arrange readout data in an event frame (*RX Frame*) and transmit them to the adjacent *Read Out Driver* across the custom backplane *RODbus* [12] via a high speed serial link.

The main task of the ROD is to perform a further framing of the readout data received from the two adjacent *RX/SL* boards. Each ROD board manages the read-out data of a whole sector of the spectrometer: data are arranged in a ROD frame and are transmitted across the optical link S-Link to the next acquisition levels, i.e. to the *Read Out Systems* (ROS). The ROD also manages the timing signals of the trigger and DAQ system. For this purpose, the ROD hosts a TTCrq receiver module from which it receives the ATLAS' timing and control signals to be forwarded to the *RX/SL* boards on the *RODbus*.

On the *RODbus*, data and timing signals are transmitted in LVDS standard in order to achieve high rate, low *skew* and *jitter*. The transmission is performed by the National DS90CR483-484 Serializer-Deserializer chip-set [13], that can transmit up to 48bit at 40 MHz, by using 8 serial links and a DC balance scrambling code. The serial links between each *RX/SL* and ROD have an aggregate bandwidth of ~ 2,2 Gbit/s. Control signals run at lower rate and are transmitted using the TTL standard. The *RODbus* also hosts a 48-bit TTL

bus that allows the *RX/SL* boards to transmit trigger data to the µCTPI boards.

IV. The Read Out Driver Board

The ROD (Fig. 3) is a VME 64X 6U board, equipped with two VIRTEX II XILINX FPGAs, labelled as *VME FPGA* and *ROD FPGA*. The board also hosts an ARM7 microcontroller, the TTCrq receiver, the S-Link transmitter and the two deserializers (*RX SerDes*) that receive data via *RODbus* backplane from the *RX/SL* boards. A complete description of the ROD board is given in [14].

The ROD board is interfaced with the *VMEbus* by the *VME FPGA*; the *VME FPGA* allows a user to access the *ROD FPGA* memory locations and configuration registers and to read the microcontroller's data. The *VME FPGA*'s 80 MHz clock is obtained from an on-board 40 MHz oscillator multiplied by 2 by the internal Digital Clock Manager.

The *ROD FPGA* performs the *event building* algorithm on the *read-out* data transmitted by the *RX/SL* boards. The ROD FPGA also hosts registers for the configuration and monitoring of the event builder engine. In the same fashion as the *VME FPGA*, the *ROD FPGA* clock is obtained multiplying by 2 the 40 MHz board clock.

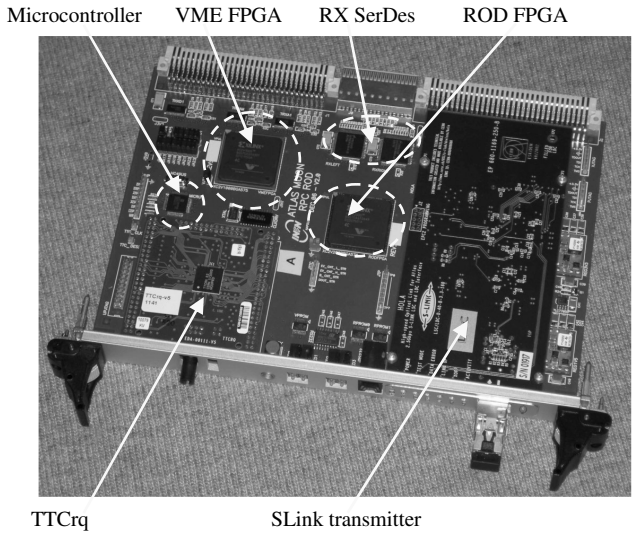

Fig. 3. A photo of the ROD board.

The *ROD FPGA* communicates with the *VME FPGA* via a serial synchronous custom protocol, carried out by two point-to-point unidirectional lines with a data rate of 80 Mbit/s. The *VME FPGA* is the *Master* of the serial link, managing both the write (for data and for address) and read operations. The protocol requires that the clocks of both the FPGAs are synchronous each other: this has been obtained by using a calibrated clock tree on the PCB and an appropriate configuration of the DLLs inside FPGA [15]. The main advantages of a serial link are a simpler PCB layout, the use of a small number of FPGA pins and limitations of *ground bounce* effects.

The *ROD FPGA* receives 32-bit words and the recovered 40 MHz clock from each *RX SerDes*. Each *SerDes* channel can sustain an aggregate bandwidth of 1,280 Gbit/s, but the *SerDes* channels are not fully loaded and presently an average bandwidth of ~ 200 Mbit/s is used. With the present ATLAS design parameters, the maximum input bandwidth is ~ 560 Mbit/s per channel.

The ROD FPGA is interfaced with the TTCrq module - from which it receives the TTC timing signals and the 40 MHz LHC's clock - and to the S-Link transmitter, that is fed by a 40 MHz clock derived by the 80 MHz internal clock. The S-Link module is a HOLA [16] ATLAS Readout link: it is based on the TLK2501 chip and the total bandwidth of the readout channel is 1,280 Gbit/s.

The ROD board is the meeting point of trigger signals and different readout data streams from the Muon Barrel Spectrometer. Besides the internal 80 MHz FPGA clocks, the 40 MHz LHC clock, the two 40 MHz SerDes clocks and the 40 MHz S-Link clock run all over the board. Even if these clock signals have the same frequency, they have an unpredictable phase relationship and should be handled as domains asynchronous to each other. All these clocks are present in the *ROD FPGA*, which is the most complex and critical section of the board. In order to decouple the clock domains and to guarantee their coexistence on the *ROD FPGA*, FIFO memories have been extensively used.

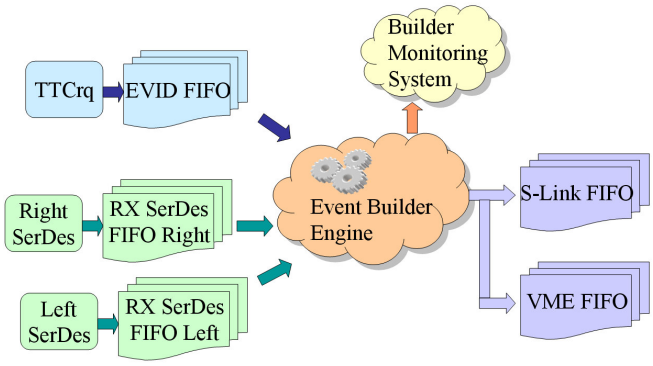

Fig. 4. The Data Flow of the Event Builder Engine.

The dataflow of the *Event Builder* Engine is shown in Fig. 4. EVID data from TTC are stored in the EVID FIFO. Input data (coming from a specific *RX/SL* board) are stored in the corresponding FIFO (RX SerDes FIFO). *Event Builder* output data are stored in the S-Link FIFO and then read out by the S-Link transmitter and sent across the optical link to the ROS. The Builder Monitoring System [17], based upon an embedded microprocessor with real-time performance, analyzes the *Event Builder Engine* behaviour and presents on an ASCII display the acquired data, arranged as bar charts or plots.

The *Event Builder Engine* builds a *ROD Muon Frame* that is compliant with ATLAS format specifications [18]. The frame starts with a *ROD Header* (belonging to a specific EVID value), includes as a payload the frames coming from the *RX/SL* boards and ends with a *Footer* containing status and error flags as shown in Fig. 5. The *Event Builder Engine* has a FIFO-based pipelined architecture that runs with the ROD FPGA 80 MHz clock.

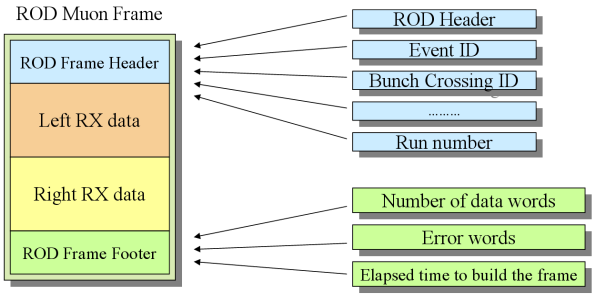

Fig. 5. ROD Data fragment produced by the *ROD FPGA* engine.

The bubble diagram of the main Finite State Machine (FSM) of the *Event Builder Engine*, called *Frame Maker*, is shown in Fig. 6. As each *ROD Muon Frame* belongs to a specific EVID value, the *Event Builder Engine* is EVID triggered, i.e. it starts writing a Frame only when an EVID is available. For this reason, the *Frame Maker* starts by checking the *empty* flag of the EVID FIFO and waits for an EVID value to be processed.

When an EVID value is available from the EVID FIFO, the *Frame Maker* starts writing a valid header in the output S-Link FIFO. The ROD Frame *Header* contains nine control words, such as the *Start of Frame*, the board ID code and information about the current EVID and BCID values. After writing the Frame Header, the *Event Builder* Engine waits for data arriving from the *RX/SL* boards.

The received RX Frames are checked in order to find a *Header*. If the RX Frame is correctly formatted and the embedded EVID and BCID values match with the ones from the TTC, the frame is appended to the ROD Frame. The ROD *Event Builder* doesn't check the payload of the RX frames: it only checks the total length.

The ROD frame is then closed by a *Footer*, written by the *Frame Maker*. The ROD Frame Footer contains status words, error flags, the total count of the words in the Frame and the time needed to build the frame. Then, the *Event Builder* Engine restarts and waits for the next EVID value.

Using the Builder Monitoring System, we studied the *Event Builder* timing performance in the commissioning phase of the ATLAS experiment with cosmic rays. We come to the conclusion that time needed to cast header and footer in the ROD Muon Frame is less than the 3% of the average time available between two triggers. On average, the building of the frame core takes 30% of the time between two consecutive triggers, such that the logic is IDLE for nearly 70% of the time.

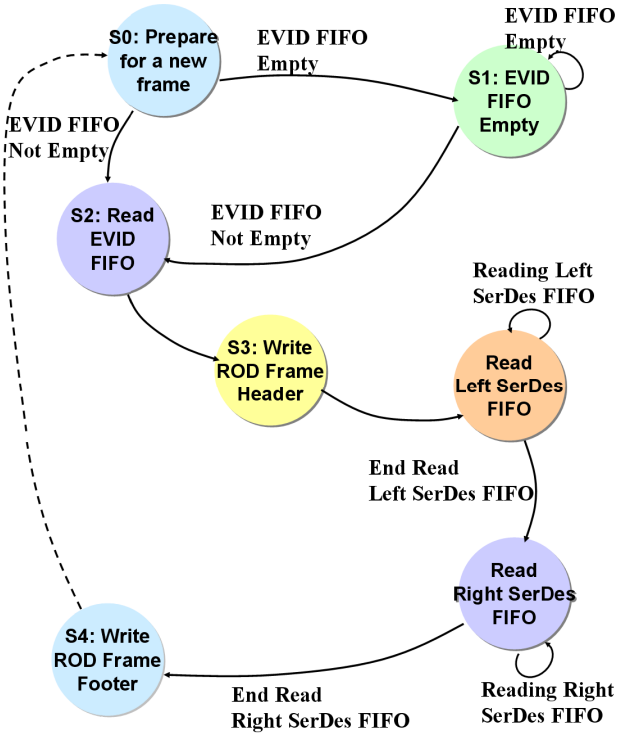

Fig. 6. Bubble diagram of the main Finite State Machine (FSM) of the *Event Builder Engine*

V. ATLAS AND THE LHC UPGRADE

The luminosity upgrade plans of the LHC will have considerable consequences on the ATLAS experiment, both on the detector side and on the trigger and DAQ systems.

The luminosity increase foreseen for the LHC upgrade leads to a corresponding increase in the mean number of interactions per bunch crossing. Depending on the different phases of the upgrade, this number can span a range from the present ~ 27 up to almost 1500 interactions per bunch crossing, leading to a more intense particle production and a higher background. The main consequences of this increase in particle production is that the various detector are not able to sustain such an intense flux of particles. Thus, newer detectors have to be designed and developed, in order to manage the higher rate of particles. For the muon spectrometer, some R&D projects are under evaluation, that foresee the use of an additional RPC station or the employment of micro-pattern gaseous detectors like MicroMegas or GEM. The main consequence of the use of these new detectors is the increase of readout channels,

bandwidth and event size, that have to be managed by the DAQ system.

Moreover, the trigger system has to be changed, in order to handle the huge amount of information coming from the detector and to correctly process the different requests of data validation. The present trigger upgrade plans are focusing on complicated trigger selection algorithms and pile-up handling. Probably, the three level trigger architecture will be changed by introducing another trigger level (the L1,5 trigger) in order accept or reject events with more accuracy [19].

VI. The ROD Board Upgrade

Starting from the present upgrade plans on the ATLAS trigger and DAQ system, the present ROD architecture has some elements that can suffer from the request for a higher bandwidth and a higher data processing capability.

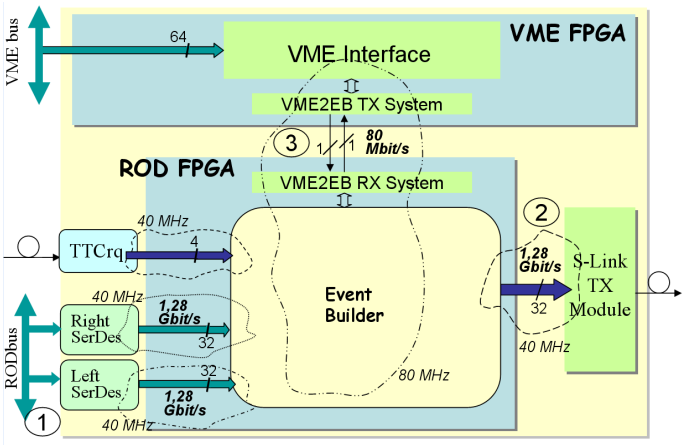

Fig. 7. The present layout of the ROD board.

Fig.7 shows a simplified layout of the present ROD board. In the present ROD board design, the elements that could have potential problems, due to the high performance requests, are listed below:

1) The two SerDes channels
2) The S-Link output channel
3) The communication channel between VME FPGA and ROD FPGA
4) The Event Builder Frequency
5) The working frequency of the Internal FIFOs

The first three elements of the list are also labelled on fig.7 for clarity reasons.

For these reasons, we are currently re-designing the ROD board, giving a particular care to the architecture of *Event Builder Engine* inside the ROD FPGA and to the increased bandwidth requests, needed at the board's Input and Output.

The increasing requirements of high performance forced us to use the state-of-art FPGA technology. We performed a feasibility study, based on the evaluation of multiple implementations and simulations, using a XILINX VIRTEX 5 FPGA [20] device as a benchmark. We propose a solution that could solve the bandwidth and data processing capability potential problems due to the ATLAS upgrade.

The main advantages in the use of a VIRTEX 5 device, in substitution of the VIRTEX II FPGA, are that the VIRTEX 5 offer a large amount of RAM blocks, a greater number of logic resources (~ 30000 vs. 10000 equivalent gates) and the Rocket I/O high speed serial links. Moreover, VIRTEX 5 has a dedicated logic in the RAM blocks that allows the user to easily implement high-speed FIFO modules (so-called Built-In FIFO); it also offers a network of high-speed clock trees, thus allowing to design a circuit architecture running at high clock frequency.

The Rocket I/O GTP transceivers are without doubt the main benefit that we obtained by changing the FPGA devices, because the GTP can be used in the communication with the RX/SL boards, in the communication between the VME FPGA and the ROD FPGA and in the emulation of the S-Link protocol.

VII. The GTP Transceiver

The serial links we will discuss in the next section are all based on the so called GTP transceiver [21] of the Xilinx Virtex 5 FPGA family. Inside the FPGA, GTPs are available as configurable hard-macros (or "tiles"). Each tile includes a pair of transceivers, which share some basic components, like a Phase Locked Loop (PLL) and the reset logic. Fig. 8 shows the architecture of the transmitter (Tx) and the receiver (Rx) included in each transceiver. We will now concisely present the features of the GTP essential to our work. More details can be found in the user guide.

The Tx consists of a Physical Medium Attachment (PMA) sublayer and a Physical Coding Sublayer (PCS), the first one works in a high-speed (~ 1 GHz) clock domain while the second one includes three low speed (~ 100 MHz) clock domains. Two of these are input clocks (TXUSRCLK and TXUSRCLK2), while the third (XCLK) is internally generated by the PLL. The PLL requires a reference clock (CLKIN), whose frequency is a sub-multiple of the bitrate (or "line-rate").

The GTP supports line rates from 100 Mb/s to 3.75 Gb/s. An integrated 5x digital over-sampler is used for rates between 100 Mb/s and 500 Mb/s. The device can serialize/deserialize input words with a width of 8, 10-bit (single-width) and 16, 20-bit (double-width). The FPGA Interface logic reads data from the fabric on the TXUSRCLK2 clock edges and outputs it synchronously with the TXUSRCLK clock. In double width modes, the interface splits input data into 8 or 10-bit words and the TXUSRCLK frequency is twice the TXUSRCLK2 frequency. In single-width modes, the interface simply transfers the input to its output. Data is then 8b/10b encoded, if requested, and it is

transferred to a First In First Out (FIFO) buffer. The latter allows safe data transfers between the TXUSRCLK domain and the XCLK domain. In some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset. The FIFO can be bypassed if the offset is sufficiently small and in fact the device offers a phase alignment circuit in order to minimize it. In the XCLK domain, data is serialized by the Parallel In to Serial Out (PISO) block, whose output is synchronous with the high-speed serial clock.

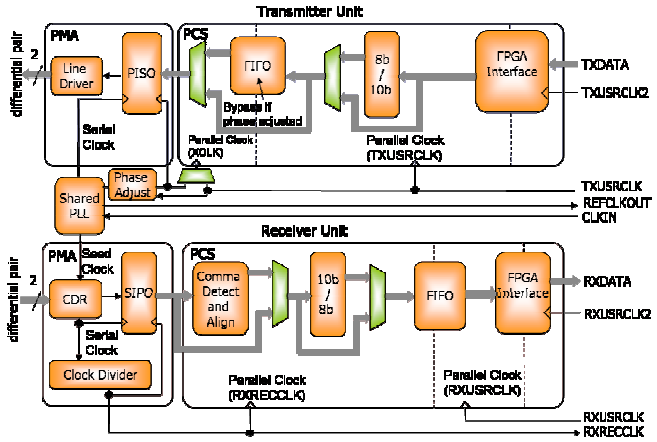

Fig. 8. Architecture of transmitter (top) and the receiver (bottom) inside a transceiver.

On the GTP receiver unit, the serial stream from dedicated FPGA pins is received by the Clock and Data Recovery (CDR) circuit, which extracts a clock and uses it to sample the data. The extracted clock is divided to generate a recovered clock (RXRECCLK) for the Serial In to Parallel Output (SIPO) and for the PCS. The recovered clock can also be used for the receiving FPGA logic. The Comma Detect and Align block following the SIPO can be programmed to search for a specific symbol (e.g. an 8b/10b comma) and automatically align it to the word boundary. Data is 10b to 8b decoded, if needed, and transferred to a FIFO in order to enter the RXUSRCLK domain. If the device has been configured to work with double-width words, the FPGA interface de-multiplexes single-width words from the RXUSRCLK domain and outputs double-width words in the RXUSRCLK2 domain at half of the frequency.

VII. Implementation of Serial Communications

In the new architecture of the ROD, the connections for the RODbus, the inter-FPGA communications and the S-Link module will be based on GTP transceivers. Since all the communications we have to implement are synchronous, in order to minimize the latency through the channel we will skip the FIFOs on the transmitters and use their phase align circuits instead.

As far as it concerns the RODbus, the present 8 lanes could be replaced by just 1 GTP-based serial connection running at 3 Gbps. By using the 8b/10b coding, the actual bandwidth for payload transmission will be 2.4 Gbps.

Supposing to keep the same number of lanes on the new implementation, the new aggregate bandwidth will grow to 19.2 Gbps. Since the GTP supports channel bonding, it will be possible to align the timing of serial streams on different lanes. Moreover the SerDes FIFOs, which now consume logic resources of the fabric, will be replaced by the internal Rx FIFOs of the GTPs.

The whole HOLA module will be replaced by logic implemented in the FPGA fabric encoding parallel data according the S-Link protocol. A GTP configured to work with 16-bit words and 8b/10b encoding will be used in place of the TLK2501 SerDes. Our S-Link emulator will be able to transmit serial data at a maximum data-rate of 3 Gbps and therefore will be potentially faster than the present S-Link module.

The bidirectional communication between the ROD FPGA and the VME FPGA can be implemented by means of a pair of GTP transceivers (one in each device). For instance, each GTP could encode 16-bit incoming words clocked at 10 MHz according to the 8b/10b protocol and serialize them at 200 Mbps over a couple of differential pairs. There will be no more the need for a phase alignment of the clocks of the two FPGAs. On the contrary, each transceiver will transfer data to the fabric on the clock edge of the hosting FPGA. In fact, the internal FIFOs will absorb phase differences between the recovered and the received clocks.

VIII. Implementation and Simulation

Fig. 9 shows the simplified layout of the new ROD board, with the use of the GTP modules in the communication on the RODbus, in the emulation of the S-Link protocol and in the inter-FPGA communication.

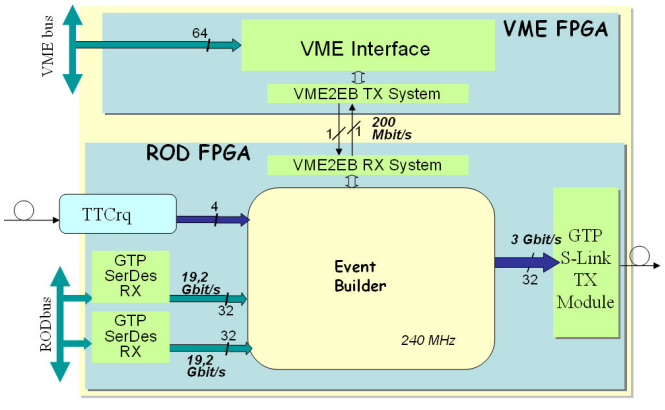

Fig. 9. The new layout of the ROD Board with the GTP modules.

We implemented the present ROD *Event Builder Engine* design in a VIRTEX 5 xc5vlx50t device, installed on a Xilinx evaluation board [22], that allowed us an easy setup of our benchmark test. We choose the VIRTEX 5 xc5vlx50t FPGA because it has an optimal trade-off between logic resources, cost and package complexity. During the implementation, we specifically required a synthesis and a routing optimization for design speed, resulting in the use of only the 18% of the logic resources. The timing analysis of the *Event Builder Engine* design shows that the working frequency can be pushed up to 240 MHz, three times the presently used frequency.

The difference between the two solutions, i.e. between a Virtex II based solution and a Virtex 5 based design, is summarized in Table 1, that shows all the main benefits that can be obtained in a re-design targeted on a Virtex 5 device.

	VIRTEX II based solution	VIRTEX 5 based solution
Event Builder Max. frequency	80 MHz	240 MHz
SerDes Bandwidth on RODbus	2.28 Gbit/s	19.2 Gbit/s
S-Link Bandwidth	1.28 Gbit/s	3 Gbit/s
VME FPGA – ROD FPGA channel BW	80 Mbit/s	200 Mbit/s
FPGA Occupancy	31%	18%

Table 1. Summary of the main benefits in the migration of the present ROD device from a Virtex-2 to a Virtex-5 device

The efficiency of the migration to a VIRTEX 5 based *Event Builder* re-design is clearly visible in fig. 10. Such figure shows, on the left, the layout of the present ROD FPGA (i.e. a Virtex II based design) and, on the right, the layout of the Upgraded ROD FPGA, based on a VIRTEX 5 device.

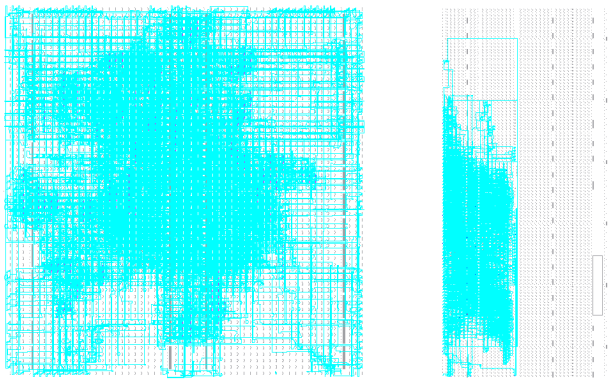

Fig. 10. The resources occupancy of the present ROD FPGA (left) and of the Upgraded ROD FPGA (right) .

VIII. Conclusions

We presented a new design of the ATLAS Muon RPC ROD board, based on the new generation Xilinx Virtex5 FPGA.

In the first part of the paper, we described the changes, in terms of event size and bandwidth requests, that will affect the ATLAS DAQ system as a consequence of the LHC machine upgrade plans. Then we identified the main potential problems that can appear on the ROD board, due to the LHC upgrade.

We proposed a ROD board upgrade, in order to give a solution to the main potential bottlenecks foreseen for the ATLAS upgrade DAQ system. In particular, we performed a feasibility study, based on the evaluation of multiple implementations and simulations, using a XILINX VIRTEX 5 FPGA device as a benchmark. We finally present a comparison between the present ROD Event Builder Engine and the proposed one. The main benefits are due to the availability of the GTP Rocket I/O transceivers, to the use of new high performance FIFO modules and a network of high-speed clock trees.

Our study shows that the state-of-art FPGA devices offer a considerable increase in data transfer bandwidth. The FPGA occupancy is lowered from 31% to 18%. The timing analysis tools show that the *Event Builder engine* on a new FPGA could work with a clock frequency six times greater than the actual bunch crossing rate of the LHC.

Our conclusion is that a new FPGA device, such as a Virtex 5 or newer, is a potential good candidate for implementing the *Event Builder Engine* for the spectrometer ROD board for the upgrade of the ATLAS experiment.

References

[1] D. Bortoletto, "*The ATLAS and CMS Plans for the LHC Luminosity Upgrade*", presented at the "Hadron Collider Physics Symposium (HCP2008)", Galena, IL (USA), September 2008. arXiv:0809.0671v1

[2] M. Nessi, "*The detector upgrade and upgrade scenarios*", presented at the "ATLAS Upgrade "ROD" Workshop", CERN, Switzerland, June 2009. [Online] Available: http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=59209

[3] ATLAS Collaboration, *ATLAS detector and physics performance – Technical Design Report – Volume I, May 1999*.

[4] ATLAS Collaboration, "*The ATLAS Experiment at the CERN Large Hadron Collider", Journal Of Instrumentation, Volume 3, August 2008*. doi: 10.1088/1748-0221/3/08/S08003

[5] ATLAS Collaboration, *Level-1 Trigger Technical Design Report, June 1998*.

[6] G. Aielli et al., "*The Level-1 Trigger Muon Barrel System of the ATLAS experiment at CERN", Journal Of Instrumentation, Volume 4, April 2009*. doi: 10.1088/1748-0221/4/04/P04010.

[7] J. Varela, "*Timing and Synchronization in the LHC Experiments*". Presented at the "Sixth Workshop on Electronics for LHC Experiments", CERN/LHCC/200-041 [Online] Available: lebwshop.home.cern.ch/lebwshop/LEB00_Book/plenary/varela.pdf

[8] B.G. Taylor, "*TTC distribution for LHC detectors*", *IEEE Trans. Nuclear Science*, Vol.45, 1998, pp. 821-828

[9] J. Christiansen, A. Marchioro, P. Moreira and T. Toifl, "*TTCrx v3.0 Reference Manual*", CERN / EP /MIC, Oct. 1999, [Online] Available http://ttc.web.cern.ch/TTC/TTCrx_manual3.0.pdf

[10] V. Bocci et al., "The Coincidence Matrix ASIC of the Level-1 Muon Barrel Trigger of the ATLAS Experiment", *IEEE Trans. Nuclear Science*, Vol.50, no.4, 2003

[11] G. Schuler, *The MICTP Module of the Muon-CTP-Interface Demonstrator User's Guide*. ATLAS Internal Note ATL-DA-ER-0017, version 1.1, June 2006
[Online] Available: https://edms.cern.ch/file/340643/1/mictp.pdf

[12] A. Aloisio et al., *"A multi Gbit/s backplane for the RPC DAQ and L1 Trigger of the ATLAS Muon Spectrometer", Journal Of Instrumentation, Volume 4, July 2009*.
doi: 10.1088/1748-0221/4/07/P07015

[13] *DS90CR483 / DS90CR484 48-bit LVDS Channel Link SER/DES datasheet*. [Online] Available:
http://www.national.com/ds/DS/DS90CR483.pdf

[14] A. Aloisio, F. Cevenini M. Della Pietra, and V. Izzo*, "The Read-out Driver for the RPC of the ATLAS Muon Spectrometer", IEEE Trans. Nucl. Sci. 55 (2008) 265.*

[15] Xilinx Application Note XAPP 132*, "Using the Virtex Delay-Locked Loop"*

[16] CERN, *HOLA High-speed Optical Link for Atlas*, [Online] Available: http://hsi.web.cern.ch/HSI/s-link/devices/hola/datasheet.pdf.

[17] A. Aloisio, L. Capasso, F. Cevenini M. Della Pietra, and V. Izzo*, "Monitoring the Event Building Features of the ATLAS RPCs ROD with an Embedded Microprocessor", Proceedings of the 16th IEEE Real Time Conference, Beijing May 10-15, 2009.*

[18] A. Anjos et. al., "*The raw event format in the ATLAS Trigger & DAQ*", ATLAS EDMS note ATL-D-ES-0019, 2009

[19] N. Gee, "*Level-1 Trigger Scenarios*", presented at the "ATLAS Upgrade "ROD" Workshop", CERN, Switzerland, June 2009.
[Online] Available:
http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=59209

[20] Xilinx UG190*, "Virtex-5 FPGA User Guide",* UG190 (v.5.1), September 2009,
[Online] Available
http://www.xilinx.com/support/documentation/user_guides/ug190.pdf

[21] Xilinx UG196*, "Virtex-5 FPGA RocketIO GTP Transceiver, User Guide",* UG196 (v.2.0), June 2009,
[Online] Available
http://www.xilinx.com/support/documentation/user_guides/ug196.pdf

[22] Xilinx UG347, "*Virtex-5 LXT FPGA ML505 Evaluation Platform User Guide*", UG347 (v.3.1.1), October 2009,
[Online] Available:
http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf