The VELO High Voltage System Control Software

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1 Introduction

The Vertex Locator (VELO) [1] high voltage system requires powerful, flexible and reliable software that is easy to maintain. Moreover, LHCb uses a distributed control system which allows inter-process communication between processes running on several different PCs. The software that was chosen for LHCb, hence the VELO high voltage system, is PVSS [2]. An overview of the HV control system is given in section 2. The PVSS architecture for the HV system is presented in section 3. Section 4 provides a description of the structure of the HV control software. PVSS has the following advantages:

- Powerful commercial product which supports distributed systems and includes tools for object-like device description, archiving, alarms, user-created panels and scripts.
- It is a Supervisory Control and Data Acquisition [3] (SCADA) framework and is used to connect to hardware (or software) devices, acquire the data they produce and use it for their supervision, i.e. to monitor their behaviour and to initialize, configure and operate them. Data structures have very flexible formats that can be exchanged between servers and clients; data can be sent on request or by subscription.
- Provides an object-like data structure called 'data points' created to model the complexity of devices and data structures in the experiments. Data points are instances of these objects and can easily be created in large numbers as needed by the application. One can create an object of data points type that can be instantiated for each hardware item (an example is an actual online value of the voltage in one channel).
- A PVSS 'manager' is available which permits exchange of data by a very simple mechanism between data points in PVSS and other processes running on different PCs.
- PVSS is the control system chosen for the LHC experiments. The Joint Controls Project [4] (JCOP) is part of the CERN IT/CO group and is a collaboration between the experiments and CERN support groups. JCOP has developed many commonly needed tools: a framework, interfaces to hardware devices, configuration tools, etc. PVSS 3.8 is used with the JCOP framework to control the ISEG[a] high voltage power supply modules and crate. An ISEG Object linking and embedding Process Control (OPC) server provides interface between the high voltage power supplies and PVSS.

The LHC experiments will be operated as Finite State Machines (FSM) [5]. The FSM will then ensure that, for example, the high voltage state of a sub-detector is appropriate depending on operational mode. The crate and each high voltage channel will therefore be part of the VELO FSM architecture (see section 5). The HV errors and alarms (see section 6) are handled at the FSM level.

2 Overview of the High Voltage Control System

As shown in figure 1, the control of the high voltage system starts from a PC where PVSS is installed and to which the ISEG power supplies and crate are connected. Then, the ISEG modules control their individual channels to supply the desired voltage. Each bias voltage will pass through the counting house cable, then the counting house patch panels. The long distance cables distribute it to the detector patch panels onto the corresponding repeater board. That repeater board then supplies the bias voltage to the corresponding VELO hybrid, hence the corresponding sensor.

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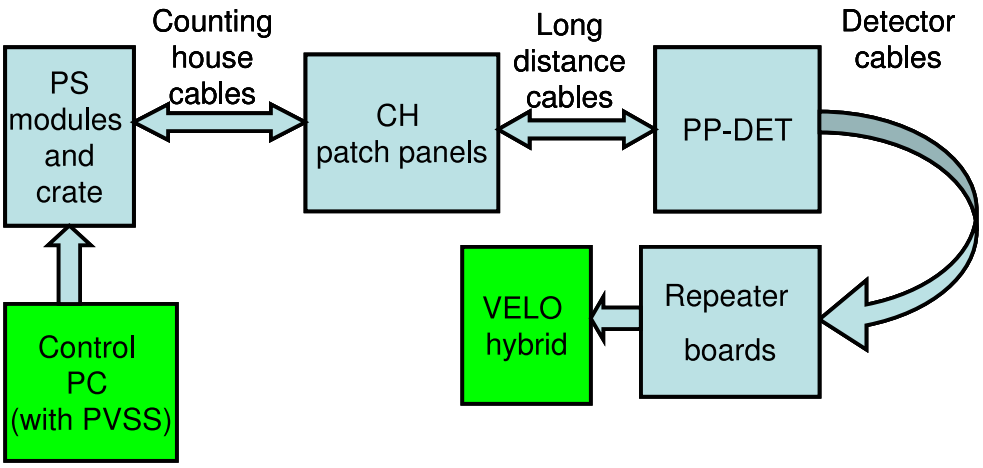

Figure 1 Overview of the high voltage system control.

3 PVSS Architecture

The control systems that are built with PVSS are composed of communicating and independent processes. These processes are called 'Managers'. As shown in figure 2, the main PVSS managers are as follows. The central part is called the Event Manager (EM). It retains all data in a volatile memory, responds to notification of data change and computes alarm conditions. Their values are held in structures called Data Points. The event manager of the VELO HV sytem is called the VELO Detector Control System High Voltage, also known as 'VEDCSHV project'. The database where non-volatile data such as system definitions, alert occurrences and latest values are stored, is managed by the Data Manager (DM). An Oracle database is used for the long term storage of data point values. The visualization of the data points values are ensured by User Interface (UI) managers such as synoptic panels, alarm screen (AES) and trend graphs (Trnd). The interconnection between individual PVSS systems that forms a distributed system is conducted by the Distribution Manager (DIM). The list of PVSS managers provided previously is not exhaustive. Managers could be created depending on its specific task (e.g the ISEG HV Manager is an interface to the HV modules and crate).

4 Structure of the High Voltage Control Software

This section describes the structure of the HV control software (see figure 3). The VELO high voltage system is controlled remotely via PVSS. The PVSS VELO high voltage project VEDCSHV runs on an online[b] PC called 'VEDCS01W' which is located in the counting house. The high voltage control software is able to control individual high voltage channels. Since the VELO has two halves, the part with $+x$ coordinates is referred to as the A-side and the one with $-x$ coordinates to as the C-side, based on the LHCb coordinate system[c] The VEDCSHV project is divided into three sub-systems called 'VELO_HV' for controlling the whole VELO, 'VELOA_HV' for controlling the A-side of the VELO, and 'VELOC_HV' for controlling the C-side of the VELO. The PVSS 'VEDCSHV FSM' was developed specifically for the VELO. This communicates to the PVSS ISEG framework. The PVSS ISEG framework is developed for all CERN users of ISEG power supplies. The PVSS ISEG framework communicates with the ISEG OPC Client[d]. The ISEG OPC Server is provided by the ISEG company. The version of

[b]Online refers to the private network which is used at the LHCb experiment area. The network is protected behind a strong firewall.

[c]The LHCb coordinate system is a right handed system with positive z running along the beam-line away from the interaction point and positive y 'upward'. Positive x points toward the cavern access and away from the LHC cryogenics.

[d]The OPC Client is the application which is interactively connected to the OPC server. It ensures the communication between PVSS and the OPC server.

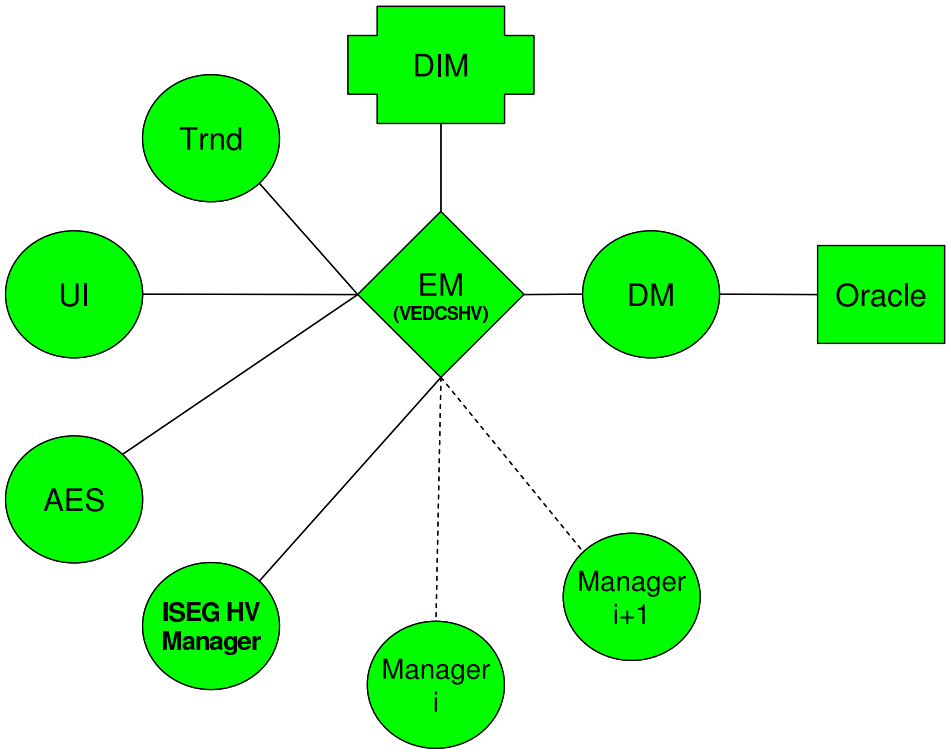

Figure 2 Representation of the architecture of PVSS.

the OPC Server currently used is 5.00.016[e]. The OPC server communicates with the power supply module via a USB hardware adapter. This USB hardware adapter is a USB-CAN interface produced by SYSTEC[f].

5 The VELO High Voltage Finite State Machine

The VELO FSM is constructed as a series of panels which are hierarchial and reactive. These panels allow the user to monitor and control the state of the system. The top level panel allows the control of all channels in the VELO. There are also panels one level down that permit control of the channels on the A-side or C-side. A number of the functionalities of the HV system can be applied to sets of 8 channels, known as a 'board'. This is a natural division of the system as each power supply module controls two sets of 8 channels. Panels are also available which monitor and control individual channels. This section provides a brief overview of the functionalities of the system. The configuration of all channels (e.g. the voltages set, ramping speeds, software current limit) is known as a 'recipe'. The voltages and current limits can be set individually for each channel. The ramping speed can only be set per board. Applying this recipe starts this configuration, ramping up all channels. The recipes can be edited from the top level panel. The recipe for all channels can be applied from the top level panel. The recipe can also be applied for A-side (or C-side), a single board or for a single channel. It is also possible to configure individual channels or whole boards by setting the individual parameters rather than applying a recipe. There are three default recipes, that all LHCb subdetectors must provide, that can be set:

- **GO_STANDBY1**: This is a first level for turning on all the channels. The voltage supplied to the VELO sensor at this level is 10 V.
- **GO_STANDBY2**: This is a second (higher) level for turning on all the channels. The voltage supplied to the VELO sensor at this level is 50 V.

[e]This version of the OPC server may change for future performance improvement.
[f]Systec Automation d.o.o. Katuri 17 52220 Labin, Croatia.

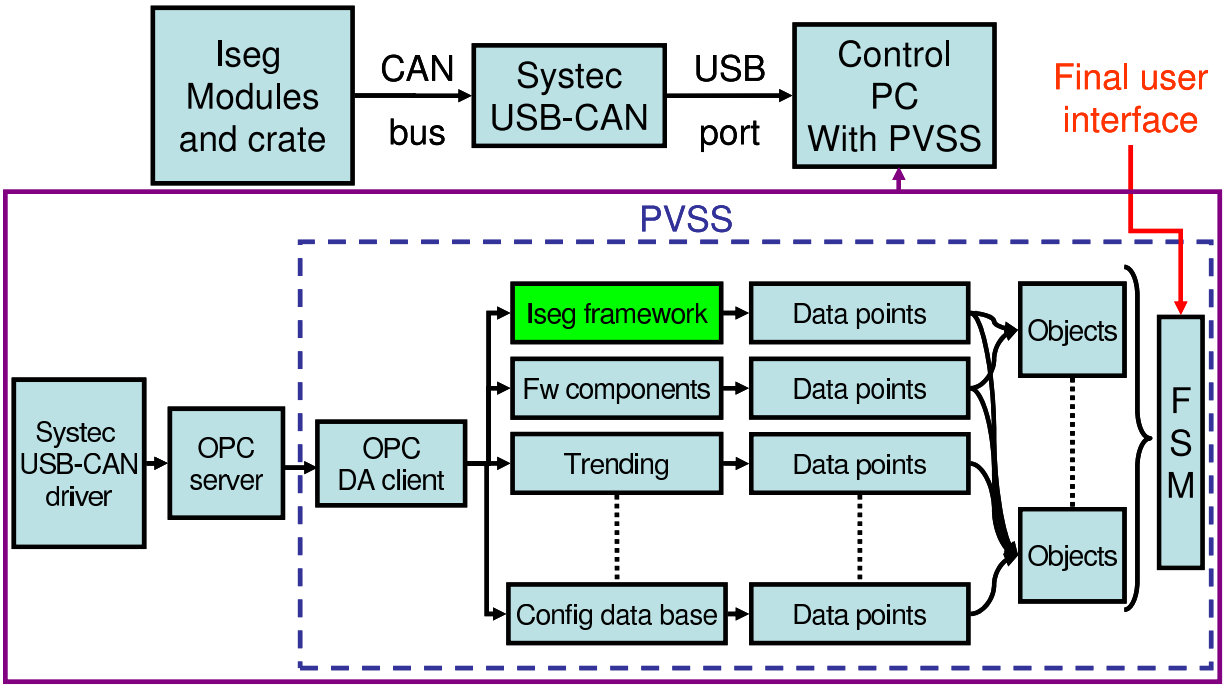

Figure 3 Overview of the high voltage control software structure.

- **GO_READY**: This is the standard physics setting for the detector. The voltage supplied to the VELO sensor at this level is 100 V. This is significantly above the depletion voltage of all sensors. Depending on the irradiation of the VELO sensors, this voltage may be increased.

There are four types of particularly important panels in the VELO HV FSM. The top level panel is called VELO_HV which provides control and monitoring of all HV channels in the VELO. The panels (see figure 4) that allow overall monitoring and control of all channels on the A-side (or C-side) are VELOA_HV (or VELOC_HV). These panels are accessible from the top level panel. The main panels for accessing information on one board (see figure 5) are 'VELO_A_HV_BOARDXY' or 'VELO_A_HV_BOARDXY' (where XY is the number of the board 00-05). The panels for individual channels (see figure 6) are 'VELO_A_HV_BOARDXY_CHVW' or 'VELO_A_HV_BOARDXY_CHVW' (where XY is the number of the board and VW is the number of the channel 00-07). These panels can either be accessed from the top level, the A-side (or C-side) panels or the main board panel. The organigram in figure 7 summarises the information and functionalities which have been discussed here, and provides a guide as to at which level of the FSM they are available.

An IV scan can also be performed. This is obtained from the top level panel, and can be performed for either the whole VELO, A-side (or C-side), the whole board or an individual channel. This information can then be saved. In addition, a panel is provided to perform a voltage scan on selected modules for use in charge collection efficiencies analyses. This panel can be accessed from the Velo top level panel which is part of the Velo top PVSS project.

6 Alarm and Error Conditions

During the operation of the VELO, nominal operation boundary conditions have been defined to prevent any unexpected human mistake and to identify any abnormal behaviour of the sub-systems. The high voltge system characterisation and performance can be found in [6]. For the VELO HV system, the main conditions are:

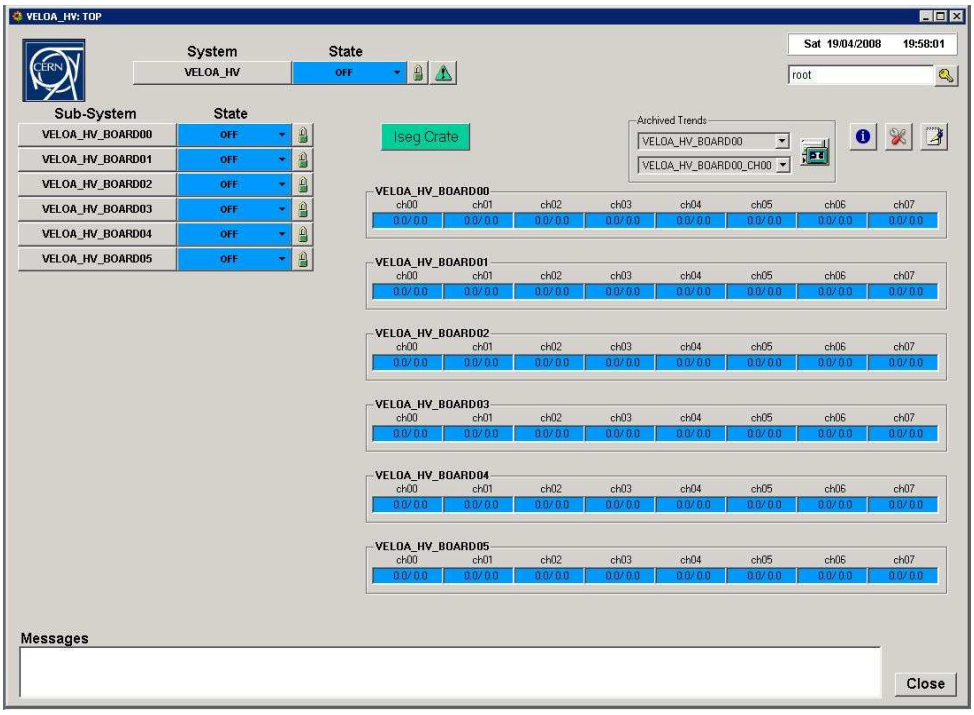

Figure 4 Layout of the VELOA_HV panel. The VELOC_HV panel layout is similar to this panel.

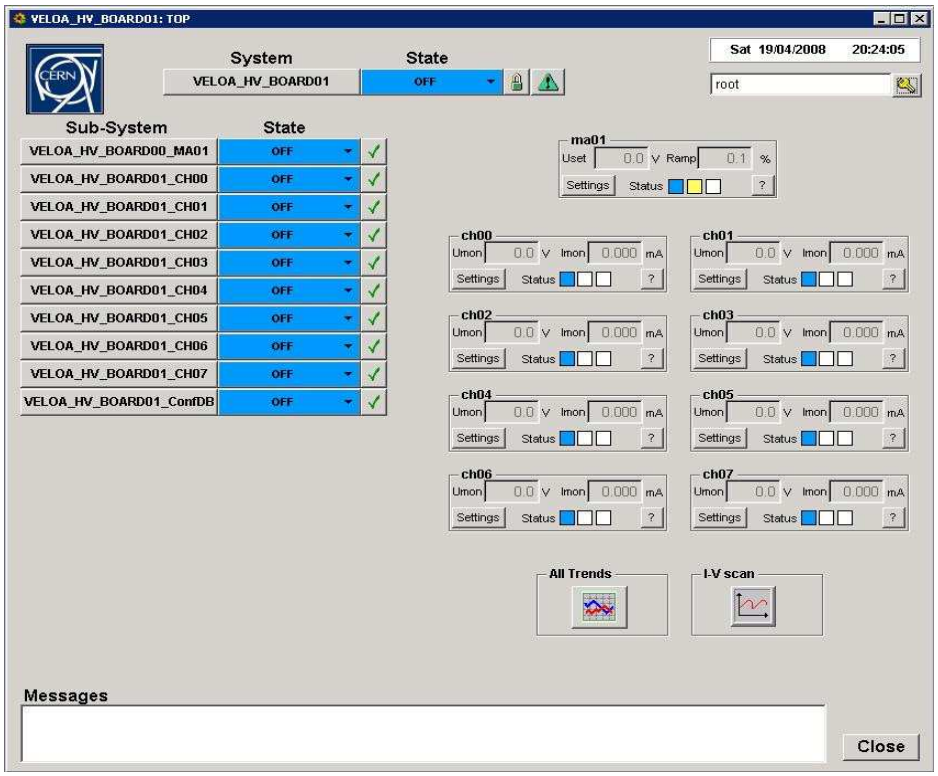

Figure 5 Layout of the VELOA_HVBOARD01 panel. All board panel layouts are similar to this panel.

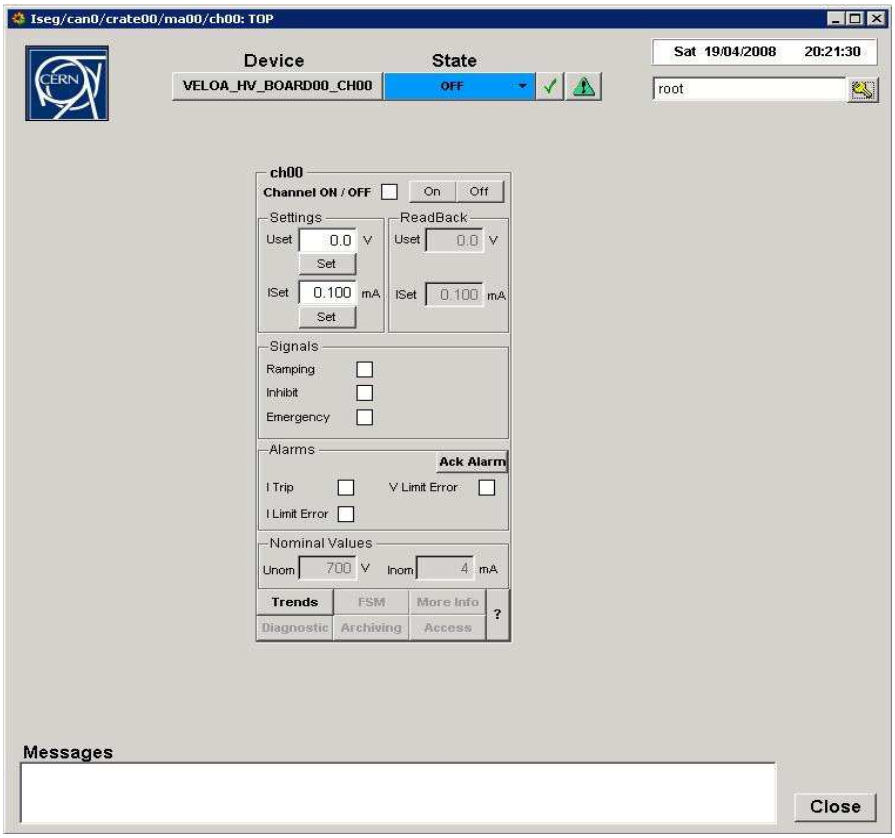

Figure 6 Layout of the VELOA_HV_BOARD00_CH00 panel. All channel panels are similar to this panel.

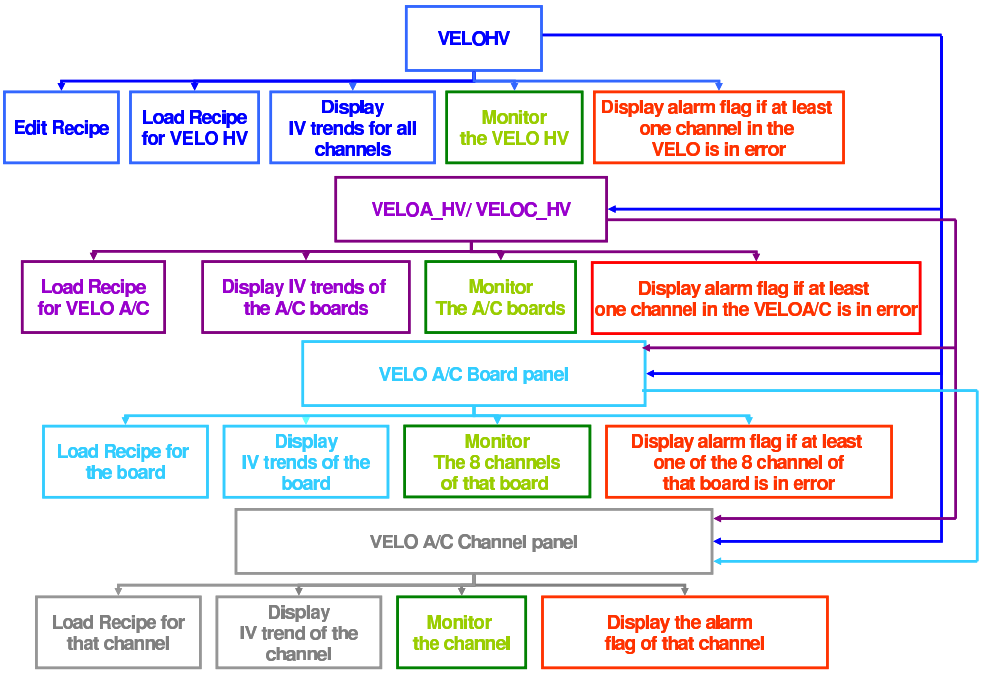

Figure 7 Organigram showing the main VELO HV Finite State Machine structure.

- Implementation of the current and voltage hardware limits. Their current values are set to 240 μA and 217 V respectively.
- Implementation of the current software limit for all HV channels. The value is currently set to 105 μA.
- Implementation of a nominal ramping speed. The chosen value is approximately 1 V/s due to the behaviour of the HV modules at low currents. Otherwise the current will trip due to the low current limit. The nominal ramping speed may be increased to 7 V/s once the sensors will draw higher current.

Furthermore, the HV FSM provides alarm monitoring of the general status of all HV channels, modules and crate. Any problem or error in the HV system will trigger an alarm which will be displayed on the HV PVSS panels. The main error conditions are as follows.

- **ITrip error** occurs when the current drawn reaches the current software limit.
- **ILimit error** occurs when one changes the current hardware limit while using the module.
- **VLimit error** occurs when one changes the voltage hardware limit while using the module.
- **Inhibit error** occurs when the interlock signal is interrupted.
- **Emergency off error** occurs when processes are interrupted. It causes channels to ramp down and then be switched off.
- **AC – line power error** is caused by an interruption of the normal crate power.
- **OPC server crash** is caused by a crash of the Iseg OPC server. The server will not respond and the process has to be restarted.

The error conditions cited above may prevent the HV system to restart if uncleared.

7 Conclusion

The description of the VELO high voltage control software was presented in this note. The implementation of its structure as a PVSS Finite State Machine was emphasized. The main error conditions that may occur during operation were also discussed. The VELO HV software conforms to the specification of the VELO.

8 References

[1] *The LHCb VELO Technical Design Report*, CERN-LHCC-2001-0011

[2] *ETM professional control PVSS*, http://www.pvss.com

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[5] P. Y. Duval et al., *Guide for ECS FSM design in LHCb sub-detectors*, EDMS No: 655828

[6] B. Rakotomiaramanana, C. Parkes and L. Eklund, *Characterization of the VELO High Voltage System*, CERN-LHCb-2008-009