Fabrication of High Aspect Ratio Silicon Nanostructure Arrays by Metal-Assisted Etching

By

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the Massachusetts Institute of Technology on May 3, 2010 in partial fulfillment of
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Abstract

The goal of this research was to explore and understand the mechanisms involved in the fabrication of silicon nanostructures using metal-assisted etching. We developed a method utilizing metal-assisted etching in conjunction with block copolymer lithography to create ordered and densely-packed arrays of high-aspect-ratio single-crystal silicon nanowires with uniform crystallographic orientations. Nanowires with sub-20 nm diameters were created as either continuous carpets or as carpets within trenches. Wires with aspect ratios up to 220 with much reduced capillary-induced clustering were achieved through post-etching critical point drying. The size distribution of the diameters was narrow and closely followed the size distribution of the block copolymer. Fabrication of wires in topographic features demonstrated the ability to accurately control wire placement. The flexibility of this method will facilitate the use of such wire arrays in micro- and nano-systems in which high device densities and/or high surface areas are desired.

In addition, we report a systematic study of metal-catalyzed etching of (100), (110), and (111) silicon substrates using gold catalysts with varying geometrical characteristics. It is shown that for isolated catalyst nanoparticles and metal meshes with small hole spacings, etching proceeded preferentially in the <100> direction. However, etching was confined in the direction vertical to the substrate surface when a catalyst mesh with large hole spacings was used. This result was used to demonstrate the use of metal-assisted etching to create arrays of vertically-aligned polycrystalline and amorphous silicon nanowires etched from deposited silicon thin films using catalyst meshes with relatively large hole spacings. The ability to pattern wires from polycrystalline and amorphous silicon thin films opens the possibility of making silicon nanowire-array-based devices on a much wider range of substrates.

Finally, we demonstrated the fabrication of a silicon-nanopillar-based nanocapacitor array using metal-assisted etching and electrodeposition. The capacitance density was increased

significantly as a result of an increased electrode area made possible by the catalytic etching approach. We also showed that the measured capacitance densities closely follow the expected trend as a function of pillar height and array period. The capacitance densities can be further enhanced by increasing the array density and wire length with the incorporation of known self-assembly-based patterning techniques such as block copolymer lithography.

Thesis Supervisor: Carl V. Thompson
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Chapter 1. Introduction

1.1 Motivation and scope

The objective of this thesis was to develop a relatively simple method for producing silicon nanowires applicable for array-type devices, and to develop a basic understanding of metal-catalyzed etching of silicon. This was driven in part by the current interest in exploring the novel properties and applications of semiconductor nanowires. In particular, silicon nanowires have proven to be good candidates for applications in nanoscale electronics, ultrasensitive sensors, energy storage, and a variety of other devices.

Currently, the most commonly used fabrication method for silicon nanowire synthesis is based on the well-known vapor-liquid-solid (VLS) growth by means of chemical vapor deposition (CVD) with metal nanoparticles such as gold as catalysts. Although relatively well-characterized, the use of this method faces many challenges, such as gold in-diffusion due to high growth temperatures and poor orientation control. Other methods for nanowire fabrication through dry etching processes have also been investigated. However, issues such as mask degradation and process complexity also limit their application as methods for creation of high-aspect-ratio silicon nanostructures.

We have shown that metal-assisted etching, when combined with various metal-patterning techniques, can be a powerful tool for creation of silicon nanowire arrays. We have explored the use of metal-assisted etching to create ordered arrays of silicon nanowires

with controlled diameter, spacing, crystallographic orientation, geometry, and placement. In order to better control the silicon nanostructure, we also investigated how the substrate orientation and catalyst geometry influenced the etching behavior. Lastly, we developed a nanocapacitor device that utilized the high surface-to-volume ratio of the silicon nanostructure made possible by metal-assisted etching.

1.2 Thesis outline

In chapter 2, we present a review on silicon anodization and electroless etching, focusing on their mechanistic similarities to metal-assisted etching. The different parameters that affect the final silicon structure, including etchant solution composition, substrate crystallographic orientation, and substrate dopant type and concentration, are discussed based on an understanding of the silicon dissolution chemistries common to all electrochemical etching approaches. In Chapter 3, we report a mechanistic study that supports the current proposed electrochemical model for metal-catalyzed etching of silicon. Different silicon morphologies obtained with patterned catalyst films of different lateral dimensions were explained based on the intermittent contact between the silicon and metal during etching. Chapter 4 summarizes all the experimental methods used to pattern metal catalyst films. Chapter 5 reports a new technique that utilizes metal-assisted etching in conjunction with block copolymer lithography to fabricate sub-20 nm silicon nanowire arrays with a high density, high aspect ratio, and good monodispersity over large areas. Chapter 6 presents a systematic investigation of

metal-assisted etching as a function of substrate orientation and catalyst geometries. We show that by carefully choosing the geometric characteristics of the catalyst, metal-assisted etching can be extended to the fabrication of vertically-aligned polycrystalline and amorphous silicon nanowires, as well as single-crystal vertical nanowire arrays with different crystallographic orientations. In Chapter 7 we report the fabrication of a silicon-nanopillar-based nanocapacitor array using both metal-assisted etching and electrodeposition. A significant increase in capacitance density is demonstrated. Finally, in Chapter 8 we give general conclusions and propose some aspects of metal-assisted etching warranting further research.

Chapter 2 Background

2.1 Introduction

Porous silicon was first reported as a surface anodic film by Uhlir at Bell Labs over half a century ago. Uhlir made porous silicon during the electropolishing of silicon in aqueous hydrofluoric acid (HF) solutions (1). The thick anodic film was reported to form at a current density below the one at which electropolishing occurs. One year later, Turner also observed the formation of a similar film and described it as "orange-red in color and glassy in appearance" (2). However, at the time the films were not recognized as porous silicon. Instead, based on electron and X-ray diffraction results, the thick films were presumed to be an anodically grown film that was amorphous in nature.

It took almost 20 years from the initial report on porous silicon for the porous nature of the thick anode film to be revealed (3). Making use of its relatively large oxidation velocity compared to bulk silicon, the first application of porous silicon was demonstrated by Watanabe *et al.* as an isolation layer for silicon integrated devices such as bipolar integrated circuits and field effect transistors. A series of studies on the fast oxidation mechanism and application of porous silicon for dielectric isolation ensued in the following decade (Imai, 1981). Nevertheless, despite progress in the field, the real explosion of interest in porous silicon research only occurred later after the first demonstration of visible photoluminescence at room temperature in 1990. (4). In the following years, an abundance of research activity in the area

followed with the prospect of someday realizing porous-silicon-based optoelectronic devices. Considerable effort has been made to explain the origin of luminescence in porous silicon. However, since it is not the purpose of this background review to discuss the optoelectronic properties of porous silicon, readers are referred to a comprehensive review by Cullis *et al.*, which discusses the luminescence properties of porous silicon and the various models that have been proposed as the origin of light emission in great detail (5).

In addition to interest in its optoelectronic properties, much research effort has been extended on the development of models to explain porous silicon formation with the intention of better controlling its structure. Due to its long history, a vast literature exists for both the etching characteristics and dissolution chemistries of anodized silicon. Because this thesis focuses primarily on metal-assisted etching, we will only review the aspects of silicon anodization that are pertinent to our present work. In this chapter, a detailed review on the anodization of silicon will be presented first as the basis for subsequent discussions on porous silicon structures formed via other approaches. This will be followed by a selected review on two types of electroless etching methods: photo-electrochemical etching and stain etching. Finally, a review of recent literature on metal-assisted etching will be presented, again with a focus on the formation mechanism. The many similarities that exist between metal-assisted etching and other electrochemical methods for forming porous silicon will become clear from the rest of this review. Certain of the experimental results and proposed mechanisms for

metal-assisted etching reported in the literature will be discussed based on an understanding of silicon dissolution chemistries that have been studied extensively for these other approaches.

2.2 Silicon anodization

This section will discuss porous silicon structures formed using anodic etching. Before going into any further detail, some terminologies need to be discussed. Typically, porous media are classified according to the IUPAC (International Union of Pure and Applied Chemistry) guidelines. Based on the IUPAC convention, pores with diameter smaller than 2 nm are called *micropores*, above 50 nm they are called *macropores*, and in between they are called *mesopores* (6). In the porous silicon literature, however, these terms are sometimes used loosely. For example, the term microporous silicon has been used to refer to porous silicon in general in some literature. Additionally, with the rise of nanotechnology, new terms that are not so well-defined such as "nanoporous" have been coined to describe porous structures with nanoscale dimensions. In this review, we will try to adhere to the criteria set by IUPAC with the exception of using the term *porous* to refer to pores formed on all size scales.

2.2.1 Anodic dissolution of silicon

Silicon anodization involves the attachment of a silicon substrate and a counter electrode to an external power supply used to apply a potential on the silicon sample. The electrochemistry is controlled by the direction and magnitude of the applied voltage as well as by the composition of the electrolyte solution. Details about the electrochemistry can often be

revealed by analyzing the current-voltage (I-V) characteristics of the system. Exact details of the I-V characteristics during the electrochemical etching of silicon can vary from paper to paper due to the large number of control parameters involved. The general form, however, tends to be similar. The anodic portion of a typical I-V curve for both p-type and strongly illuminated n-type silicon (the reason for illumination of n-type silicon will be discussed later) in an electrolyte of HF shows three different dissolution regimes: *pore formation*, *electropolishing*, and a *transition* region in between (7). **Figure 2.1** shows one such typical I-V curve in the anodic dissolution portion. As shown in the figure, there exists a critical current density (J_{crit}) and peak potential above which electropolishing takes place (Region C). Below J_{crit}, silicon only partially dissolves to form a porous layer which can gradually grow into the surface as anodization proceeds (Region A). At intermediate potentials, the silicon surface morphology is determined by a competition between electropolishing and porous silicon formation (Region B).

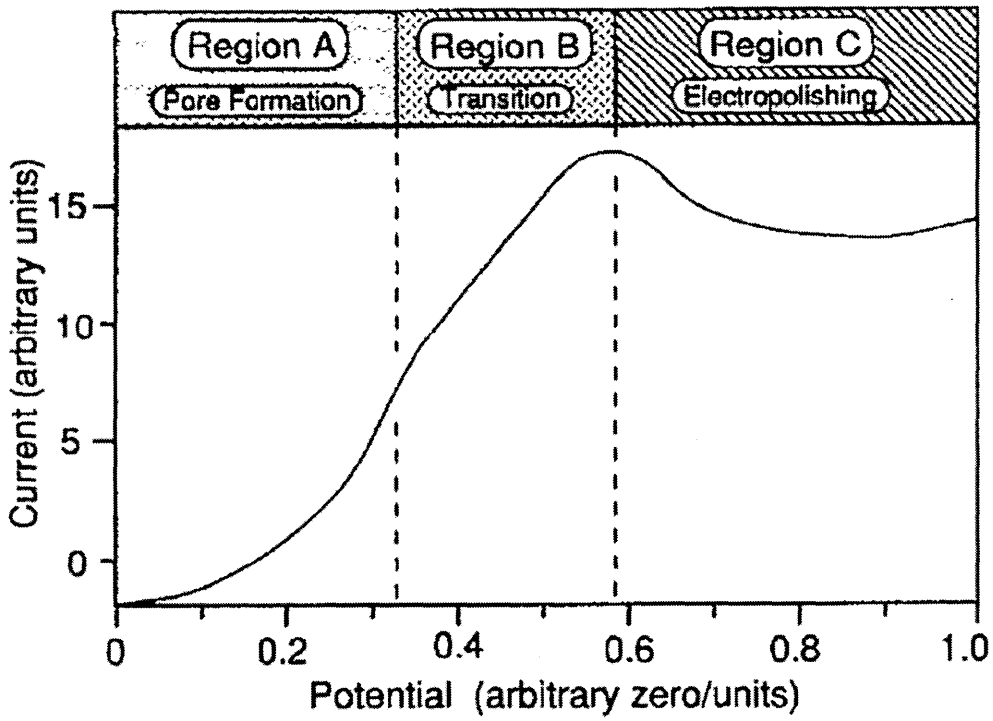

Figure 2.1 Typical I-V curve for the anodic dissolution of silicon in hydrofluoric acid (HF) solutions showing the three regimes of dissolution: pore formation, transition, and electropolishing (7).

In order to understand the different regimes during silicon anodization, an understanding of the surface dissolution chemistries of silicon in hydrofluoric acid (HF) is necessary. Although the exact mechanism is still in question, it is generally accepted that electronic holes (h^+) are required for the oxidation of silicon in the initial stages of both pore formation and electropolishing (7). Note that the term oxidation is used in a broad sense. It is defined as a chemical reaction that involves an increase in oxidation number (loss of an electron), and does not necessarily mean the formation of an actual oxide. The overall reaction of silicon dissolution in HF is most simply written as the following (8):

$$Si_{(solid)} + 6F^- + (4 - n)h^+ \rightarrow SiF_{6(soln)} + ne^- \qquad [2.1]$$

where *n* is the effective valence number ranging between 0 and 4 for Si. The valence number in this case indicates the number of electrons flowing through the external circuit per dissolved silicon atom, and has been reported to be approximately 4 during electropolishing and 2 during porous silicon formation (2) (9). In other words, during porous silicon formation, only 2 out of the 4 available silicon electrons/holes participate in a direct interfacial charge transfer whereas during electropolishing, all 4 electrons participate in the surface reaction (7).

A number of mechanisms including the autocatalytic electron promotion into the silicon conduction band at surface impurity sites (i.e. dopant sites) (10) and a dual hole transfer model (11) have been proposed to explain the divalent state of silicon during porous silicon formation. Nevertheless, most experimental data point toward a surface bound oxidation scheme presented by Lehmann and Gosele (12). A schematic of the proposed dissolution mechanism is shown in **Figure 2.2**. Steps (1) - (5) indicate the sequence of reaction steps associated with porous silicon formation. According to this model, due to similar electronegativity values of silicon and hydrogen, a hydrogen-terminated silicon surface is stable against dissolution in HF solutions unless electronic holes (h^+) are available. If a hole reaches the surface and polarizes a Si-H bond, the bond that is originally stable can now be attacked by fluoride ions to form a Si-F

bond (step 1). One might ask why electrons, which are also charge carriers, do not contribute to the initial stage of silicon dissolution. This is mainly because of the higher energy necessary for electron injection compared to the energy required for recombination with holes. As a consequence, the presence of electrons is not required to initiate the dissolution, and instead is only considered as a second step in the dissolution reaction (13). Due to polarization effect of this first Si-F bond, another F^- ion can attack the neighboring Si-H bond, injecting an electron into the silicon (step 2). As the polarization of the two surface Si-F bonds weaken the Si-Si backbonds, the backbonds are now susceptible to attack by HF to form SiF_4 (step 3 and 4) which then reacts with HF to form the final, stable end product for silicon in HF, H_2SiF_6 (step 5). The remaining silicon surface atoms are again bonded to hydrogen, as they started, and are passivated against further dissolution unless more electronic holes are available. An atomic size dip now remains where a silicon atom is removed, changing the electric field distribution in such a way that hole injection occurs preferentially at the site. As a consequence of the uneven field distribution, a pore will begin to grow at this site, provided that the pore walls are passivated against etching.

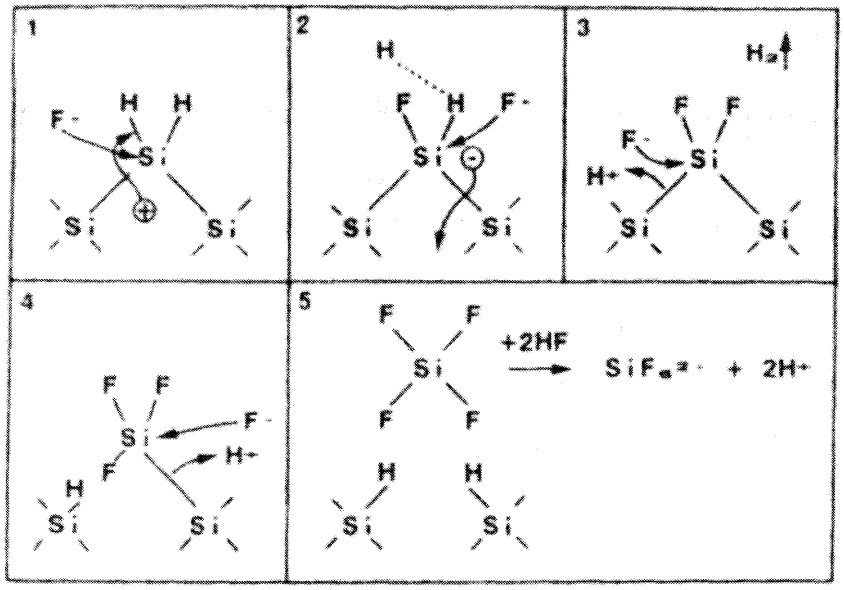

Figure 2.2 A surface bound oxidation scheme used to explain the dissolution of silicon electrodes in HF (12).

Based on the understanding that holes are required for silicon dissolution, the I-V curve in **Figure 2.1** can now be explained as follows. In the pore formation regime where the current density is low, the reaction is limited by the supply of holes to the silicon electrode surface. Generated surface holes, regardless of their origin, are immediately consumed as HF etches away the "oxidized" silicon. The I-V curve in this regime is therefore characterized by a linear Tafel slope. In the electropolishing regime where the current density is high, holes are accumulated on the silicon electrode surface. The reaction is now limited by the rate at which HF etches silicon away. As a result, the slope of the I-V curve is much smaller than in the pore formation region.

The reason illumination is required for anodizing n-type silicon can also be explained

based on the silicon dissolution chemistry. As shown in **Figure 2.1**, there exists a critical current density below which porous silicon can form. It was found that this critical current density is independent of the doping type of the silicon as long as enough holes are supplied to the silicon surface. A topological distribution map for the different silicon dissolution regimes as a function of current density and HF concentration is shown in **Figure 2.3** (11). According to this result, neither the semiconducting properties of silicon nor the way holes are created have much effect on the occurrence of the three dissolution regimes. In other words, although the electronic properties of p- and n-type silicon substrates are different, the dissolution chemistry is the same. For p-type silicon, a moderate applied potential is enough to provide the electronic holes needed for silicon dissolution. N-type silicon, on the other hand, would require a very large potential, enough to cause breakdown. This often leads to an uneven porous film. In order to produce a porous silicon film that is uniform in thickness and morphology, additional holes are often generated via other means such as backside illumination. More details regarding the etching behavior dependence on doping type and concentration are discussed in **Section 2.2.3**.

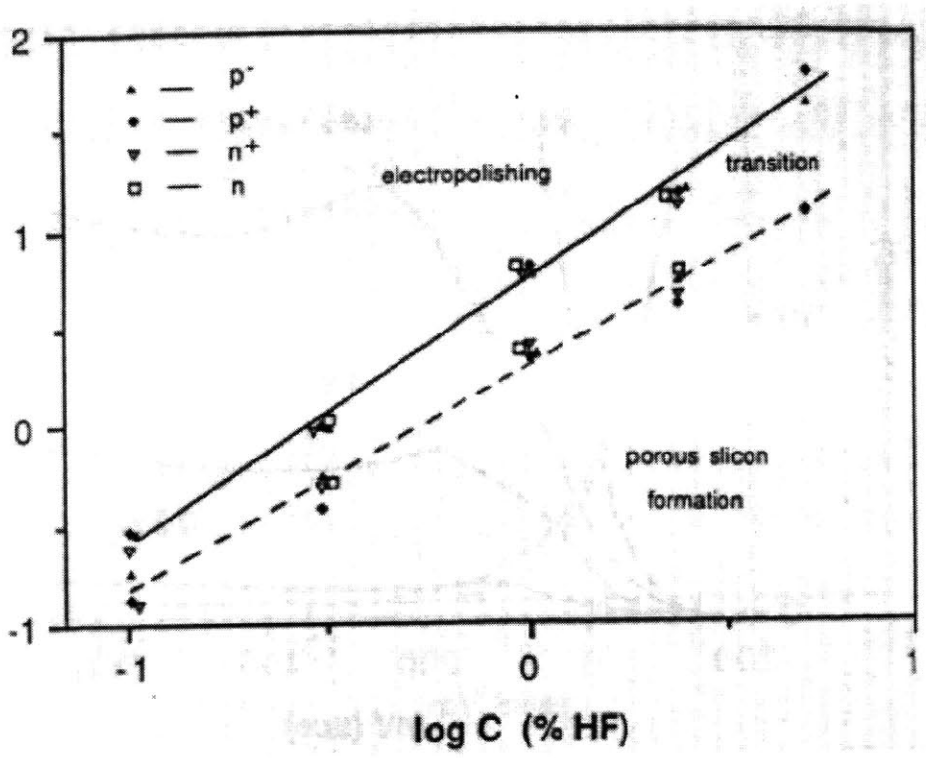

Figure 2.3 A plot of the upper limit of the current density for porous silicon formation as a function of HF concentration indicating regions for porous silicon formation, transition region, and electropolishing. (11)

2.2.2 Crystallographic orientation dependence

Similar to the well-characterized etching behavior of silicon in alkaline solutions (14), the electrochemical etching of silicon in HF solutions also exhibits preferential etching along certain crystallographic directions; i.e. anisotropic etching. Harsanyi and Habermeier have reported preferential etching directions parallel to {100} planes in anodically-etched n-type (100) and (111) silicon substrates, determined by imaging plan-view etch patterns on sectioned planes parallel to the original substrate surface at different section depths (15). The observation of anisotropic etching in the <100> direction was later confirmed by Chuang *et al.* by direct cross-sectional transmission electron microscopy (XTEM) for both n- and p-type

silicon (16). Based on XTEM results, it was found that the observed preferential pore propagation direction was indeed the <100> direction regardless of the substrate orientation, dopant type, and dopant concentration. **Figure 2.4** shows three examples of the <100> pore propagation direction in n(100), n(110), and p(100) silicon substrates.

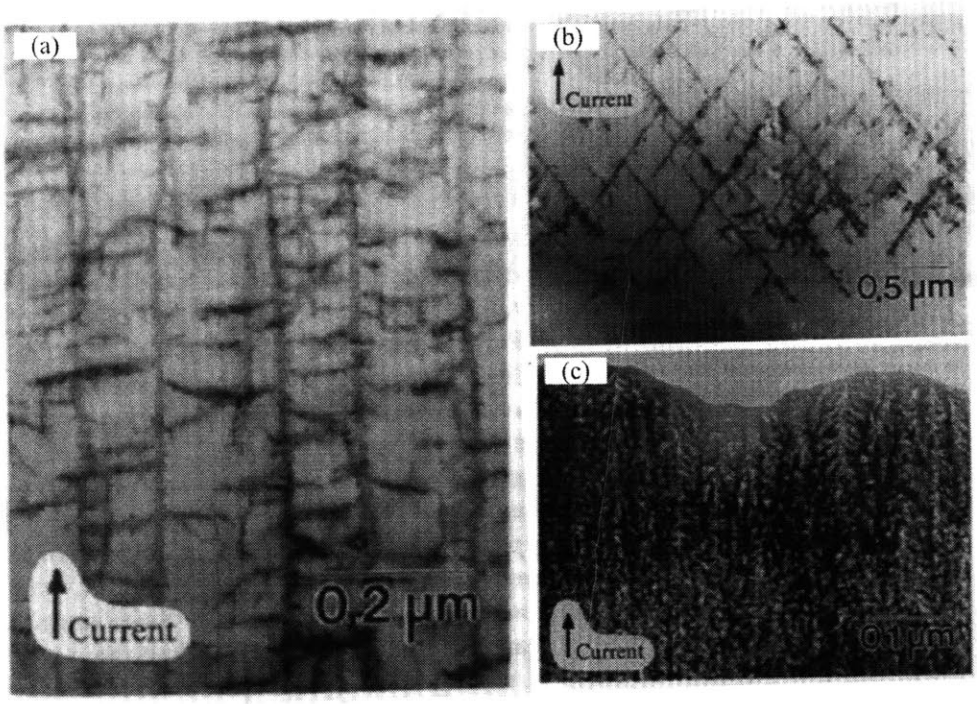

Figure 2.4 Cross sectional transmission electron microscopy (XTEM) image of porous silicon formed on (a) n (100); (b) n (110); and (c) p (100) silicon substrates (16).

Two models have been proposed to explain the etching direction dependence on substrate orientation. The first model attributes the anisotropic etching to the surface bonding geometry of silicon, and the second explains the anisotropy as based on hydrogen passivation effects for different crystallographic planes of silicon. Details of each model are briefly summarized below.

✧ *Silicon surface bond configurations*

As described in **Section 2.2.1**, polarization induced by Si-F bonds can distort and thereby weaken the Si-Si backbonds for further attack by HF. This effect is most prominent for {100} planes with two of the four Si bonds symmetrically directed into the solution (17). A {111} surface silicon atom, on the other hand, has just one dangling bond directed into the solution. Thus only one F can bond to the Si atom, and this one Si-F bond must weaken three Si-Si backbonds enough for the silicon atom to be removed from the surface. As a result of this geometrical difference, etching is the fastest in the <100> direction. The bond configurations for (100), (110), and (111) planes are shown schematically in **Figure 2.5**.

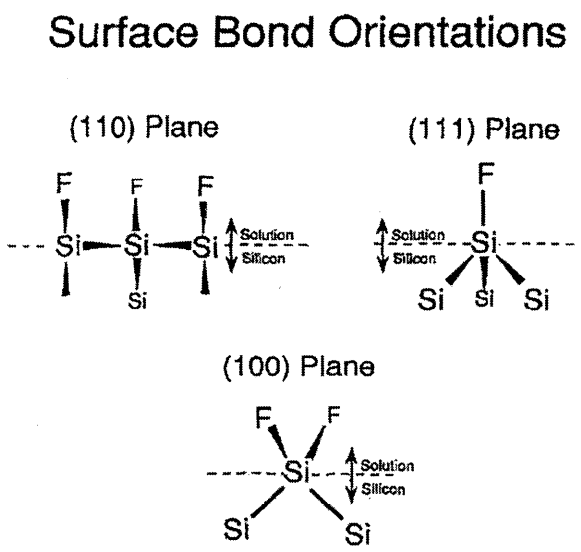

Figure 2.5 Bond orientation for three common crystal planes: (100), (110), and (111). The (100) plane has the most sterically favored geometry for the divalent silicon surface state in the initial stage of silicon dissolution (7).

✧ *Hydrogen passivation effects*

Cristophersen *et al.* pointed out that the degree of hydrogen passivation on different surface orientations may also play a role in the anisotropy (18). Namely, the degree of H-passivation on {111} surfaces is much better than on {100} surfaces. In addition, H-adsorption is faster on {111} surfaces compared to {100} surfaces. Since an H-passivated silicon surface is stable against dissolution in HF solutions (12), <100> directions are, again, the preferred growth direction for pore formation.

It is worth noting that the etching anisotropy discussed in this section applies primarily to silicon dissolution in the porous silicon formation regime. Above J_{crit} in the electropolishing regime, {100} and {111} surfaces are found to have the same etch rates. (19). This difference in etching behavior can be used to explain the etching direction change as a function of etchant solution composition in metal-assisted etching, which is discussed in **Section 2.4.3**.

2.2.3 Dopant dependence

Although the semiconductor properties have little influence on the onset of the three different regimes of silicon dissolution as a function of current density and HF concentration, (11), the pore morphology is heavily affected by the dopant concentrations of the silicon substrate. Typically, porous silicon morphologies can be grouped into four basic groups according to their doping type and concentrations: n, p, n^+, and p^+ (lightly doped n- and p-type Si, heavily doped n- and p-type silicon, respectively) (7). Generally two distinct types of

microstructure are observed. In degenerately-doped n- and p-type silicon, the porous silicon film consists of many long channels running perpendicular to the substrate surface. Alternatively, lightly-doped n- and p-type silicon forms interconnected pores on a much smaller size scale (M.I.J. Beale, 1984). For p-type Si, the pore diameters and interpore spacings increase slightly as a function of dopant concentration (at below degeneracy). For n-type silicon, the opposite is true. In general, pore diameters in n-type silicon are considerably greater than that in p-type silicon. The different pore morphologies as a function of dopant type and concentration are shown in **Figure 2.6**.

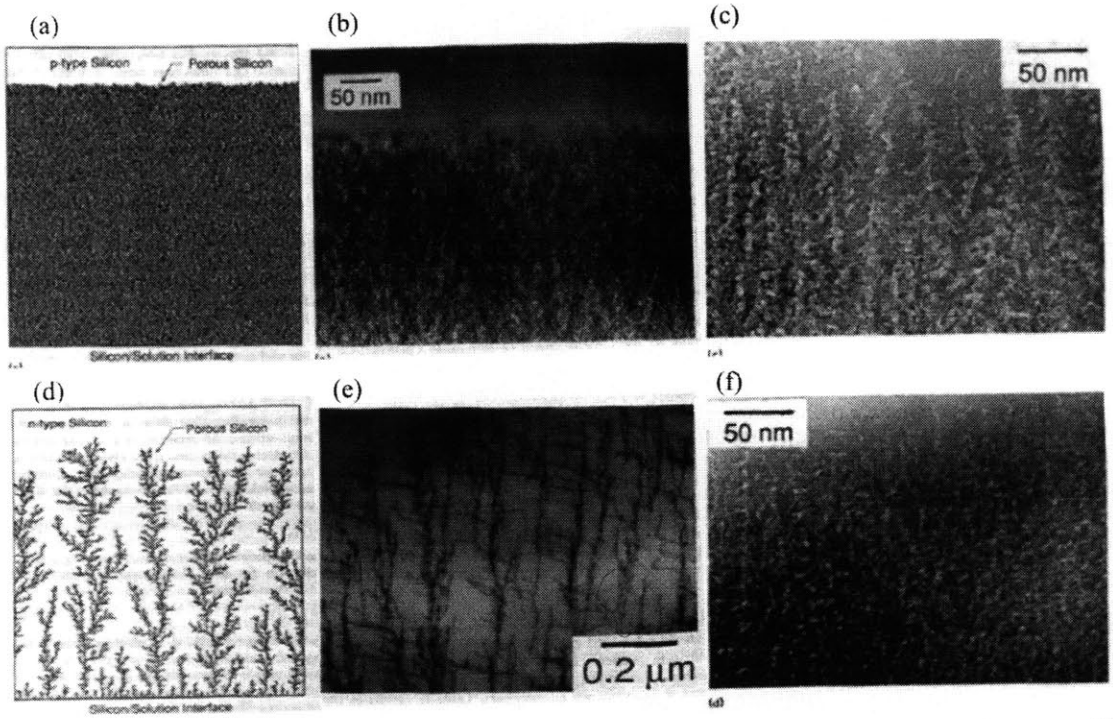

Figure 2.6 (a)-(c) Porous silicon structure of p-type Si: (a) computer-generated p-type Si sample; (b) XTEM micrograph of lightly doped p-type Si sample; and (c) XTEM micrograph of a heavily doped p-type Si sample. (d)-(f) Porous silicon structure of n-type Si: (d) computer-generated n-type Si sample; (e) XTEM micrograph of lightly doped n-type Si sample; and (f) XTEM micrograph of a heavily doped n-type Si. Lightly-doped n-type silicon shows a

strong tendency to form straight channels. Lightly-doped p-type silicon shows extremely small and highly interconnected pores. Both n+ and p+ -type silicon showed tendency to form small 5-10 nm channels with numerous side branches (7).

Several models have been proposed to account for pore formation and pore morphologies in porous silicon. Among these models, the Beale model is the most generally accepted, and will be discussed in greater detail here.

The Beale model discusses the porous silicon formation process on the basis of semiconductor physics rather than chemistry (20). The model makes several assumptions: (i) the total voltage drop occurs over two regions connected in series: the interface region (including the surface states on the semiconductor surface and the screening layer in the electrolyte), and the bulk silicon up to the interface; (ii) the chemistry of the interface region is independent of the dopant type and concentration in the semiconductor; and (iii) the Fermi level at the silicon surface is pinned near midgap due to a large density of surface states at the silicon-electrolyte interface. A schematic of the band diagrams for both p- and n-type silicon with and without an applied bias is shown in **Figure 2.7**.

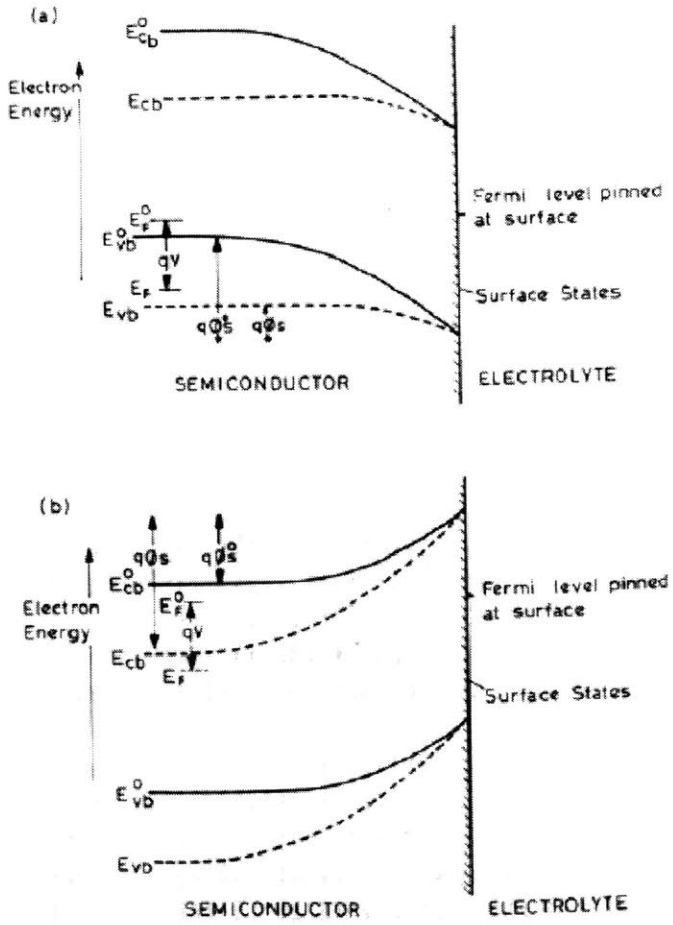

Figure 2.7 A schematic diagram of the semiconductor band structure up to the electrolyte interface. Solid lines represent the situation with zero applied bias and dashed lines represent the situation with applied anodizing voltage for (a) p-type, and (b) n-type material. Φ_S, E_F, E_{vb}, and E_{cb} correspond to the barrier height, Fermi energy, valence band energy, and conduction band energy, respectively. The superscript ^{0} corresponds to the case with zero applied voltage (20).

Pore growth can only proceed if pore tips are preferentially etched. The Beale model attempts to explain the preferential etching of pore tips over pore walls based on the existence of a depletion layer at the Si-electrolyte interface. The observed inter-pore distance is always less than the depletion layer width. As a consequence of the high resistivity of the depleted region, the current always flows down the electrolyte into the pore tips. Dissolution is

therefore confined to pore tips. Pore walls, on the other hand, remain stable in the etchant solution because of the depletion region.

The difference in the porous silicon microstructure between degenerate and non-degenerate silicon can also be explained by studying the depletion region in the silicon at the Si-electrolyte interface. Both the width of the depletion region and the barrier height depend on the dopant concentration in the semiconductor. For degenerately doped material, the width of the barrier is sufficiently narrow to allow tunneling of charge carriers. For non-degenerately doped material, however, current transport across the barrier can only occur by thermionic emission.

In the tunneling case, or degenerately doped silicon, the width of the depletion layer determines the current density. The width is the smallest at a pore tip due to geometrical effects in the electric field distribution. The higher current density at the pore tips results in a directional channel structure that is typically observed for heavily doped silicon. The directional nature of the channels is further enhanced by the presence of other nearby pores. The depletion regions begin to overlap when the pores are spaced close enough. Any tunneling currents in regions other than the pore tips are unlikely as the carriers would have to tunnel through a prohibitive distance. As a consequence, the pores are in effect repelling one another during etching. This effect is schematically illustrated in **Figure 2.8**.

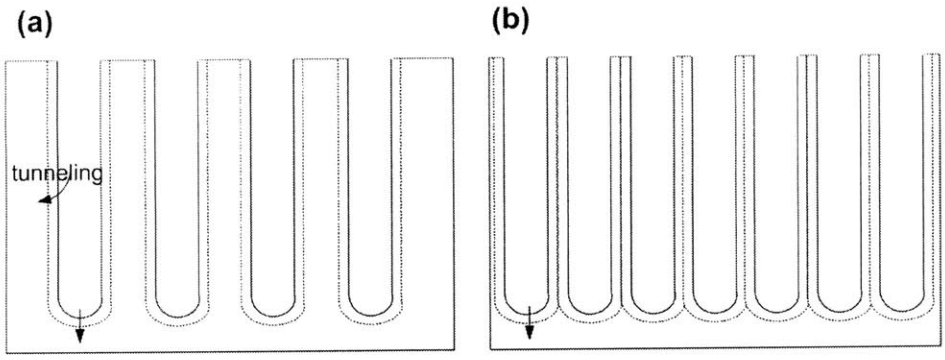

Figure 2.8 A schematic illustration showing the effect of the overlap of the depletion regions when the pores are spaced close enough in a degenerately doped silicon substrate. When the pores are spaced further apart (a), tunneling can occur to form side branches. When the pores are spaced close to one another (b), tunneling can only occur at the pore tips, resulting in a highly directional channel structure.

In the thermionic emission case, or non-degenerately doped silicon, the height of the barrier determines the current density. Since it is the height rather than the width of the barrier that determines the current flow, the pores can grow into each other's depletion regions. The cooperative motion of pore growth discussed in the previous paragraph is not observed for lightly-doped material since the repulsion effect between pores no longer exists. The smaller size of pores grown in non-degenerately doped material is explained using an argument based on image charge effects. Image charges build up in the surface states and the electrolyte in response to carriers approaching the interface region. Similar to the case of a silicon-metal interface, the potential associated with the image charge lowers the barrier height. The lowering is a function of the electric field, which in turn is an inverse function of the pore tip radius. In other words, the barrier height lowering becomes more significant as the pore sizes become smaller.

As mentioned previously, another difference between n-type and p-type silicon is the applied potential necessary to initiate porous silicon formation. Based on the band diagrams shown in **Figure 2.7**, this difference can be explained in terms of a barrier lowering effect at the interface. With an applied anodizing voltage, the barrier height is lowered in p-type material whereas in n-type material, the barrier is raised. As a result, a much lower voltage is needed for p-type than n-type Si to generate a high enough current density for silicon dissolution. This barrier lowering effect is later used to account for the different silicon morphologies as a function of dopant type and concentration in metal assisted etching as well. An example of this will be given in **Section 2.4.4**.

The pore diameter in n-type silicon is in general greater than that observed in p-type silicon. The different etching behaviors for n-type silicon as a function of dopant concentrations have been studied by several groups (8) (21). Since the relevant dimensions of metal-assisted etching is usually in the regime of macro- and occasionally mesopores, a brief review on the underlying physics of macropore formation in low-doped n-type silicon is presented here.

As discussed earlier, for electrochemical pore growth, two conditions must be satisfied: (i) the pore walls must be stable against dissolution in HF, and (ii) the pore tips must be susceptible to dissolution in HF (17). Since holes are minority carriers in n-type

semiconductors, the first condition is easily satisfied as the pore walls are depleted of holes and therefore passivated against etching. The second condition is typically fulfilled by a charge build-up of holes either by illumination or a bias large enough to cause breakdown. In both cases, the maximum local current density is limited by the mass transfer rate in the electrolyte, which is a function of ionic concentrations, and temperature. As a result, all pore tips are in the steady-state condition of maximum mass transfer specified by the critical current density (17). For instance, if all the holes are consumed at the pore tips via silicon dissolution, then the pore walls become passivated against HF etching due to a depletion of holes. However, if mass transport of HF into the pores is not sufficiently fast, the holes begin to penetrate into the walls, causing a widening of the pores and eventually leading to electropolishing of the entire substrate. Similar findings have been reported for metal-catalyzed etching and will be reviewed in **Section 2.4.2**.

2.3 Electroless etching of silicon

Besides the anodization approach discussed in **Section 2.2**, other electrochemical routes to porous silicon formation including photo-assisted etching and electroless etching have also been demonstrated. In photo-assisted etching, a light source is used to generate additional charge carriers. In electroless etching, silicon dissolution occurs spontaneously without the need for an external power supply or light source (22). There are several types of electroless etching, among which the most important are stain etching and metal-assisted etching. The

basic silicon dissolution chemistry in these other approaches is mechanistically very similar to the anodization of silicon. The main difference is in how the electronic holes are generated. The basic mechanisms of photo-assisted and stain etching are discussed below in light of their similarities and differences to anodized silicon. A detailed discussion on metal-assisted etching will be presented in the next section.

✧ *Photo-assisted etching*

Photo-electrochemical etching of silicon was first reported by Noguchi and Suemune (23). In this approach, surface irradiation, such as an ultraviolet (UV), visible or infrared (IR) laser irradiation, is utilized to generate the electronic holes necessary for silicon dissolution without external biasing. The band bending in silicon at the Si-electrolyte interface is thought to be responsible for separating the generated holes from electrons. In n-type silicon, the internal field resulting from band bending is such that holes are forced toward the surface of the irradiated area. In p-type silicon, the reverse is true, and etching occurs only in the un-irradiated area.

In addition to the doping type of the substrate, the laser intensity and HF concentration also influences the porous silicon structure formed photo-electrochemically (24). It is suggested that whether etching is isotropic or anisotropic depends on the relative availability of holes and fluoride species which are in turn determined by the laser intensity and the HF concentration, respectively. This is quite similar to the different regimes observed in the

anodization of silicon.

✧ *Stain etching*

Stain etching is the etching of silicon that results from an etchant solution consisting of fluoride species and an oxidant. Turner was among the first to study the stain etching of silicon (and germanium) in a mixed solution of hydrofluoric acid and nitric acid, although at the time the porous nature of stain-etched films was not recognized (25). Based on etch rate measurements as a function of the HNO_3/HF ratio, he proposed the following reactions:

$$HNO_3 + 3H^+ \rightarrow NO + 2H_2O + 3h^+ \qquad [2.2]$$

$$Si + 2H_2O + nh^+ \rightarrow SiO_2 + 4H^+ + (4-n)e^- \xrightarrow{6HF} H_2SiF_6 + 2H_2O \qquad [2.3]$$

$$3Si + 4HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4NO + 8H_2O + 3(4-m)h^+ + 3(4-m)e^- \qquad [2.4]$$

Equation [2.2] is the cathode reaction, **[2.3]** the anode reaction, and **[2.4]** the overall reaction of the system. Note that according to the overall equation, the maximum rate of etching should occur at a mole ratio of 1/4.5 (HNO_3 to HF).

Beale *et al.* recognized the porous nature of stain-etched Si films by doing structural studies (26). The structural similarity between anodized and stain-etched porous silicon films led them to believe that a similar formation mechanism exists for the two processes. Indeed, analogous to the case of the anodization of silicon, the etching behavior can be separated into

different regimes corresponding to different mole ratios of HNO_3 to HF. Robbins and Schwartz concluded that for mole ratios smaller than 1/4.5, the etch rate is controlled by the diffusion and/or convection of HF to the substrate surface; whereas for molar ratios greater than 1/4.5, the etch rate is controlled by the availability of HNO_3 at the Si surface (i.e. availability of holes) (27). Additionally, electropolishing occurs only at a sufficiently high concentration of the oxidizing species, suggesting a local current density greater than the critical current density (25). This is very similar to the electropolishing regime in the anodization of silicon.

As discussed above, the role of the oxidant is to inject holes into the silicon valence band. Therefore, one important selection criterion for the oxidant is the electrochemical potential and the rate at which it can transfer its charge to the silicon surface (22). An oxidant with a sufficiently positive electrochemical potential is desired such that the acceptor level of the oxidant lies at or below the Si valence band. This is demonstrated schematically in **Figure 2.9**. The structure and hence the properties of the resulting porous silicon film can be controlled by using oxidants with different electrochemical potentials (28).

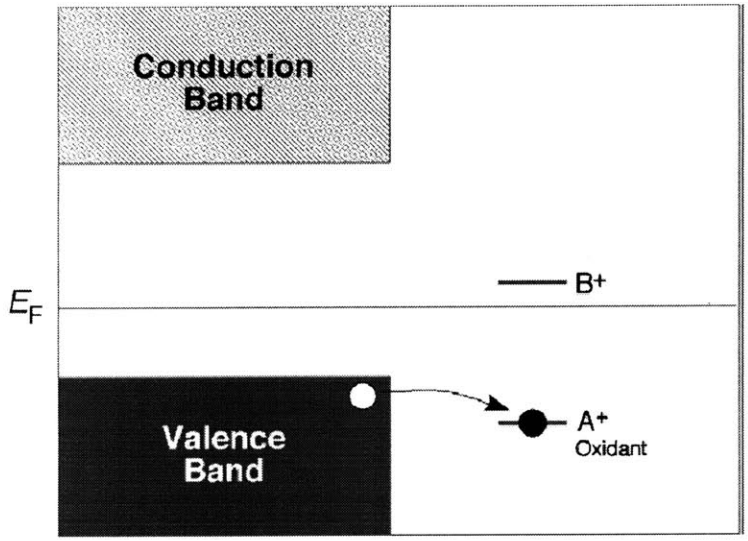

Figure 2.9 A schematic diagram showing hole injection into an oxidant with an electron acceptor level below the silicon valence band. An oxidant such as B^+ cannot be used as an oxidant for the stain etching of silicon (22).

2.4 Metal-assisted etching

2.4.1 Introduction

The electrochemical etching of silicon in HF solutions in the presence of metal was first reported as an attempt to minimize the time between insertion of silicon and porous silicon formation in stain etching. This incubation time is a consequence of the complexity of the nitric acid reduction process and can be minimized by giving the reduction process a boost using a catalyst (29). This was demonstrated by Dimova-Malinovska *et al.* by depositing a thin layer of evaporated Al on the silicon substrate prior to etching to initiate the reduction of HNO_3 via the following equation (30).

$$Al + 3HNO_3 \rightarrow Al(NO_3)_3 + 3H^+ \qquad [2.5]$$

The H^+ produced in **Equation [2.5]** initiates the cathode reaction (shown in **Equation [2.2]**). The Al dissolves during the process. It was also demonstrated that the aluminum can be patterned for formation of porous silicon at selected areas.

The etching of Si in the presence of metal was further investigated by Kelly and co-workers (31). In their studies, Si etching was induced by forming a galvanic cell composed of a noble metal electrode short-circuited to a silicon substrate in an HF solution. The principle of galvanic cell formation for the Si-metal system is illustrated schematically in **Figure 2.10** (32). Curve (a) in **Figure 2.10** represents the anodic region of the dissolution of a p-type Si electrode, which is of the same form as the general anodic I-V curve shown in **Figure 2.1**, with a porous silicon formation regime below the peak potential and an electropolishing regime at high potential. Curves (b) – (d) are the I-V curves of the electrochemical reduction of two different oxidizing agents by the noble metal electrode, one with a redox potential slightly more negative than the anodic peak of silicon [(b)], and the other with a redox potential above the peak [(c) and (d)]. When the metal is short-circuited to silicon, a new rest potential, usually referred to as a *mixed potential*, at which the rate of oxidant reduction is equal to the rate of silicon dissolution is formed (U_b, U_c, and U_d). For the less electropositive oxidizing agent (b), the new mixed potential U_b is located below the peak anodic potential. For the more electropositive oxidizing agent (c and d), two things can happen depending on the concentration of the oxidizing agent. At a lower concentration, the mixed potential U_c rests

below the anodic peak. At a higher concentration, the mixed potential U_d lies above the peak potential where polishing occurs.

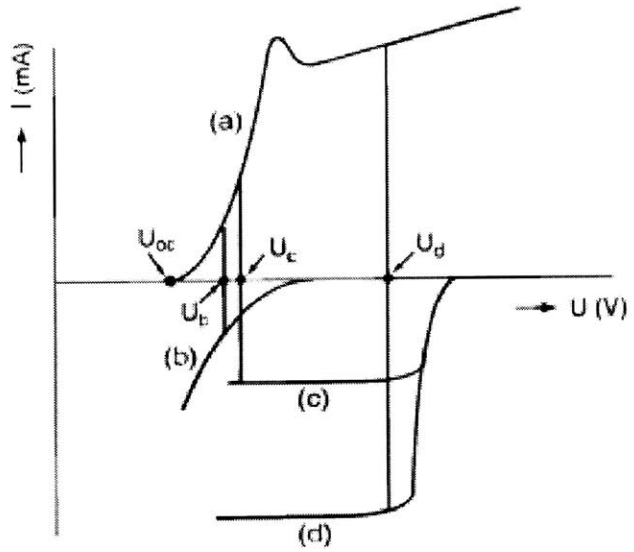

Figure 2.10 Schematic representation of galvanic cell formation. Curve (a) is the I-V curve for a p-type Si(100) in an aerated HF solution. Curves (b) – (d) are the cathodic I-V curves for various oxidizing agents on a noble metal electrode in the same solution. (32).

Based on the basic principle of galvanic cell formation described above, the regime in which silicon dissolution occurs and the respective etch rate can be controlled by varying the concentration of the oxidizing agent and/or changing the metal electrode; i.e. either porous silicon formation or electropolishing can occur. For example, a Pt electrode in contact with silicon in a relatively strong oxidizer such as H_2O_2 may correspond to curve (c) or (d) depending on the concentration of the peroxide. For a gold/Si combination in a solution containing either oxygen or H_2O_2, the shift in potential is small (31), and the system may correspond to curve (b) in **Figure 2.10**.

It is important to note that in addition to selection of metals, the oxidizing agents should

be carefully chosen so that they are not reduced at the silicon surface, which will lead to the chemical dissolution of silicon without the presence of metal catalysts. This is in contrast to stain etching where the electrochemical dissolution of silicon by only HF and an oxidant is desired.

A similar mixed potential theory was also used by Goristiza and co-workers to explain porous silicon formation during the electroless deposition of Pt in fluoride solutions onto Si (33). They explained the process by constructing an energy diagram at the interface, shown in **Figure 2.11**. In the absence of metal ions, the Fermi level in n- and p-type silicon lies close to the redox potential of H^+/H_2. Hole injection in this case is not likely because there is no overlap between the electron acceptor level of the H^+/H_2 system and the silicon valence band. The addition of Pt^{2+} ions in the electrolyte solution moves the potential of the solution closer to the valence band of silicon, making hole injection into the semiconductor valence band possible. For n-type silicon, the band bending keeps the injected holes close to the surface, which promotes silicon dissolution after hole capture. For p-type silicon, the decrease in band bending lowers the barrier height which helps promote thermionic emission of holes over the barrier, also leading to silicon dissolution. It is worth noting that the actual surface which is composed of Pt clusters and naked silicon is heterogeneous. As a result, some modification of the band diagram is needed. Nonetheless, the underlying physics remains the same.

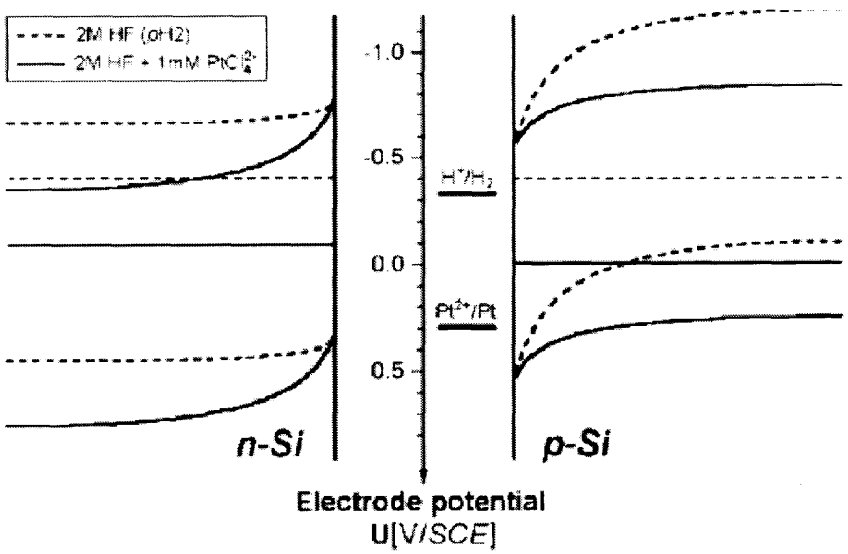

Figure 2.11 Experimental energy diagram at the Si-electrolyte interface. The dotted lines represent the situation of a fluoride blank solution, and the solid lines represent the situation where 1 mM of Pt^{2+}/Pt is added in the solution (33).

It is also interesting to note that no porous Si formation was observed in the electroless deposition of Ni on silicon in fluoride solutions (34). This is because the Ni^{2+}/Ni system has a potential that lies in the bandgap. The resulting band bending in this case is therefore not enough to promote dissolution.

The concept of using the catalytic properties of noble metals to produce porous silicon was developed by Bohn and co-workers by directly depositing nanometer-size metal catalyst particles onto the silicon surface prior to etching (35). By studying the etching characteristics of p^+, p^-, and n^+ Si substrates using metal-assisted etching, it was found that, in contrast to the anodization approach, this etching approach can generate porous silicon *regardless of doping type and level.* Similar to etching results based on galvanic cell formation (32), the observed etch rate was much higher for Pt than Au, again suggesting a catalytic role.

Li *et al.* proposed the following reaction scheme involving local redox reactions at local anode (Si) and cathode (metal) sites to explain the etching:

$$\text{Cathode: } H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \text{ and } 2H^+ + 2e^- \rightarrow H_{2(g)} \quad [2.6]$$

$$\text{Anode: } Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \text{ and } SiF_4 + 2HF \rightarrow H_2SiF_6 \quad [2.7]$$

$$\text{Overall: } Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_{2(g)} \quad [2.8]$$

Hole injection in this case is provided by the reduction of H_2O_2 on the metal catalyst particles (**Equation 2.6**]). They also observed limited etching *away* from metal-coated areas, possibly due to the lateral transports of charge carriers.

The catalyst metal can also be patterned to pattern the resulting porous film. This was demonstrated by Chattopadhyay and Bohn using focused-ion-beam assisted maskless deposition of Pt (36). Pattern sizes ranging from 1 μm to 20 μm were produced. The resulting silicon structure was highly non-uniform, with a central porous region surrounded by some very deep craters. They attributed this morphology to the non-uniformity in Pt deposition during FIB patterning. However, as shown in **Chapter 3**, the same type of uneven morphology was also observed for electron beam evaporated films patterned using lift-off. The observed uneven etching is more likely related to a size effect than a result of the FIB patterning. The size-dependent etching behavior was further confirmed by the observation that different

morphological characteristics of etched silicon were observed to be dependent on the distance from the edge of a patterned Pt-coated area (37).

Another important characteristic of metal-assisted etching is the localized etching of silicon in proximity to the metal catalysts. The localized etching could be due to a faster surface dissolution reaction than lateral hole diffusion, or a lower energy barrier for holes at the silicon-metal interface than at the silicon-electrolyte interface (38). Although the exact reason is not clear at this point, the localized etching makes metal-assisted etching a very versatile method to pattern silicon. For example, in anodized silicon, the pore sizes and morphologies are determined by the semiconducting properties of the material (20). As a result, the formation of long vertical macro-channels in lightly-doped p-type Si or small micropores in heavily-doped silicon is not likely. The limitation does not apply to metal-assisted etching as the pore size is determined solely by the size of the metal catalysts and in some cases, the electrolyte composition, as discussed in the next section.

2.4.2 Etchant solution composition dependence

Chartier *et al.* observed that different regimes of dissolution occur in metal-assisted etching depending on the relative amount of HF and H_2O_2 (38). As shown in **Figure 2.12**, four regimes were observed at different ratios of HF: porous Si, simultaneous formation of microporous and porous Si, craters, and a polished surface. Here, porous silicon is used to indicate the pores formed as a result of silicon etching in close vicinity to the metal.

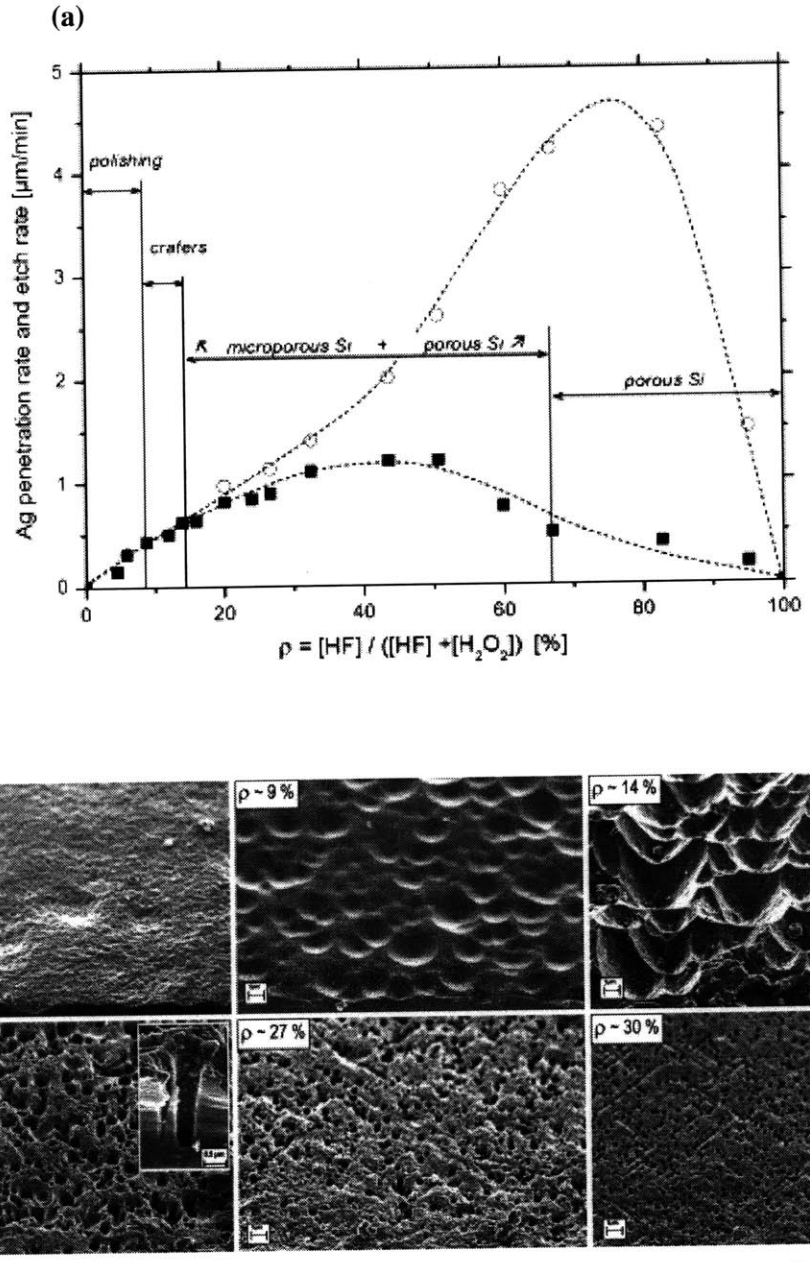

Figure 2.12 (a) Etch rates as a function of the molar ratio of HF: $\rho = [HF]/([HF] + [H_2O_2])$. Open circles: penetration rate of Ag nanoparticles. Filled squares: HF-H_2O_2 etch rate. (b) SEM images of p-type Si (100) samples after HF- H_2O_2 etching for different values of ρ (38).

An argument similar to that used to explain the three regimes of silicon anodic dissolution is proposed to explain this dependence. As described in **Section 2.2.1**, the final morphology of

anodized silicon is controlled by both the current density and the electrolyte (HF). In metal-assisted etching, the HF concentration controls the surface dissolution chemistry in a similar manner. The oxidant concentration, on the other hand, is considered to be the equivalent of current density in an anodization approach

The following overall reaction is proposed to summarize etching in all regimes.

$$Si + 6HF + nh^+ \rightarrow H_2SiF_6 + nH^+ + \left[\frac{4-n}{2}\right] H_2 \qquad [2.9]$$

Similar to the case of silicon anodization, the valence number *n*, represents the number of charge carriers flowing in the system per silicon atom dissolved. This number varies from 2 to 4. An *n* value of 2 corresponds to the porous silicon formation regime at below the critical current density. The dissolution reaction in this regime is described by

$$Si + 4HF_2 \rightarrow SiF_6^- + 2HF + H_2 + 2e^- \qquad [2.10]$$

Note that one hydrogen per dissolved Si atom is evolved in this case. This is because in the absence of a counter electrode (like in the case of galvanic cell formation), a reduction step must also occur on the substrate. The most commonly assumed counter reaction is hydrogen ion reduction (39). As a result, bubble formation is usually observed during metal-assisted

etching which might sometimes cause non-uniformities in the resulting porous silicon structure. It may be possible to solve this problem by adding alcohol or a surfactant in the etchant solution (17).

When $n = 4$, an oxidized intermediate species such as SiO_2 may form. This corresponds to the electropolishing regime in silicon anodization. The dissolution reaction in this regime can be described by

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \qquad [2.11]$$

$$SiO_2 + 2HF_2^- + 2HF \rightarrow SiF_6^{2-} + 2H_2O \qquad [2.12]$$

In this regime the etching should be isotropic as SiO_2 dissolution in HF is known to be an isotropic process (40).

The four etching morphologies shown in **Figure 2.12** can be now be summarized as follows. Note that ρ is defined as $[HF]/([HF] + [H_2O_2])$ where the quantities in square brackets represent the concentration.

- ✧ *Pore formation*: A high ρ is needed for silicon etching to be confined to the Si-metal interface. This is because all the holes produced in the reduction of H_2O_2 are consumed by HF etching away the locally oxidized silicon. For the fabrication of silicon nanowires by metal-assisted etching, a high ρ is therefore preferred.

✧ *Simultaneous formation of microporous and porous silicon*: in **Figure 2.12(a)**, between ρ = ~ 40 - 80%, the Ag particle penetration rate decreases while the HF- H_2O_2 etch rate (calculated from the total mass loss) increases; i.e. holes are being consumed at the pore walls, leading to Si dissolution *away* from the pore tips. This is quite similar to the case of macropore formation in n-type Si substrates discussed in **Section 2.2.3**. That is, when the reaction is controlled by the mass transport of HF into the pores, holes begin to penetrate into the walls and cause dissolution to occur away from the tips. As a result, cone-shaped pores with an opening diameter larger than the Ag particle diameter are formed. One such pore is shown in the insets in **Figure 2.12(b)**.

✧ *Crater formation*: Micron-sized craters with a rounded morphology are formed at ρ = 9 – 15%. This could be the result of mixed porous silicon formation and electropolishing.

✧ *Polishing regime*: At a very low ρ value, a thick oxide layer is formed over the entire substrate surface, leading to isotropic etching. As a result, the substrate surface appears to be macroscopically smooth. No hydrogen evolution was observed in this regime, as expected according to **Equation [2.9]**.

In addition to the relative concentration of HF to the oxidant, the choice of catalyst metal also plays an important role in determining the regime in which silicon dissolution occurs. In their initial studies of metal-assisted etching, Tsujino and Matsumura found that even when etching takes place under exactly the same conditions (i.e. same etchant solution concentration,

temperature, and etc.), the resulting silicon morphology can be very different depending on the types of metal catalyst employed (41). For example, when a Si(100) substrate covered with Ag nanoparticles was etched in a mixed solution of 10% HF and 30% H_2O_2 (10:1 v/v, corresponding to ρ = 76%), a microporous film roughly 300 nm thick covered the vertical channels drilled into the Si by the Ag nanoparticles. However, when Pt particles were used as the catalyst, the microporous Si layer became as thick as 3 μm. The result is consistent with what Kelly and coworkers observed in the formation of a Galvanic cell when Au and Pt were connected to Si in a solution of HF and an oxidant (31). A similar explanation based on the catalytic abilities of the metals might be used to explain this difference in etching behavior. Pt, for example, is known to be a very good catalyst for the decomposition of H_2O_2. As a consequence, the resulting "local current density" is a lot higher compared to when Ag catalysts are used.

Another factor that may influence the etching regime is particle density. Yae *et al.* found that for the same etchant concentration and etching time, the Si sample is polish-etched at higher particle densities while macropores are formed when a lower density was used (42). This is also similar, though not entirely comparable, to the case of Galvanic cell formation in which a lower current density corresponds to a smaller metal electrode area compared to the silicon area (32). To the author's knowledge, there has not been a systematic study to date comparing the influence of different catalyst metals on the onset of the different etching

regimes as a function of the etchant concentration.

2.4.3 Crystallographic orientation dependence

Similar to the electrochemical etching of silicon, metal-assisted etching also depends on the crystallographic orientation of the Si substrates. In both cases, etching proceeds preferentially in <100> directions. Tsujino and Matsumura were the first to report inclined holes when a (111) oriented Si wafer was used for etching (43).

The crystallographic orientation dependence can be affected by two factors: (i) the geometric characteristics of the catalyst; and (ii) the relative concentrations of the oxidant and HF. The effects of each are discussed below.

✧ *Catalyst morphology*

The geometric characteristics of the catalyst particles are found to influence the pore morphologies. For example, Tsujino and Matsumura found that although etching generally proceeds in the expected <100> direction on a Si (100) substrate, horizontal pores in the [010], [0-10], [001], and [00-1] directions are also observed. A closer examination of the particle shapes revealed that in the vertical [100] pores they were mostly spherical, whereas in the horizontal pores the Ag particles were mostly semi-spherical or irregularly-shaped (44).

On non-(100) oriented substrates, the etching direction is also dependent on the morphology of the deposited metal catalyst. For example, Huang *et al.* found that on Si (110) substrates, the etching direction is found to be in the crystallographically preferred <100>

directions in the case of isolated metal particles or for a small-area metal film with perforating nanoholes (Z. Huang, 2009). However, when the overall area of the metal film is suffciently large, etching can be forced to proceed in the vertical [-1-10] direction. We have shown that in addition to having a metal mesh, the inter-hole distance in the metal catalyst film also plays an important role in determining the etching direction. These results are discussed in detail in **Chapter 6**.

✧ *Oxidant concentration*

Tsujino and Matsumura found that pore morphologies of a (100)-oriented silicon wafer were also dependent on the etchant concentration. They observed that cylindrical holes grew preferentially in the <100> direction at low HF concentrations and helical or winding holes formed at a high HF concentration for both Pt (41) and Ag (44).

The etching direction of non-(100)-oriented Si substrates were also found to be influenced by the concentration of oxidant in the etching solutions (45). At low oxidant concentrations, the etching was found to proceed in the crystallographically preferred <100> direction. However, at sufficiently high oxidant concentrations, pores were found to grow in an etching direction normal to the substrate surface, regardless of the substrate orientation. A model similar to that proposed by Chartier *et al.* (38) was used to explain this dependence. As discussed in **Section 2.2.1** and **Section 2.4.2**, for both the electrochemical etching and metal-assisted etching of silicon, two competing dissolution processes occurring at the surface

determine the final morphology of the etched silicon, namely, the direct dissolution of silicon in the divalent state, and the dissolution of SiO_2 formed as an intermediate state. The two dissolution reactions are summarized in **Equations [2.10]** and **[2.12]**, respectively. When the peroxide concentration is sufficiently high, the latter reaction prevails as the dissolution rate is slower than the formation rate of the oxide. Etching proceeds in a vertical direction (normal to the wafer surface) in this case. In contrast, if the peroxide concentration is relatively low, dissolution of divalent silicon dominates. Etching in this case is orientation-dependent.

A change in etching direction from vertical to <100> on non-(100) oriented substrates was also observed for etchant solutions with an initially high oxidant concentrations. This was ascribed to a diffusion effect by Huang *et al.* As etching proceeds, the concentration of the oxidant near the etching front is reduced and must be resupplied by diffusion from the bulk solution (45). However, HF is also consumed during the reaction. For example, if **Equation [2.9]** holds, then 6 HF are consumed per dissolved Si atom for both $n = 2$ and $n = 4$. In addition, if mass transfer in the pores occurs by diffusion, one can also expect a linear decrease in HF concentration along the pore lengths, from Fick's first law. A closer examination of the relative consumption rates of HF and H_2O_2 rate is needed to confirm this model.

In a similar study of control of the etching direction, Chen *et al.* explained the change in angle during metal-assisted etching using an argument based on the different potential barriers the Ag catalysts must overcome to change etching directions (46). They found etching to

proceed in the vertical <111> direction on a (111)-oriented Si substrate when etching at a low oxidant ($AgNO_3$) concentration and low temperature. In contrast, when etching was carried out with a higher oxidant concentration at a higher temperature, they found three types of "zigzag" wires with different orientations on the *same* sample: (I) <111> and <113>; (II) <111> and <100>, and (III) two orthogonal <100> directions. A schematic illustration of the zigzag wires and their proposed etching mechanism is shown in **Figure 2.13**.

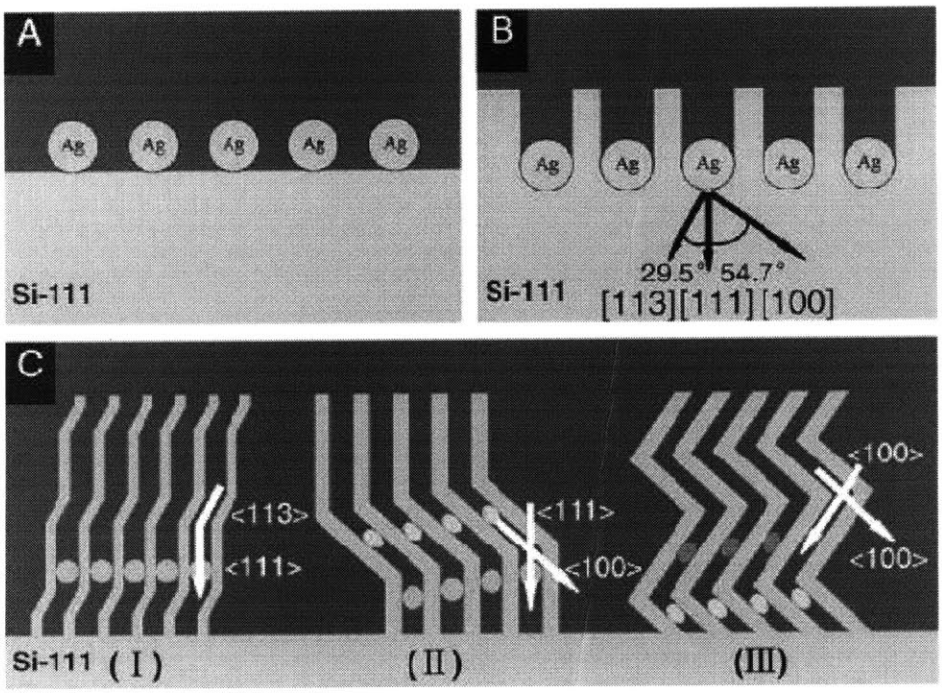

Figure 2.13 A schematic showing the proposed etching process of zigzag Si nanowires fabricated at a relatively high oxidant (silver nitrate) concentration and a relatively high etching temperature (46).

The low temperature behavior is consistent with the observations reported by Huang *et al* (45). However, according to Huang *et al.*, at a higher oxidant concentration, vertical etching resulted due to formation of an intermediate SiO_2 state. A possible explanation for this is the

different oxidizing strengths of $AgNO_3$ and H_2O_2. Also, the high and low $AgNO_3$ concentration used in their study is 0.02 and 0.04 mM, respectively, whereas in the study carried out by Huang *et al.*, the concentration differs by as much as 20-fold. For the concentrations used in this study, the local "current density" may simply not be high enough for oxide formation, and the observed difference could be more attributable to the higher temperature used.

Chen *et al.* proposed that in some cases the etching proceeded in the vertical <111> direction initially due to the large angle between the <100> and the <111> directions. For type (I) wires, they suggested that the switch to the <113> direction is due to perturbations (e.g. caused by hydrogen bubbles) which allows the silver nanoparticles to switch from the <111> direction to a nearby <113> direction. They also suggested that the switchback from <113> to <111> is due to energy considerations; i.e. since the <113> orientation is not energetically favorable, the Ag nanoparticles may switch back to the <111> direction as etching time increases. The alternating angle is due to a repeated perturbation and switchback process. For wires of type (II) and (III), they suggested that the switch to the crystallographically preferred <100> direction is a result of the higher etching temperature and Ag ion concentrations, aiding the silver nanoparticles to overcome the potential barrier to switch from the original <111> direction to the lowest energy <100> direction.

Although the model proposed by Chen *et al.* has its merits, some doubts and

inconsistencies remain about the exact mechanism responsible for the switch in etching directions. For example, although it is possible that the higher temperature might help Ag catalysts overcome the energy barrier to switch directions, it is also likely that the higher temperature simply enhances mass transport (47). If the HF can remove the silicon at a faster rate, etching of silicon in the divalent state can dominate over the isotropic etching of a silicon dioxide intermediate state, resulting in etching along the preferential <100> directions.

Concerning the relative energies of different crystallographic directions, Chen *et al.* proposed that for type (I) wires, etching switches back from <113> to <111> because the later is more energetically favorable. However, in some reports, both <100> and <113> have been identified as prevalent etching directions in the electrochemical etching of silicon (18), suggesting that the <113> direction is more energetically favorable than the <111> direction. This is contradictory to what Chen *et al.* suggested. Also regarding the model proposed for type (I) wires, it is well-known that the pressure in a gas bubble is size-dependent ($\Delta P = 2 \times 2\gamma/R$, where γ is the surface tension and R is the radius of the bubble) (48). For bubble diameters less than a few micrometers, the pressure is much larger than the ambient pressure, causing the diameter of the bubble to increase to the size of the etched pores almost immediately after they are formed. As a result, mass transport (for both the HF and $AgNO_3$), and hence the etch rate, is reduced in pores where bubbles were generated. If the alternating angle of type (I) wires is indeed caused by perturbations due to collective bubble formation in

every pore, the silver penetration distance should be much smaller compared to type (II) and (III) wires. However, that is not what is observed in the SEM images.

Moreover, if as suggested, the switching in etch directions is indeed due solely to energy considerations and the Ag catalysts initially proceed along the vertical <111> direction simply due to the large angle between <111> and <100>, then for type (II) wires, once the switch to <100> has occurred, there is no good energetic reason for the etching direction to change back to <111>. Similarly, for type (I) wires, once the switch to the <113> direction has occurred, it should be much easier to convert to one of the most energetically favorable <100> directions (e.g. the angle between [113] and [001] is 25.2°, smaller than the angle between [113] and [111]).

2.4.4 Dopant dependence

Zhang *et al.* carried out a study of the morphological dependence of catalytically etched silicon on the dopant type and concentration (49). Ag catalysts were deposited electrolessly via Galvanic displacement on the silicon samples prior to etching in HF and H_2O_2. Several observations were made, as summarized below. First, comparing lightly and heavily doped p-type silicon, the heavily-doped wires have a lower density, length and diameter in general. Second, comparing p-type (111) and n-type (111) silicon, p-type silicon produces wires in the <100> direction at an inclined angle to the surface whereas n-type silicon produces vertically-aligned wires in the <111> direction. Lastly, TEM examination reveals a rougher

surface on heavily-doped p-type silicon nanowires compared to lightly-doped material. Although no explanation was provided in their work for the different etching directions between p-type (111) and n-type (111) silicon, since they used two different oxidant concentrations for the two samples (0.15 M for p-type sample, and 0.4 M for n-type sample), no direct comparison can be made. The higher oxidant concentration used for the n-type sample may lead to etching in the SiO_2 formation regime, as discussed in previous section. For the difference in density and geometry of the wires between heavily and lightly doped silicon samples, they suggested that the higher "activity" in electron transfer because of the higher carrier concentration in heavily-doped silicon is responsible for the faster etching.

An argument based on the electroless deposition of Pt from fluoride solutions (P. Gorostiza, 2003) may also be used to explain this dependence. For p-type silicon, a higher carrier concentration leads to a smaller band bending. This can be seen in **Figure 2.11**. The redox potential of Ag^+/Ag lies below the silicon valence band. A higher dopant concentration (i.e. a lower Fermi energy) leads to a smaller degree of band bending, promoting the thermionic emission of holes as discussed in the Beale model (**Section 2.2.3**). This may also be the reason that more heavily-doped wires have a rougher surface. However, this may not be true for n-type wafers, as a higher dopant concentration will only lead to greater band bending.

A similar approach was also used by Hochbaum *et al.* to produce mesoporous silicon nanowires (50). By soaking heavily-doped p-type silicon wafer pieces in an etching bath

comprised of $AgNO_3$ and HF for prolonged periods (for both the electroless deposition of Ag and metal-assisted etching), silicon nanowires with a mesoporous surface were obtained.

2.4.5 From porous silicon to silicon nanowires

A number of studies have appeared in the past decade involving various porous structures fabricated using metal-assisted etching, some of which are summarized in the previous sections. The metal-assisted approach is not limited to only the fabrication of pores. Because of the localized nature of etching, the metal catalyst can be patterned in such a way that wires instead of pores are fabricated. The first report of silicon nanowire formation using metal-assisted etching was demonstrated by Peng and co-workers, as shown in **Figure 2.14**. By first forming an interconnected network of Ag catalyst using electroless deposition in HF and $AgNO_3$, films composed of vertically-aligned silicon nanowires were fabricated (51). Following their work, many novel methods have been developed to pattern the metal catalyst and thereby the silicon nanowire arrays. These methods are discussed in detail in **Chapter 5**.

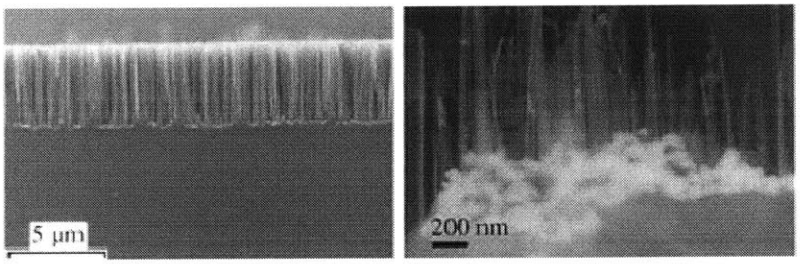

Figure 2.14 Cross-sectional SEM micrograph (left) and TEM micrograph (right) of a porous silicon film composed of vertically-aligned silicon nanowires. The Ag catalyst can be clearly seen at the interface between the silicon substrate and the silicon nanowires (51).

2.5 Conclusion

It should be clear from this review that, mechanistically, the dissolution chemistry is similar for the anodization, photo-assisted etching, and electroless etching (including stain etching and metal-assisted etching) of silicon. In all cases, electronic hole production in the valence band is the crucial first step in the etching reaction. The major difference is how the electronic holes are supplied. For anodization, the holes are supplied by the application of a potential with an external voltage source. For photo-assisted etching, photo-generated electron-hole pairs are created via surface irradiation and are responsible for initiating silicon dissolution. For stain etching, the local current on the silicon surface is driven by reduction of the oxidizing species present in the etchant solution. For metal-assisted etching, the injection of holes is achieved by metal catalysts on the silicon surface drawing electrons from the silicon valence band for the reduction of the oxidizing species in the etch solution.

For all the etching methods discussed in this chapter, different etching regimes can be identified. In the porous silicon formation regime, the initial oxidation step increases the Si oxidation state to a more positive value *without* forming an actual oxide layer. In the electropolishing regime, an oxide is formed as an intermediate state followed by chemical dissolution of the oxide layer. Whether electropolishing or porous silicon formation occurs is controlled by the relative rate of oxidation via hole injection to the rate of etching by the fluoride solution. If the former is greater, electropolishing will occur and etching is isotropic.

If the etch rate exceeds the rate of oxidation, porous silicon will be formed, and etching in this case is anisotropic and maximum in the <100> directions. In anodized etching, this can be controlled by controlling the current density and the HF concentration. In metal-assisted etching, the current density is controlled by *both* the oxidant concentration and the catalytic abilities of the metal. The HF concentration and the temperatures can also, to a limited extent, be varied to affect mass transport characteristics in a similar manner to anodization.

Other parameters of metal-assisted etching affecting the porous silicon morphology, such as the dopant concentration and catalyst geometry, were also summarized. The dopant concentration influences etching by changing the barrier height and width at the interface, and the catalyst geometry can help suppress the crystallographically preferred <100> directions in non-{100} oriented samples. A comprehensive understanding of all the control parameters is essential in controlling the process and the resulting structure. Unfortunately, so far there has not been a systematic study on metal-assisted etching which takes into account all these parameters. Nevertheless, based on the review presented in this chapter, with the aid of an extensive understanding of silicon anodization, such systematic study should be carried out with relative ease using similar analysis techniques.

Chapter 3. Metal-Catalyzed Etching Mechanism: Electrochemical Etching or Oxide Overlayer Formation

3.1 Introduction

Pore formation in many semiconductor materials under anodic conditions is a well-known phenomenon. In particular, porous silicon, which was first reported almost half a century ago during the electropolishing of silicon in aqueous hydrofluoric acid (HF) has been studied since 1956 (52). The anodization approach, however, requires conducting substrates and often requires independent control of a relatively large number of process parameters to attain optimum results. To circumvent these problems, an electroless etching method, know as metal-catalyzed etching, has recently received significant attention. In this approach, metal particles or films are used to catalyze local silicon etching in a mixture of HF and an oxidant. This relatively simple process has been used to fabricate a number of high aspect ratio structures through patterned etching of silicon wafers. For example, we and others have used this technique to make arrays of silicon nanowires using metal catalyzed etching in conjunction with various metal patterning techniques (51) (53) (54) (55).

The current proposed model used to explain metal-catalyzed etching is reviewed in **Chapter 2**. The electrochemical model suggests that reduction of the oxidant in solution by the catalyst metal helps draw valence-band electrons from silicon, resulting in the local

dissolution of silicon that is in the direct vicinity of the catalyst into the HF solution. However, no direct experimental results have been reported to confirm this electrochemical model. In addition to the electrochemical explanation, it is also known that when a silicon substrate is covered with a gold or a silver thin film and heated in an oxidizing atmosphere at relatively low temperatures, an oxide overlayer is readily formed. This phenomenon has been observed even at room temperature. Since metal-assisted etching also involves a similar silicon-metal interface, it is also conceivable that the localized etching is caused by silicon diffusing through the metal catalyst to form an oxide layer which is subsequently etched away by HF.

In this chapter, we investigate the etching mechanism by studying the etch rate dependence and silicon morphology after metal-assisted etching as a function of the metal catalyst geometries. We begin by first presenting a more detailed literature review for the two mechanisms discussed above, and follow by presenting experimental results used to determine the etching mechanism. Based on these results, we found evidence that supports the currently proposed electrochemical model and have proposed a possible explanation for the observed post-etching silicon morphologies.

3.2 Metal-catalyzed etching model

In the following two sections, a detailed review for the two proposed etching mechanisms will be presented. Experimental design to test the two models as well as the expected trend for both mechanisms will also be discussed.

3.2.1 Electrochemical

Although the exact silicon dissolution chemistry in hydrofluoric acid is still in debate, it is generally accepted that hole injection into the silicon valence band is required for silicon dissolution into HF. A scheme suggested by Lehmann involves a surface-bound oxidation scheme in which a hole is absorbed to produce a divalent silicon oxidation state in the initial stage of silicon dissolution (56). According to this model the silicon surface is passivated against etching by silicon hydride bonds unless a hole is available.

There are several electrochemical routes to achieving this hole injection including anodic etching and electroless etching in acidic fluoride solutions, where the former requires the attachment of the silicon sample to an external circuit, and the latter achieves hole injection without any external power or photon source. In particular, hole injection in metal-catalyzed etching is achieved by the reduction of the oxidant by the metal catalysts. Based on an electrochemical reaction scheme proposed by Li *et al.*, the etching process can be regarded as two simultaneous reactions at the metal surface where the cathode reaction involves the

reduction of the oxidant species and the anode reaction involves the oxidation and dissolution of the underlying silicon (57). The overall reaction can be written as:

$$Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_{2(g)},$$

where the reduction of the peroxide is catalyzed by the metal.

The etching confinement at the silicon-metal interface can be explained by considering the existence of a charge-depletion layer around the metal catalysts which leads to a lower energy barrier for surface holes (58). The hole injection occurs predominantly near the interface as the interface has the shortest charge transport distance; i.e. holes are injected into the silicon directly underneath the metal catalysts, resulting in a localized oxidation Si state. As the HF etches away the silicon, shallow pits form underneath the metal. Eventually the catalysts will gradually sink down into the silicon surface. A schematic representation of this process is shown in **Figure 3.1**.

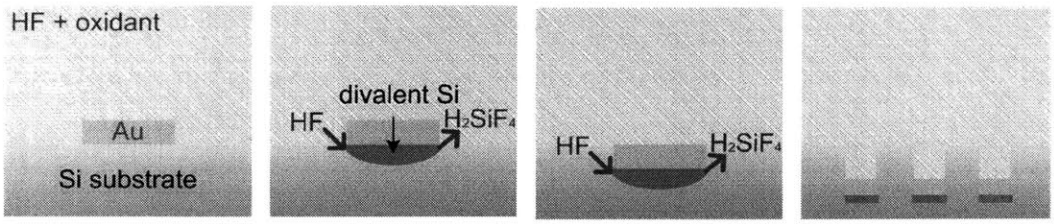

Figure 3.1 Schematic representation of the *electrochemical* model in which etching proceeds by first forming an oxidized divalent silicon layer susceptible to dissolution in hydrofluoric acid (HF) underneath the gold catalyst

The electrochemical etching can be regarded as an etching process analogous to a metal thin film lift-off process or a pattern release etch process for micro-electro-mechanical systems (MEMS), where locally-oxidized silicon *beneath* the catalyst is etched away by hydrofluoric acid. The etching behavior should therefore depend on the lateral dimensions of a patterned catalyst thin film. In other words, if etching is a result of the formation of an oxidized divalent silicon state, the etch rate should increase with decreasing lateral dimension, as there is less material to be removed.

It is also worth noting that the specific activity for the reduction of O_2 of thin film Au electrodes in acidic media is independent of the Au film thickness (59). Assuming the reduction of H_2O_2 on thin film Au electrodes behaves in a similar manner, the etch rate should not be a strong function of the film thickness if the electrochemical mechanism is indeed responsible for metal-catalyzed etching of silicon.

3.2.2 Oxide overlayer formation

When a silicon substrate is covered with thin layers of gold, low temperature migration of Si atoms into the Au can occur (60). When heated in an oxidizing atmosphere, these dislodged silicon atoms can migrate through the gold thin film and accumulate on its front surface, eventually forming an oxide overlayer. The process can occur at a temperature well below the high temperatures typically required for the thermal oxidation of silicon. For example, the

dislodgement of silicon atoms and the formation of SiO_2 on top of the gold have been observed at temperatures in the range of 150 – 250°C, well below the Si-Au eutectic temperature. Recently, it was also found that a silicon oxide overshell can form on Au catalyst particles (used for vapor-liquid-solid silicon nanowire growth) at room temperature when exposed to air (61).

Native oxide growth on silicon in H_2O_2 solutions at room temperature has been reported in the literature (62). Decomposition of H_2O_2 on noble metals to produce oxidant radicals or ions may also aid oxide growth. It is therefore plausible that metal-catalyzed etching of silicon could be a result of silicon diffusing through the metal catalyst to form an oxide which is subsequently etched away by HF. A schematic representation of this process is shown in **Figure 3.2**.

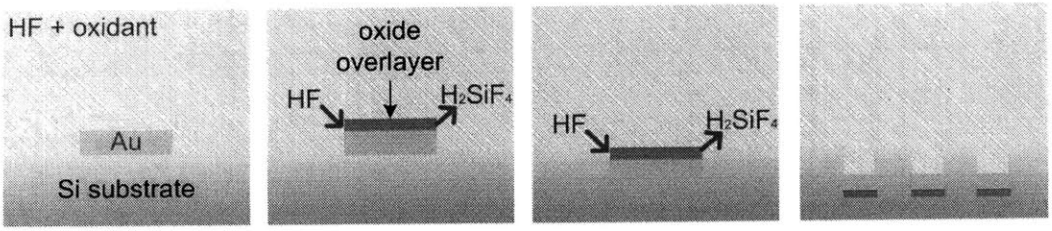

Figure 3.2 Schematic representation illustrating the *oxide overlayer formation* model in which etching proceeds by the silicon first diffusing through the gold catalyst to form an oxide overlayer which is then etched away by HF.

To better understand how this low-temperature silicon migration phenomenon can play a potential role in metal-catalyzed etching and to experimentally test this hypothesis, one must first understand the parameters that can affect the oxidation behavior. A review of the

literature is provided below, focusing on the effects of the catalyst film thickness, and the types of catalyst metals.

Hiraki *et al.* studied the effect of gold film thicknesses on the oxide formation rate by depositing gold films of different thicknesses and measuring the amount of oxide formed on the surface as a function of heat treatment time (63). Their results showed that the growth of the oxide saturates after some time and that although the initial growth rate decreases with increasing gold thickness, the saturation thickness is almost proportional to that of the original gold film. They also found that low-temperature silicon migration occurs in other metal systems such as the Si-Ag system, for which the migration of silicon atoms does not occur until 400°C, higher than the temperature required for the Si-Au system (64). In order to establish whether the silicon migration process is limited by silicon transport through the metal or silicon dislodgement at the silicon-metal interface, they compared the difference in oxidation behavior between a Si-Au-Ag double layer specimen and a Si-Ag-Au specimen heated at 200°C. The annealing temperature was high enough for oxide overlayer formation in the Si-Au system but too low for any appreciable silicon accumulation in the Si-Ag system; i.e. if silicon dislodgment is the limiting process, oxide formation on top of the Ag layer should be observed on the Si-Au-Ag double layer specimen and no oxide formation should be observed on the

Si-Ag-Au system. That is indeed what was observed. Silicon diffusion through Au and Ag is assumed to be similar at such low temperatures.

Assuming both of the above-mentioned parameters (film thickness and catalyst type) have the same effect in the solution environment for metal-catalyzed etching, through measurement of the etch rate as a function of film thickness and catalyst type it should be possible to determine whether or not this low-temperature silicon migration phenomenon plays a dominant role in the catalytic etching mechanism. In other words, if etching does occur by silicon diffusing through the catalyst thin film, then for a given catalyst metal, the etch rate should initially decrease with increasing film thickness and the etching should stop at an earlier time for thinner films. Also, the etching rate should be faster for gold than for silver as a higher activation energy is required for silicon dislodgement at the Si-Ag interface.

In addition to the Si-Au and Si-Ag system, silicon diffusion through thin layers of platinum at temperatures well below the eutectic temperature has also been observed (60). However, only a stable PtSi compound has been observed. The lack of a significant amount of silicon accumulation and silicon oxide formation over the PtSi film implies that if oxide overlayer formation is indeed the dominant mechanism for metal-catalyzed etching, platinum would not work as a catalyst for the chemical etching process.

3.3 Experimental procedures

For the etch rate dependence experiments, nanosphere lithography (NSL) was used to pattern the catalyst thin films. The process was begun by first coating a silicon substrate with a monolayer of polystyrene spheres. Silicon(100) substrates (p-type, Boron-doped, resistivity = 1 – 25 Ωcm) were first cleaned in a mixture of concentrated sulfuric acid and 30 % hydrogen peroxide (3:1 by volume) to create a hydrophilic surface for subsequent colloidal particle coating. A close-packed monolayer of polystyrene spheres was then coated on the substrate by dip-coating using a home-built dip-coater (1.2 wt% polystyrene colloidal solution coated at a coating speed of 20 μm/sec). The sample was then subjected to oxygen reactive ion etching (RIE) to reduce the sphere diameter. The final sphere diameter can be controlled by changing the RIE time. For example, for an oxygen plasma at 10 mTorr and 40 W, the etch rate is roughly 30 nm/min. With the polystyrene spheres serving as a metal deposition mask, a metal catalyst thin film was deposited using electron beam (e-beam) evaporation. The polystyrene spheres can be selectively removed by sonicating in toluene, leaving behind a hexagonal array of perforating nanoholes in the metal thin film. Finally, ordered arrays of silicon nanopillars with good fidelity to the original polystyrene sphere pattern were obtained by etching the silicon under the catalyst in a solution of hydrofluoric acid and hydrogen peroxide (10 wt% HF and 1.5 wt % H_2O_2) at room temperature in ambient light. After etching, samples were rinsed in isopropanol and blow-dried with nitrogen.

To study the etch behavior for patterned gold pads with different lateral dimensions, interference lithography and contact lithography were used to pattern the catalyst. For interference lithography, a trilayer stack consisting of an anti-reflection coating (ARC) layer, 30 nm of an ebeam-evaporated SiO_2 layer, and a photoresist layer were first deposited on a silicon (100) wafer. Square arrays of holes were created in the photoresist layer by carrying out two exposures at a 90° rotation. The pattern was then transferred into the oxide and ARC layers using CF_4 and O_2 RIE. For contact lithography, a photoresist layer was spun onto a silicon (100) wafer coated with hexamethyldisilazane (HMDS). Patterns in the photoresist layer were formed by contact lithography using a Tamarack i-line system. In both cases, the patterned photoresist layers were used as a metal deposition mask for gold evaporation. Lift-off for the interference-lithography-patterned sample was carried out by a brief immersion in diluted HF to remove the oxide layer followed by oxygen RIE to remove the ARC. For the contact-lithography-patterned sample, lift-off was carried out by soaking and sonicating the sample in acetone for roughly 1 minute. Finally, the silicon samples were etched in an HF/H_2O_2 mixture as described in the previous paragraph.

3.4 Etch rate dependence on thicknesses and lateral dimensions of patterned catalysts

As discussed in sections **3.2.1** and **3.2.2**, the reduction activity of thin film Au electrodes has no clear dependence on the film thicknesses whereas silicon diffusion through a gold thin film does. As a result, if the measured etch rate is found to be dependent on the thickness of the patterned film, this would imply that silicon is selectively etched by first diffusing through the metal catalyst and then forming an oxide overlayer. To study the etch rate dependence as a function of the film thickness, three different thicknesses of two types of catalyst metal (Au and Ag) were patterned using nanosphere lithography on p-type Si (100) substrates. The samples were etched catalytically in a solution of HF and H_2O_2 for 5 – 20 minutes. The etch depth was measured as a function of etching time. The linear etch rate is plotted for both Au and Ag in **Figure 3.3(a)**. As shown in the figure, there is no clear correlation between the measured etch rate and the film thickness for either gold or silver. For 15, 20, and 25 nm of Au, the etch rates are 99.9, 100.2, and 111.3 nm/min, respectively, and for 15, 20, and 25 nm of Ag, the etch rates are 200.9, 212.1, and 198.9 nm/min, respectively.

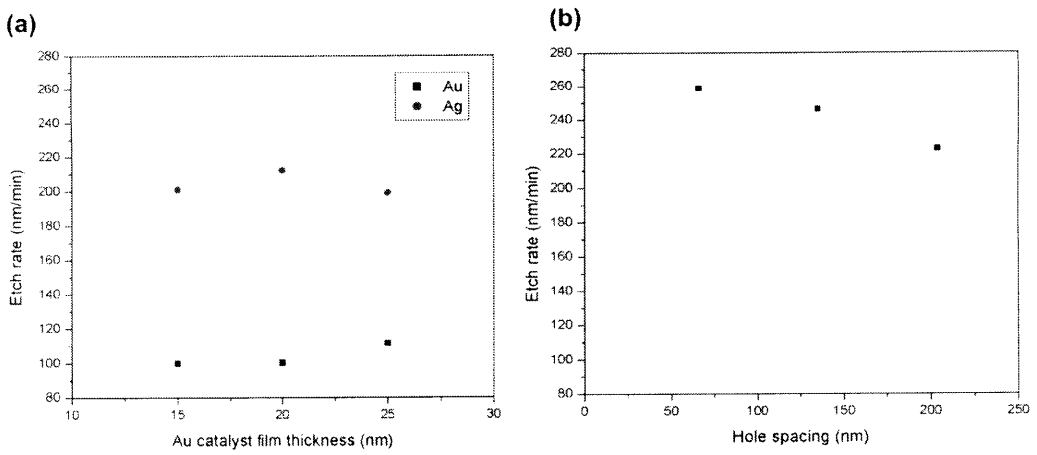

Figure 3.3 Plots showing the etch rate of silicon as a function of (a) gold catalyst film thickness, and (b) hole spacing.

The lack of a correlation between the etch rate and the film thickness for a given metal by itself is not sufficient to invalidate the oxide overlayer formation model as the range of film thicknesses is limited by the lift-off technique. However, the much higher etch rate for Ag than Au also contradicts the oxide overlayer formation model since the activation energy for silicon dislodgement is higher for the Si-Ag system than for the Si-Au system, as discussed in section **3.2.2**. The difference in etch rate suggests a catalytic role. H_2O_2 reduction on gold in acidic media is slow (59) whereas Ag is known to have a good catalytic activity for hydrogen peroxide decomposition (65). Similar results have been observed for Pt, another good catalyst for H_2O_2 reduction. The etch rate was observed to be much higher for Pt than Au (57). Since only a stable SiPt compound rather than an oxide overlayer is formed for the Si-Pt system, this again suggests that the oxide overlayer formation mechanism cannot be used to explain the silicon etching.

According to the electrochemical model, etching occurs from underneath the catalysts where an oxidized divalent silicon layer is first formed. The etch rate in this case should increase with decreasing lateral dimensions of the catalyst. To study this etch rate dependence, nanosphere lithography where the polystyrene spheres were subjected to oxygen RIE for 4, 6, and 8 minutes were used to pattern silver catalyst films on p-type Si (100) substrates. The resulting hole spacings, or the distance between two nearest-neighbor nanoholes, were 204 nm, 135 nm, and 66 nm. **Figure 3.3(b)** shows the measured etch rate as a function of the hole spacing. As shown in the figure, the etch rate increases with decreasing hole spacing, confirming the expected trend for the electrochemical model. However, since hole spacing control in nanosphere lithography is also limited by lift-off, other metal film patterning techniques were used to study the etching behavior with a greater range of lateral dimensions. The results are discussed in the next section.

3.5 Silicon morphology after etching as a function of the catalyst lateral dimensions

An investigation of the effect of the pattern width on the etching behavior is carried out by etching p-type Si(100) samples with metal catalysts ranging from several hundreds of nanometers to several tens of micrometers in lateral pattern dimensions. Scanning electron microscopy (SEM) images of representative etching results using patterned catalyst films with

lateral dimensions of 130 nm, 6 μm, and 95 μm (denoted as sample A, B, and C, respectively) are shown in **Figure 3.4**. Sample A was patterned using interference lithography; sample B and C were both patterned using contact lithography as described in the experimental section. **Figure 3.4(d)** shows one edge of the etched silicon from C after removal of the gold catalyst using a commercially available iodine-based gold etchant. Etching time was 10 minutes for A and 1 hour for samples B and C in etchant solutions of the same strength.

As shown in the SEM images, the final morphology of the etched silicon is different for all three cases. For sample A, the smallest gold pad, the catalyst successfully drilled down into the silicon substrate. However, for sample B and C, despite the much longer etching time, the micron-sized gold pads failed to etch into the silicon. Instead, small empty "pockets" were found underneath the entire gold pad for sample B and near the edges of the gold pad for sample C. In addition, the original Au catalyst films also appeared to be wrinkled after etching was completed.

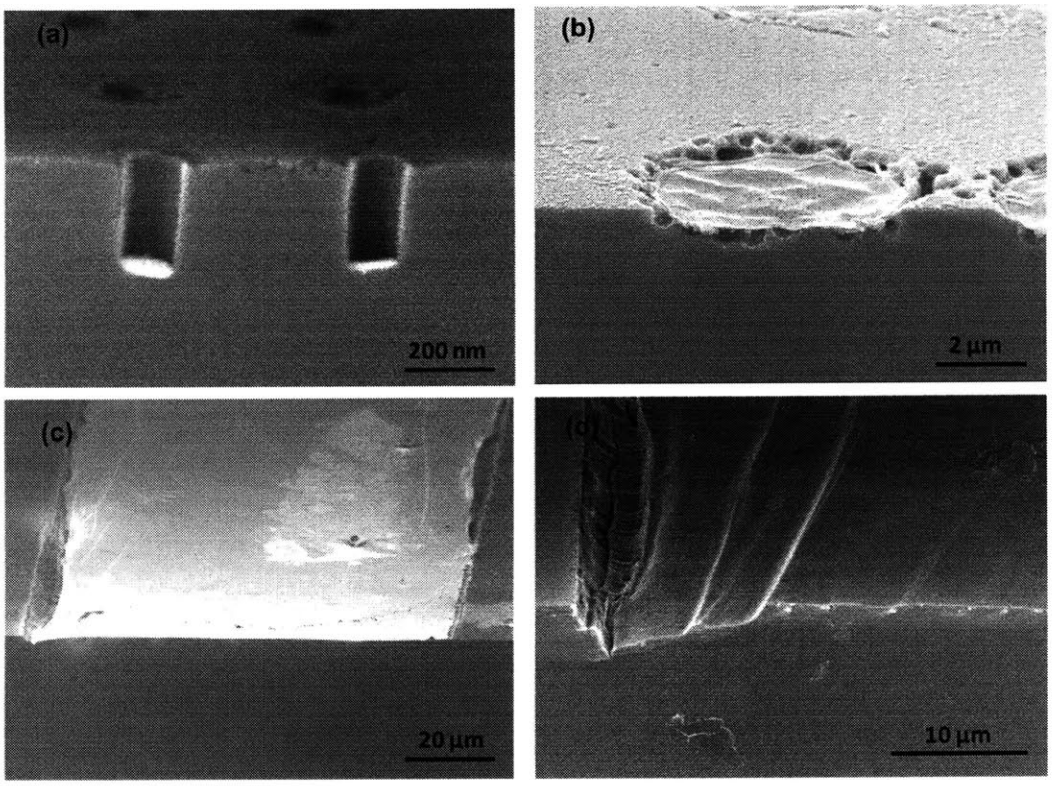

Figure 3.4 Scanning electron microscopy (SEM) images showing etching results on patterned Au catalyst pads of three different lateral sizes: (a) 130 nm, (b) 6 µm, and (c) 95µm. Figure (d) shows a higher magnification image of one edge from sample C after the Au catalyst has been removed.

This difference in the etching behavior can only be explained if etching occurs from underneath the metal catalyst thin film. As illustrated in the schematics in **Figure 3.5**, an oxidized divalent silicon region exists in the vicinity of the metal catalyst which is then etched away by hydrofluoric acid. Since it is essential that the HF has access to the silicon underneath the metal during the etching process, the Si-metal contact must be intermittent during the etching process. For the smallest pads, the dissolution of the divalent silicon layer into HF proceeds fast enough to create a pit underneath the entire catalyst, eventually causing the gold pads to sink into the silicon substrate, as shown in **Figure 3.5(a)**. For the medium-sized pads, a

divalent silicon layer is also formed underneath the metal. However, because of the larger size of the metal catalyst film, as the HF etches away the silicon near the edge of the catalyst film, the film edge loses contact to the silicon momentarily until it reattaches itself to the silicon to form another divalent silicon region. As the HF gradually etches away these newly formed divalent silicon regions, small empty pockets are formed, as shown in **Figure 3.5(b)**. For the largest pads, etching initially proceeds in a similar manner to the medium-sized pads. However, as the gold film gradually becomes more wrinkled near the edges, it becomes increasingly difficult for the HF to reach the central regions. As a result, only the silicon near the catalyst film edges is etched away initially, as shown in **Figure 3.4(d)**. Note that the etched edge has a width of roughly 4.5 μm, which is of the same order of magnitude as the lateral dimensions of the medium-sized pads. If the sample is subjected to etching for sufficiently long, the HF might still be able to etch through the newly-formed oxidized Si regions under the reattached gold to eventually reach the silicon near the center part of the catalyst. **Figure 3.6** shows an SEM image of a large pad etched in the same solution for 19 hours. The empty pockets are clearly visible near the edges and on the sidewalls of the etch pits, possibly due to the random nature of gold reattachment to silicon in solution. In some cases, the catalyst film was completely delaminated during the process.

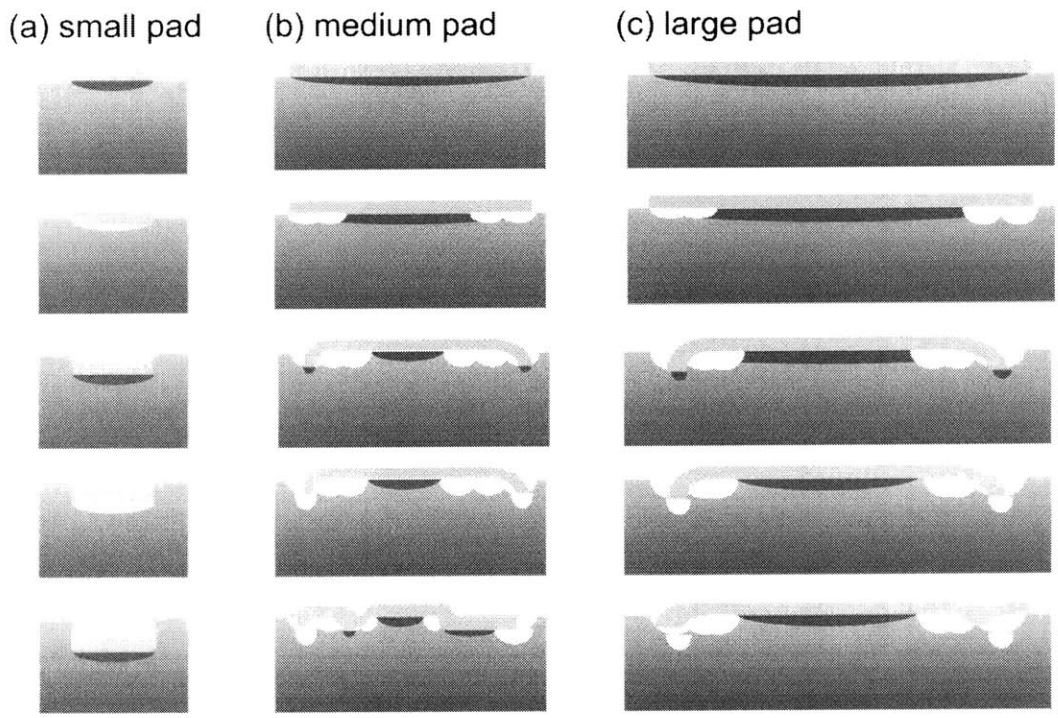

Figure 3.5 Schematics showing different etching behaviors as a function of the lateral dimensions of patterned catalyst pads [(a) small, (b) medium, and (c) large] based on the electrochemical model for metal-catalyzed etching.

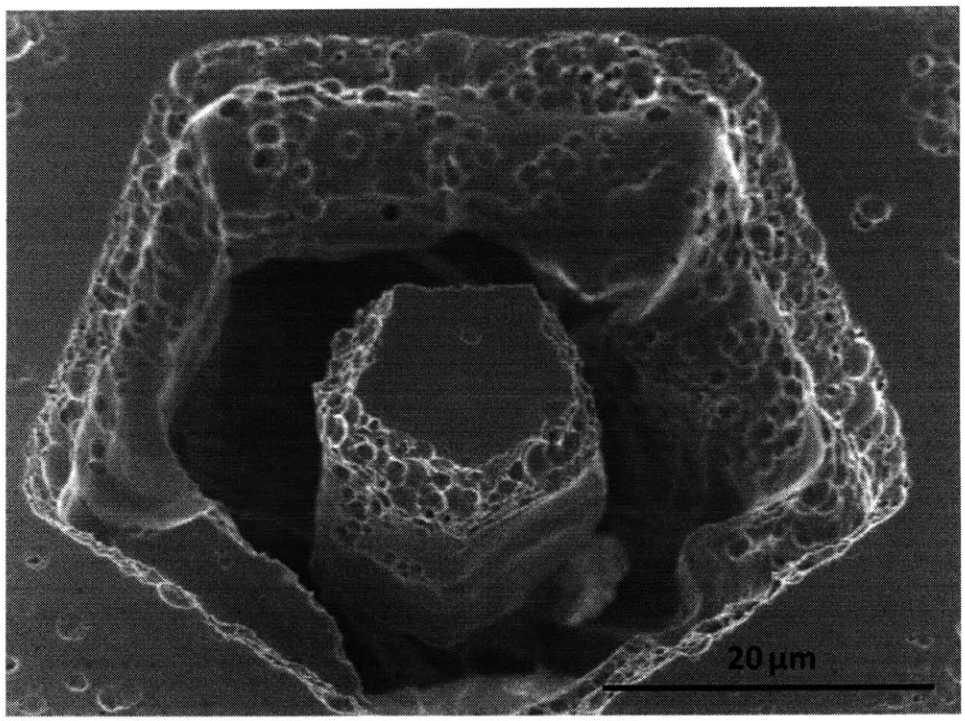

Figure 3.6 SEM image of a large Au pad patterned using contact lithography etched in HF-H_2O_2 solution for 19 hours.

As described in the previous paragraph, the HF must have access to the silicon-metal interface in order for the catalyzed etching to proceed. In the case of patterned continuous metal films, HF can only etch away the silicon from the edges of the catalysts. By creating perforating holes in these patterned films, more of the silicon-metal interfaces are exposed to the etchant solution; i.e. etching can occur both from the edges of the metal films and from the edges of the holes. As a result, etching should proceed successfully. This is demonstrated by patterning a medium-sized Au catalyst film with perforating holes using templated self assembly of polystyrene spheres. The patterned Au pads with nanoholes and the results of etching are shown in **Figure 3.7**. As shown in the figure, although the overall pad size is the same as the pads shown in **Figure 3.4(b)**, etching occurred as the HF can easily access the silicon-metal interface at the perimeters of the perforating holes. **Figure 3.7(c)** shows an interesting case where the perforating holes are only patterned near the edges of the metal films due to poor self-assembly in this region. As a result, the central region, which is in essence a micron-sized continuous Au pad, etches much slower compared to the edges. Since the edges cannot break free, the two sides continued etching down into the silicon at an angle whereas the center region becomes wrinkled due to formation of the empty pockets underneath. In a similar manner, if holes can be created in the largest pads, etching should also occur. This was demonstrated by annealing the Au pads on a hotplate to allow the film to slightly dewet.

Etching results, shown in **Figure 3.7(d)**, confirmed that an etch depth of roughly 10 μm was achieved.

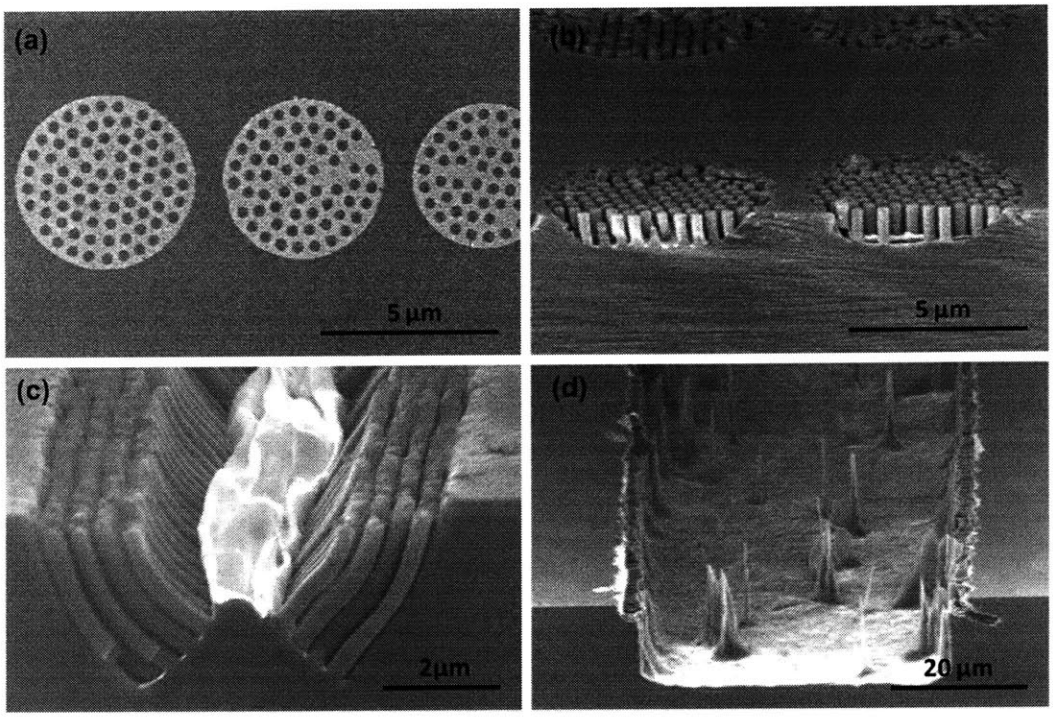

Figure 3.7 SEM images of (a) Au pads with perforating holes patterned using templated self assembly of polystyrene spheres; (b) etching results using the patterned pads as the catalysts; (c) non-uniform etching for films with patterned holes only near the edges; and (d) etching for a slightly dewetted large-area gold film.

This interesting behavior might be utilized to create through-wafer holes by first creating perforating holes in a catalyst film, and removing the fine wires extruding from these holes using an isotropic etch after metal-assisted etching. In addition, by patterning perforating holes in a catalyst film using nanosphere lithography, we have demonstrated the fabrication of a "pillar-in-trench" structure, shown in **Figure 3.8**. Detailed film patterning process is described in **Chapter 4**.

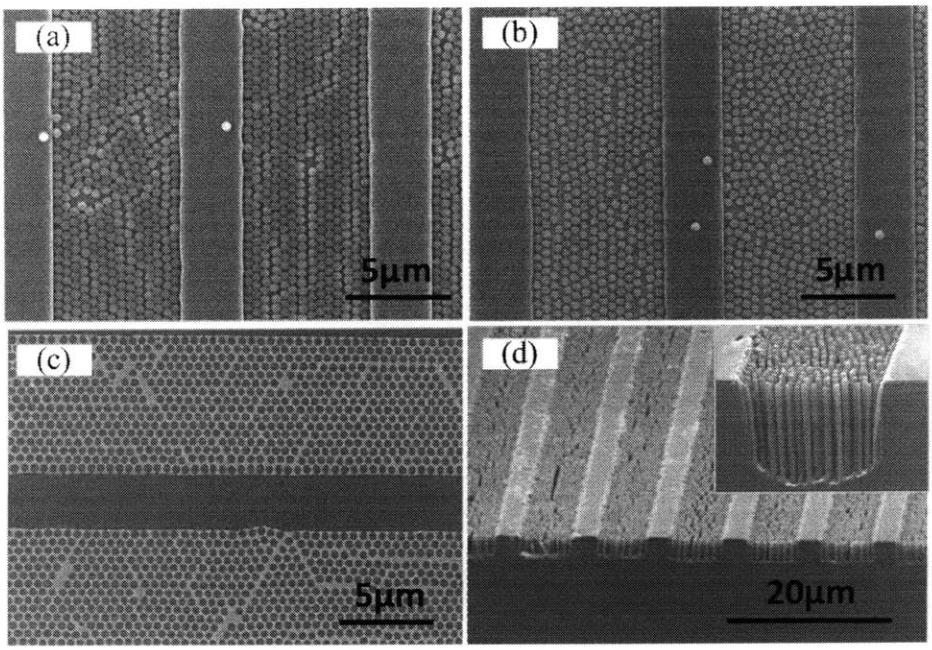

Figure 3.8 SEM images showing the silicon nanopillar-in-channel structure fabrication process flow: (a) PS sphere packed in PR gratings by vertical flow-directed self assembly; (b) PS spheres with reduced diameter in PR gratings after RIE in oxygen plasma; (c) A narrow Au strip with nano-hole array after sonicating in acetone to remove both the PS spheres and PR gratings; (d) Final silicon nanopillar-in-trench structure after etching in HF and H_2O_2.

2.6 Conclusion

In summary, the etching mechanism was investigated by studying the etch rate dependence and silicon morphology as a function of the geometrical characteristics of patterned catalyst films. Etch rate dependence results are consistent with the current electrochemical model, which suggests the existence of an oxidized divalent silicon layer *underneath* the metal catalysts. The intermittent contact between the silicon and metal during etching based on this model is used to explain the different silicon morphologies after catalytic etching when patterned continuous catalyst films with different lateral dimensions were used.

It was also shown that one critical condition for successful etching is for the HF to be able to access the silicon-metal interface. The results might be used to create large-area through-wafer holes in silicon.

Chapter 4 Experimental Methods: Metal Thin Film Patterning Techniques

Metal-assisted etching used in conjunction with various film-patterning techniques has been employed to fabricate high-aspect-ratio one-dimensional (1D) silicon nanostructures including both pore and wire arrays. In this chapter, the various lithographic techniques used to create patterned catalyst films are described. The main techniques utilized include *contact lithography*, *interference lithography*, *nanosphere lithography*, *block copolymer lithography*, and *templated self assembly*. Details of each technique including recipes, limitations, and potential issues associated with each method are presented in the following sections. The film patterning techniques introduced in this section were used extensively throughout this thesis research. The applications of metal catalyst films patterned using these methods for metal-assisted etching of silicon will be discussed in greater detail in the following chapters. Images of the as-fabricated structures can also be found in these chapters.

4.1 Contact lithography

Contact lithography is a photolithographic method whereby the pattern to be printed is recorded in a photosensitive resist layer by exposing it to a uniform light source through a photomask that is in direct contact with the substrate. This method is useful for producing micron-sized features. In this work, we used contact lithography to create photoresist (PR)

relief structures for lift-off to form large metal patterns and to fabricate templates for nanosphere lithography (discussed in section **4.5**). A general fabrication process is outlined below.

- *Resist coating*: Hexamethyldisilazane, or HMDS, is first spin-coated onto a silicon wafer to promote adhesion between the substrate and the photoresist layer. HMDS is applied by first drop-casting enough solution to cover the entire substrate surface, letting it sit for 60 s, and spinning at 3K rpm for 60 s to remove excess HMDS. A positive PR (Shipley Microposit® S1813) is then spin-coated onto the substrate at a speed of 3K rpm for 60 s. A soft bake for the photoresist layer at 115°C for 60 s is carried out on a hotplate

- *Exposure*: A Tamarack i-line system is used for exposure. The exposure time [s] is calculated by dividing the energy required [J/cm^2] by the intensity of the lamp used [W/cm^2]. To ensure good contact between the photoresist and the mask, exposure is usually carried out 1 s at a time with 15 s intervals of wait time in between each run to allow the nitrogen outgassed from the photoresist to get pumped out.

- *Development*: Shipley Microposit® MF-321 developer is used. The exposed sample is spray-developed for 60 s, rinsed thoroughly with flowing D.I. water, and blow-dried with nitrogen.

- *Ashing*: In some cases, unwanted photoresist residue may persist between resist lines after development. The residue can be removed fairly easily by ashing the sample in an asher in an He and O_2 plasma (0.4 T, 200W) for a few seconds.

- *Metal deposition and lift-off*: A more directional metal deposition method is usually preferred for lift-off processes since a conformal metal coating over the photoresist features prevents the selective removal of the photoresist. Electron beam (ebeam) evaporation is therefore used for all the patterning processes used in this thesis research unless otherwise noted. For lift-off, the sample is soaked in acetone for as long as it takes to remove all the photoresist. Sonication or stirring can also be used to aid this process.

4.2 Interference lithography

Interference lithography (IL) is a low-cost method for the exposure to form identical structures over large areas. Fabrication of both holes and posts in the resist layer using IL has been demonstrated. With this method, features with dimensions as small as mid-ultraviolet wavelengths can be obtained.

The basic principle of interference lithography involves the formation of a standing wave pattern when two or more beams of coherent light interfere (66). For example, through the interference of two beams, the standing wave forms a grating pattern. This is demonstrated schematically in **Figure 4.1**. The period of the grating pattern in the x-direction (P_x) is

determined by the light wavelength (λ) and the half angle at which the two beams meet (θ), and is given by the following equation.

$$P_x = \frac{\lambda}{2 \sin \theta}$$

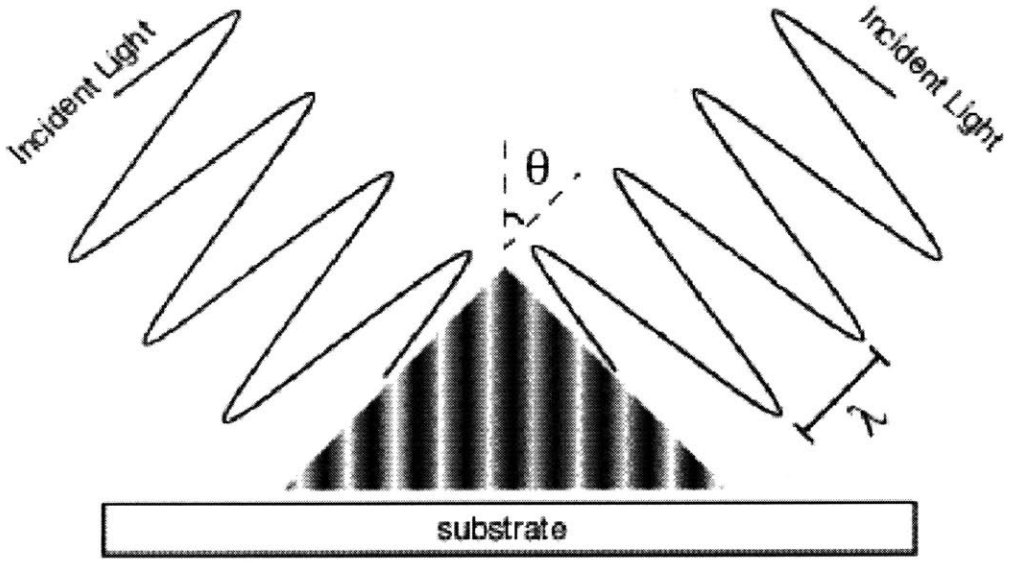

Figure 4.1 Two beams of coherent light interfere to form a pattern of parallel fringes.

The standing wave pattern can be recorded in a photoresist to create periodic structures in the photo-sensitive layer. Depending on whether the resist is positive or negative, the areas that receive an exposure dose greater than the threshold dose will become either soluble or insoluble in the photoresist developer, respectively. In addition to simple grating patterns, a variety of periodic patterns are also possible with multiple exposures. For example, a square array of holes or posts can be obtained by exposing the sample twice with a rotation angle of 90°.

A Lloyd's mirror interferometer, which involves the use of a broad beam of light and a mirror to reflect part of the light back onto itself, was used in our work. The basic configuration is shown in **Figure 4.2** (66). The system, equipped with a 325 nm wavelength helium-cadmium laser, is capable of producing features with a minimum period of ~165 nm. For the particular system we used, the mirror is fixed at a perpendicular angle to the image plane. The period of the grating is hence controlled by changing the rotation angle of the entire mirror/substrate assembly.

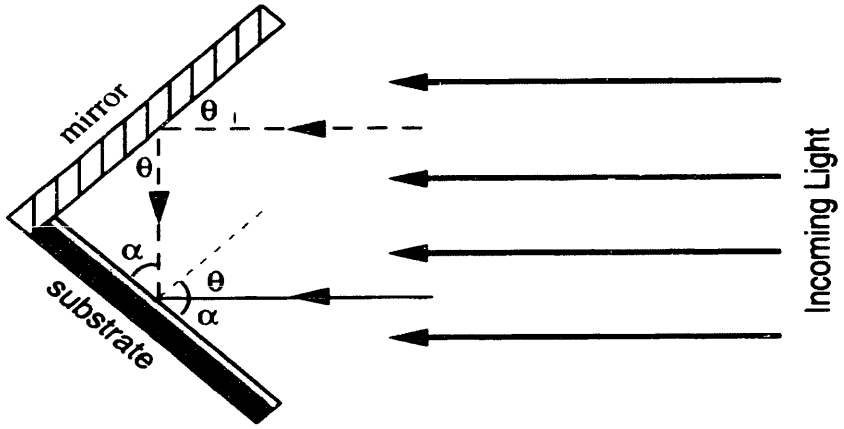

Figure 4.2 Basic Lloyd's Mirror configuration.

In addition to the standing wave pattern formed in the plane of the substrate, a second interference pattern is also formed perpendicular to the substrate due to back reflection at the substrate-photoresist interface. The secondary interference can cause a loss of line-width control and mechanical weakening of the resist structure. To minimize the back reflection at the substrate-resist interface, an anti-reflection coating layer (ARC) is coated underneath the

photoresist layer. The effectiveness of the ARC is determined both by its optical constants and the thickness of the layer. Simulation software developed by Walsh (66) is used to determine the optimal thickness of each layer. Typically a surface reflectivity of < 5% is desired for optimal results. The general process for the fabrication of both hole and post arrays is described below. Readers should be advised that the exposure dose and dry etching recipes should be used only as a guide as results can vary significantly for different systems.

- *Resist stack coating*: An interlayer between the ARC and the resist layer is used to facilitate pattern transfer and ensure a good sidewall profile for subsequent metal film deposition and lift-off (M. L. Schattenburg). The ARC, interlayer, and photoresist are collectively referred to as a *trilayer stack*. The materials used, spin speed, and bake time are summarized in **Table 4.1**.

Table 4.1

Layer		**Hole Arrays (negative PR)**	**Post Arrays (positive PR)**
ARC	**Material**	XHRiC – 11 (Brewer Science)	BARLi (AZ Electronic Materials)
	Spin speed	2.9K rpm for 60 s (110 nm)	4.6K rpm for 60 s (220 nm)
	Bake temp.	175°C for 90 s	175°C for 90 s
Interlayer		30 nm SiO_2 E-beam evaporated	20 nm SiO_2 E-beam evaporated
PR	**Material**	THMR-iN PS-4 (OHKA America)	PFI88 (Sumitomo Chemical Co.)
	Spin speed	2.4K rpm for 30 s (200 nm)	3.75K rpm for 60 s (200 nm)
	Prebake temp.	*no* soft bake required	90°C for 90 s

*Prior to the application of photoresist on SiO_2, HMDS must be first coated to augment adhesion of the photoresist layer on the oxide surface. The resist feature will otherwise delaminate during the development process. The application of HMDS is described in section **4.1**.

- *Exposure*: A double exposure process at a 90° sample rotation angle between the two exposure runs is used to create a square array pattern in the photoresist. The period of the pattern is determined by the rotation angle of the mirror/substrate stage. The duty cycle,

or the ratio of the width of the features to the period, is controlled by the exposure dose (power at stage [μW] multiplied by exposure time [s]). **Table 4.2** lists some sample exposure doses and resulting duty cycles (d_{hole}/period for hole arrays and d_{post}/period for post arrays).

Table 4.2

Negative PR (hole arrays)			**Postive PR (post arrays)**		
Period	**Dose**	**d_{hole}/P**	**Period**	**Dose**	**d_{post}/P**
200	25.2	0.5	200	122.4	0.27
400	24.5	0.52	400	145.8	0.26
600	21.9	0.57	800	98.8	0.28
1000	25.8	0.47	1200	120.8	0.31
1200	19.4	0.56	1500	142.7	0.27

- *Development*: A post exposure bake (PEB), which is performed after exposure but before development, is required for the PS-4 resist in order to complete the photo-reaction initiated during exposure. PEB for PS-4 is done on a hotplate at 110°C for 90 s. This PEB step is not necessary for PFI88. Development for both types of resists is carried out using tank development in CD26 (Shipley Micropost®), a tetramethylammonium hydroxide (TMAH) based developer, for 60 s.

- *Pattern transfer*: Reactive ion etching (RIE) is used to transfer the photoresist pattern into the underlying oxide and ARC layers. The RIE parameters are listed in **Table 4.3** for both the positive and negative resist stack.

Table 4.3

		Hole Arrays (negative PR)	**Post Arrays (positive PR)**
SiO_2	**Recipe**	*CF4_150W*	*CF4_150W*
	Conditions	10 mT CF_4, 150 W	10 mT CF_4, 150 W
	Time	1:15	1:15
ARC	**Recipe**	*ARC_POW*	*ARC3*
	Conditions	10 mT $He+O_2$ 130 W	10 mT $He+O_2$, 300 W
	Time	1:40	1:20

It is worth noting that the ARC layer in both cases is slightly over-etched in order to create a more vertical sidewall. This is made possible by having an oxide interlayer. The more vertical sidewall facilitates the lift-off process, which is demonstrated in **Error! Reference ource not found.**. As shown in **Figure 4.3(a)**, without the oxide interlayer and over-etching, the lack of etch selectivity between the photoresist and ARC (essentially 1:1 in an oxygen plasma) leads to a sloping ARC sidewall which in turn leads to metal deposition on the sidewall even when a highly directional metal deposition method such as evaporation is used. This conformal coverage protects the resist stack from being selectively removed during the lift-off

process. The cartoon inset in figures (b) and (c) show the discontinuity in the metal thin film near the resist features which makes lift-off a relatively easy process compared to the case shown in (a).

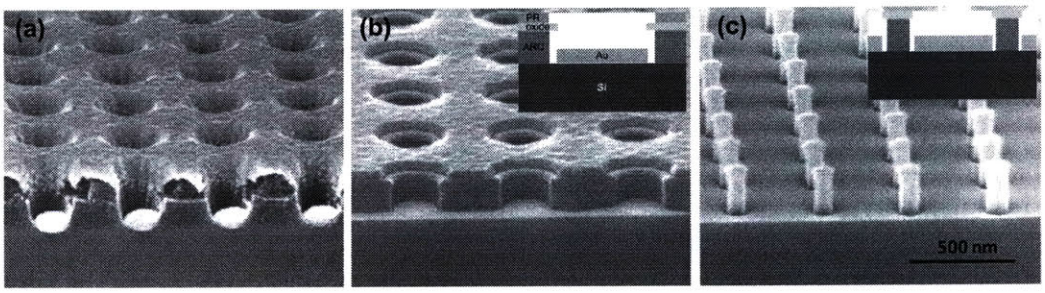

Figure 4.3 Scanning electron microscope (SEM) images showing reactive ion etching (RIE) results for (a) hole-array samples without an oxide interlayer; (b) hole-array samples with an oxide interlayer; and (c) post-array samples with an oxide interlayer. The cartoon insets in (b) and (c) demonstrates the non-conformal metal film coverage made possible by the trilayer resist stack.

- *Metal film deposition and lift-off*: Metal thin film is deposited through the resist mask using ebeam evaporation. To remove the BARLi ARC, the sample is soaked and then sonicated in hot N-Methyl-2-pyrrolidone (NMP) at ~70 - 80°C for 5 minutes and 2 minutes, respectively. The process can be repeated until the BARLi ARC posts have been completely removed. For the hole-array samples, lift-off is carried out by soaking the sample in 10% HF for 2 minutes to remove the oxide interlayer. The remaining XHRiC11 ARC is then stripped using oxygen RIE (*recipe: ARC3* for 1:20). Completion of lift-off can usually be determined by visual inspection by observing the diffraction pattern on the sample surface for periods > 350 nm.

4.3 Nanosphere lithography

Nanosphere lithography (NSL) is an economical method for fabrication of hexagonally-closed-packed arrays of nanoscale features on a substrate. The process generally begins with the formation of a two-dimensional, self-assembled monolayer of monodispersed nanospheres such as polystyrene or silica, which serve as a lithographic mask. The monolayer can be prepared using various techniques including spin-coating (67) and a Langmuir-Blodgett method (68). Both techniques, while very useful in producing relatively low defect density, large area (a few cm^2) monolayers, require the addition of a surfactant to change the surface tension properties of the liquid. Au and Ag catalyst films patterned using nanosphere masks prepared using the two techniques failed to catalyze silicon etching even after immersion in the etchant solution for prolonged periods. Although the exact reason is still unclear at this point, one possible explanation could be failure to remove the surfactant on the silicon surface during rinsing, preventing good contact between the metal catalysts and the silicon substrate surface.

A method based on the controlled evaporation of a solvent from a nanosphere colloidal solution was used instead to prepare the monolayer (69). Although it has been shown that the addition of a surfactant at low particle concentrations can improve the ordering of the nanospheres (70), deposition results without the use of surfactants was found to be acceptable

for our purposes. The general procedure for the preparation of a catalyst mesh using nanosphere lithography is outlined below.

- *Substrate preparation*: A hydrophilic surface is necessary for successful nanosphere monolayer coating using liquid-evaporation-based methods. Silicon substrates are first treated in a piranha solution (H_2SO_4: H_2 O_2 = 3:1) for 15 minutes to grow a thin layer of chemical oxide to ensure that the substrate is wettable by water.

- *Nanosphere monolayer preparation*: A home-built dip-coater equipped with a piezoelectric motor is used to prepare the polystyrene sphere monolayer. Specifications for the dip-coater are included in the **Appendix**. The as-received colloidal solutions (microParticles GmbH) are first diluted to desired concentrations (0.8 wt % for spheres with a diameter of 100 nm, and 1.2 wt% for spheres with diameters of 300 and 500 nm) with DI water. The piranha-treated silicon substrate is then vertically inserted into the colloidal solution and pulled up using the dip-coater at a speed of 20 μm/sec to allow the solvent to slowly evaporate off the substrate surface

- *Reactive ion etching*: The nanosphere mask can be used directly as a metal-deposition mask for the fabrication of hexagonal arrays of metal dots, as shown in **Figure 4.4**. To pattern a metal mesh an additional etching step to reduce the sphere diameter is needed. For polystyrene spheres, oxygen RIE serves this purpose. The dry etching rate is roughly

etching rate is roughly linear with respect to time for a given RIE condition. For example, for an oxygen plasma at 10 mTorr and 40 W, the etch rate is approximately 30 nm/min, as shown **Figure 4.5(a)**. It is important to note that the diameter of the spheres shrinks faster in the normal direction (to the surface) due to the directional nature of RIE, which can be seen in the SEM micrograph in **Figure 4.5(b)** in which a polystyrene sphere array is shown after the sample has been subjected to dry etching for 6 min. As a result, there exists a minimum lateral diameter below which metal lift-off no longer works as the deposited metal film becomes conformal over the spheres.

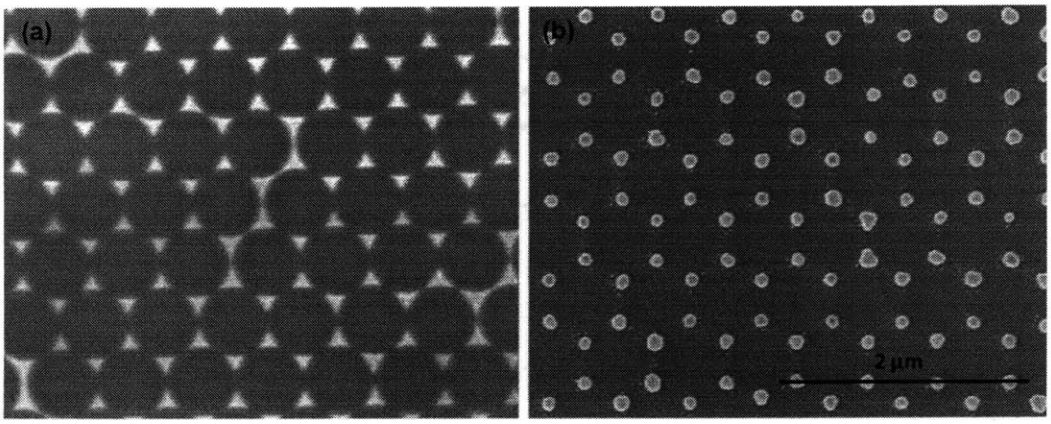

Figure 4.4 A hexagonal array of gold nanoparticles patterned using nanosphere lithography: (a) Au deposited through the interstices of the nanosphere mask, and (b) Au nanoparticles after annealing at 800°C for 1 hr.

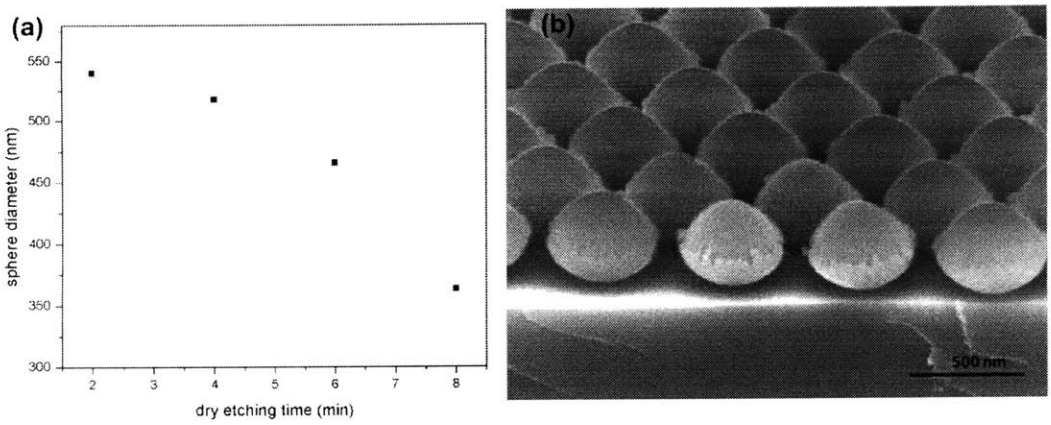

Figure 4.5 (a) Polystyrene sphere diameter (with original diameter of 550 nm) plotted as a function of oxygen dry etching time. RIE conditions were: oxygen pressure = 10 mTorr, and power = 40 W; (b) SEM image of an array of polystyrene spheres after etching for 6 minutes.

- *Metal film deposition and lift-off*: Ebeam evaporation is used for metal thin film deposition. The typical film thickness was 15 nm for most of our samples. The film thickness is limited as a thick film will cause difficulties in the subsequent lift-off process. As an example, for nanospheres with an original diameter of 300 nm and a diameter of roughly 100 nm after oxygen RIE, a film thickness of greater than 25 nm can lead to problems in lift-off. One such example is shown in **Figure 4.6**. After the metal film has been deposited, lift-off of the polystyrene spheres is carried out by sonicating the samples in toluene for 3 -5 min.

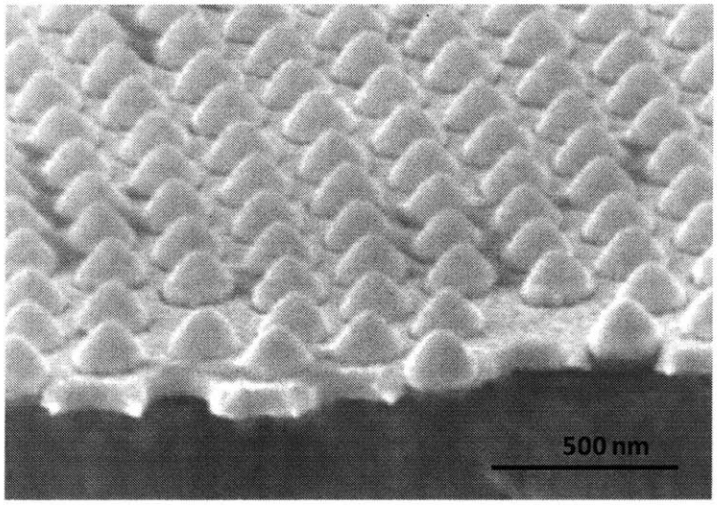

Figure 4.6 SEM image showing a polystyrene nanosphere mask after the deposition of 45 nm of Au film. The conformal coverage of the film prevents the selective removal of the polystyrene spheres.

4.4 Block copolymer lithography

Diblock copolymers are two chemically distinct types of polymer chains connected covalently at one end. Because of the covalent bond, the two immiscible polymers that constitute the material cannot phase separate on a macroscopic length scale. Instead, given that kinetics permits, the polymers microphase separate into organized patterns with lamellar, cylindrical, or spherical morphologies at a characteristic length scale determined by the volume ratio and chain length (71).

Typically in block copolymer (BCP) thin film processing, the BCP is first dissolved in a good solvent for both types of polymer and spin- or dip-coated onto a substrate. Microphase segregation is induced by annealing the BCP thin film at elevated temperatures or in a solvent

vapor to speed up the kinetics. Block copolymer lithography refers to the process by which the microdomain structures in a BCP thin film are used to fabricate positive or negative patterns in the underlying functional films by either subtractive or additive processes.

For patterning of the catalyst Au films, a subtractive process in which a continuous film is first deposited underneath the BCP mask and subsequently dry-etched to create the patterns in the film is not very feasible as there is not a well-characterized dry etching chemistry for gold. Instead, an additive process involving lift-off was used for this purpose. However, for small features such as BCP microdomains, lift-off can be a tricky process due to difficulties in depositing a fully continuous metal thin film that is not conformal over the nano-sized features. To solve this problem, we used an additional oxide layer into which the BCP pattern was transferred to serve as the metal deposition mask. A spherical domain polystyrene-*block*-polyferrocenyldimethylsilane block copolymer, denoted as PS-*b*-PFS, was used as the pattern transfer mask due to its high etch resistance owing to the organometallic nature of the PFS block. Details of the processing steps are described below.

- *Substrate preparation*: Prime silicon wafers are used as received without further cleaning. A 60 nm-thick silicon oxide layer is deposited using ebeam evaporation on the substrate, to serve as the pattern transfer layer.

- *BCP self assembly*: PS-*b*-PFS diblock copolymer is dissolved in toluene to form a 1.5 wt% solution. Freshly-prepared solution is usually allowed to sit for two days before use, to ensure good mixing. The remaining solution can be stored in a fridge for future use. Depending on the molecular weight of the polymer, the film thicknesses for monolayer formation can vary. For example, for PS-*b*-PFS 47/15 (47K g/mol for PS and 15K g/mol for PFS), the film thickness is 51 – 55 nm, whereas for PS-*b*-PFS 43/12 (43K g/mol for PS and 12K g/mol for PFS), the film thickness is 42 – 45 nm. Film thickness is adjusted by the spinning speed and solution concentration, and can be measured using an ellipsometer (starting index of refraction = 1.46). The sample is subsequently annealed in vacuum at 140°C for over 24 hours to induce microphase segregation.

- *Pattern transfer*: The PS matrix surrounding the spherical PFS microdomains is first removed in an oxygen plasma. Pattern transfer into the underlying oxide layer is achieved using RIE in CF_4. The RIE conditions are summarized in the following table.

Table 4.4

	PS matrix removal	**Oxide pattern transfer**
Recipe	*O2_90W*	*CF4_150W*
Conditions	6 mT O_2, 90 W	10 mT CF_4, 150 W
Time	0:52 for PS-*b*-PFS 47/15 0:45 for PS-*b*-PFS 43/12	1:00 for 60 nm SiO_2

- *Metal deposition and lift-off*: A metal thin film is deposited through the oxide-post mask using ebeam evaporation. Lift-off to selectively remove the oxide posts is carried out by immersing the sample in 10% HF for 1-2 min. It is worth noting that an inorganic shell can form over the PFS spheres during the RIE process. As a result, some of the inorganic material covered with deposited metal can remain on the metal film surface after the HF lift-off process. The residue persists even after sonication or an oxygen RIE treatment. However, since the residue does not appear to affect the final etching, no additional effort was made to remove it.

4.5 Templated self-assembly

Templated self-assembly (TSA) permits the manufacturing of nanoscale features with programmable structures and arrangements on a size scale that is otherwise difficult to achieve. General approaches to TSA include chemical modification of substrate surfaces (72), patterned charge (73), and physical templating (74). By combining top-down and bottom-up methods, control over important design parameters for device applications such as placement accuracy, spatial arrangement, size and shape can be achieved. In our work, lithographically-patterned relief structures were used as the template.

We utilize both colloidal and block copolymer TSA to pattern catalyst thin films on different size scales for metal-catalyzed etching. For the TSA of colloidal particles, a

sedimentation and/or capillarity-based method is used to order the particles (75). A variety of lattices can be assembled using this method by varying the ratio between the size of the particles to the template dimensions (74). The colloidal TSA process involves two main steps: (i) the fabrication of topographical features on the substrate, and (ii) flow-directed self assembly of nanospheres. For the self-assembly process, the topographical features act as pinning sites for the moving contact line during evaporation. In a similar manner to the formation of "coffee stain," as the contact line gets pinned, there is a net liquid flow towards the contact line, carrying the nanoparticles with it (76). Once the particle concentration becomes high enough at these sites, the long range capillary force can help self-assemble them into close-packed structures (77). A more detailed description of the fabrication process for patterned metal meshes is provided below.

- *Template fabrication:* Contact lithography is used to create the micron-sized physical templates for colloidal self-assembly. To avoid multilayer formation, the template is ashed in a He and O_2 plasma for several minutes to reduce the height of the photoresist features to roughly the dimension of the polystyrene spheres used. The etch rate of S1813 at 0.4 T and 200 W is approximately 110 nm/min, as shown in **Figure 4.7**.

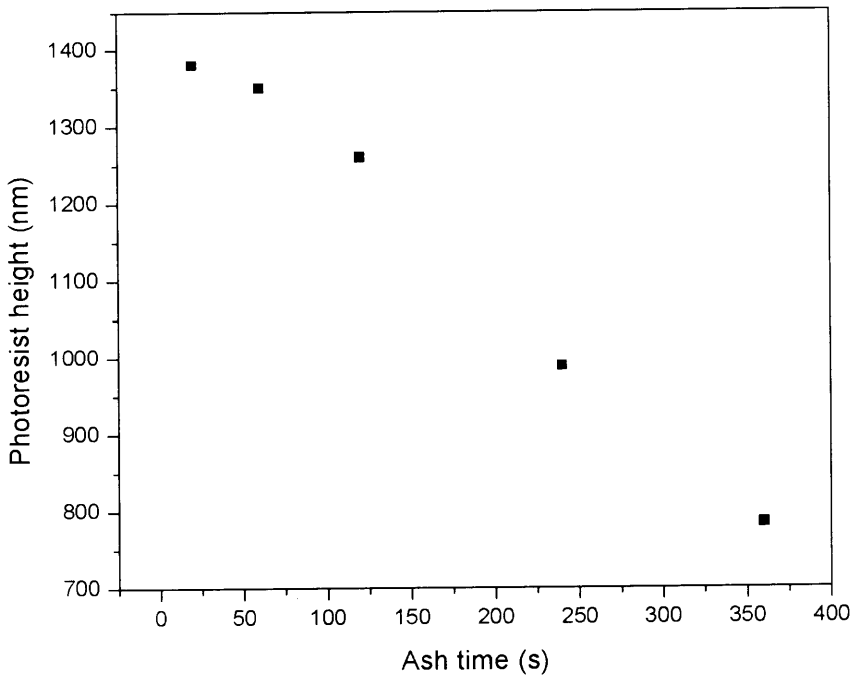

Figure 4.7 Photoresist (S1813) height change as a function of ashing time (ashing conditions: 0.4 T He and O_2 at 200 W).

- *Templated self-assembly:* The TSA of polystyrene spheres is achieved by a flow-directed self assembly method in which the patterned substrate is inserted vertically in a colloidal suspension of polystyrene spheres (diluted to ~0.05 wt %). The solvent (water) is then allowed to slowly evaporate at room temperature.

- *Metal deposition and lift-off*: Ebeam-evaporated metal is deposited with both the photoresist features and the polystyrene spheres serving as a deposition mask. Patterned metal meshes are obtained by sonicating the sample in acetone to selectively remove both the photoresist and the polystyrene nanospheres.

For the TSA of block copolymer, relief structures fabricated using interference lithography are used as the physical template. The general approach of utilizing topographical features to achieve long range order is called graphoepitaxy (78). Similar to the case of colloidal self assembly, the template height should be roughly the same as the thickness of one BCP monolayer to avoid multilayer formation. For PS-*b*-PFS 47/15, this thickness is approximately 50 – 55 nm; i.e. the actual template (consisting of an oxide and an ARC layer) should have a thickness of 50 - 55 nm. However, as discussed in section **3.2**, the efficacy of the ARC layer in minimizing back reflection from the substrate-resist interface is also determined by its thickness. Surface reflectivity calculations showed that, for any practical photoresist thicknesses, an ARC thickness of 50 – 55 nm is ineffective for reducing back reflection. As a result, a different resist stack is used to fabricate the template. Details of the process are described below.

- *Resist stack coating*: The resist stack, shown in **Figure 4.8**, consists of 5 different layers on top of 60 nm of ebeam SiO_2 used for BCP pattern transfer. The bottom two layers (50 nm BARLi ARC/7 nm SiO_2) are used as the final template for BCP-TSA, whereas the top three layers (220 nm BARLi ARC/20 nm SiO_2/200 nm PFI88) constitute the trilayer stack used for interference lithography. To coat 50 nm of BARLi ARC, the solution is first

diluted. The thin oxide layer (7 nm) is deposited using sputter deposition. The spinning speeds for the trilayer are listed in **Table 4.1**.

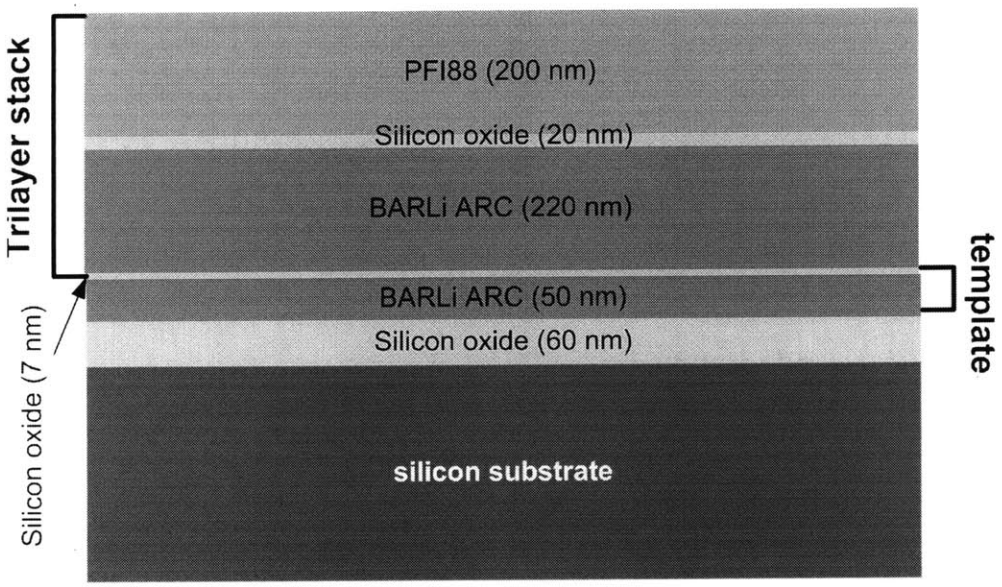

Figure 4.8 Resist stack for the fabrication of templates for block copolymer templated self-assembly.

- *Exposure*: During the TSA process, the polymer flows from the grating mesas into the trenches. To facilitate this process, gratings with a greater ratio of trench width to period are preferred.

- *First pattern transfer*: We refer to the template fabrication as the first pattern transfer step. RIE is used for this step. RIE conditions for each layer are summarized in **Table 4.5**. The resulting structure is gratings consisting of only the bottom two ARC and oxide layers.

Table 4.5

Etch step	**7 nm SiO_2**	**220 nm ARC**	**7 nm SiO_2**	**50 nm ARC**
Recipe	*CF4_100W*	*ARC3*	*CF4_150W*	*ARC3*
Conditions	10 mT CF_4, 100W	10 mT He/O_2, 300W	10 mT CF_4, 150W	10 mT He/O_2, 300W
Time	2:00	1:20	1:00	0:45

- *BCP-TSA*: The ARC-oxide gratings are spin-coated with a 1.5 wt% PS-*b*-PFS solution in toluene. The film thicknesses should be adjusted such that upon thermal annealing, the polymer that was originally on the grating mesas can flow into the trenches to completely fill them; i.e. for gratings with a smaller trench-to-mesa ratio, a more diluted solution or a faster spinning speed should be used. An example of the polymer solution properly filling the trenches is shown in **Figure 4.9(a)**. If the polymer thin film is too thin, such as shown in **Figure 4.9(b)**, poor self assembly can result as there is little film coverage at the center of the trench structures.

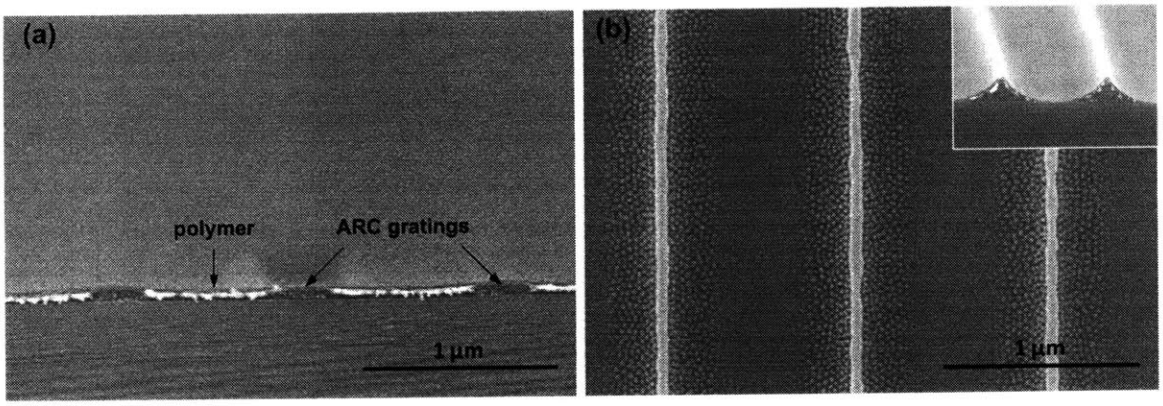

Figure 4.9 SEM images of (a) block copolymer filling the trenches after spin-coating onto the gratings (after thermal annealing but before removal of the polystyrene matrix); and (b) poor self assembly of the BCP microdomains after thermal annealing as a result of unsuitable film thickness (too thin). The PS matrix has been removed to reveal the PFS spherical domains in this image. The inset shows improper filling of the polymer solution before the removal of the PS matrix.

- *Second pattern transfer*: Two types of pattern can be fabricated at the second pattern transfer step, or pattern transfer into the bottom oxide layer. A schematic of the process is shown in **Figure 4.10**. Figure (a) represents the spherical PFS domains assembled in gratings after the PS matrix has been selectively removed in an oxygen RIE. The a-b-c series represents the process sequence used to transfer both the grating pattern and the spherical PFS pattern into the underlying oxide layer. The oxide posts and oxide gratings are then used as the metal deposition mask for patterning metal thin film strips with perforating hole arrays. The a-d-e-f process sequence is used to transfer *only* the templated spherical PFS pattern into the oxide layer for the fabrication of patterned hole arrays in a continuous metal thin film extending over the entire substrate. For the a-b-c process sequence, only a single RIE step is required for pattern transfer. For the a-d-e-f

sequence, however, a slightly more complicated process is necessary. The pattern transfer step is done by first removing the oxide on top of the ARC gratings, and then removing the ARC gratings using organic solvents. The first step is necessary in order for the solvent to access the ARC layer. Since the PFS spheres are covered with an inorganic shell formed during the RIE processes, they are protected from dissolution in the solvent (79). Detailed process conditions are summarized in **Table 4.6**.

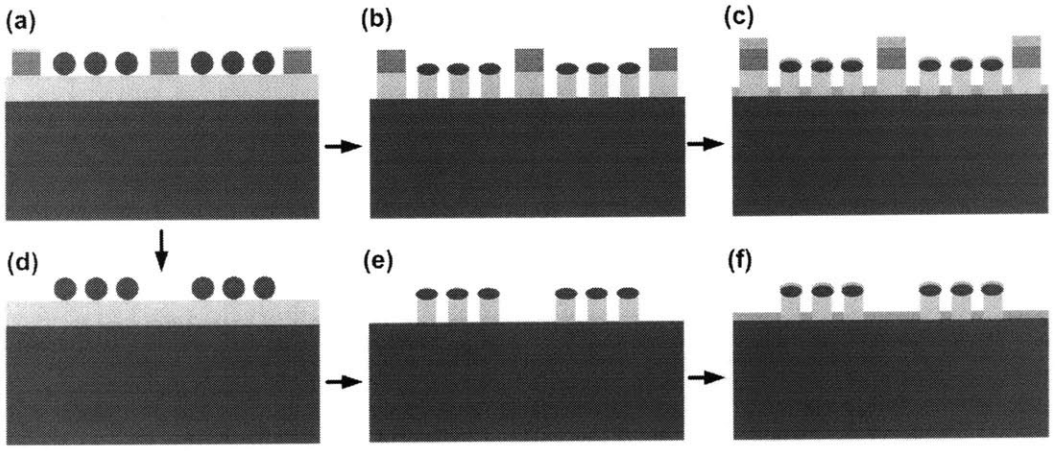

Figure 4.10 Schematic representation of the second pattern transfer process for the templated self assembly of a block copolymer. The a-b-c series represents the process flow for the fabrication of *patterned strips of metal meshes.* The a-d-e-f series represents the process flow for the fabrication of *patterned hole arrays in a continuous metal thin film.*

Table 4.6

Step			**Process conditions**
PS removal	**Recipe**		*O2_90W*
	Conditions		6 mT O_2, 90 W
	Time		0:54 for PS-*b*-PFS 47/15 0:45 for PS-*b*-PFS 43/12
a → b	**Recipe**		*CF4_150W*
	Conditions		10 mT CF_4, 150 W
	Time		65 s
a → d	**Silica removal**	**Recipe**	*CF4_100W*
		Conditions	10 mT CF_4, 100 W
		Time	20 s
	ARC grating removal		Spin-clean with NMP, acetone, methanol, and isopropanol successfully for 15 s each.
d → e	**Recipe**		*CF4_150W*
	Conditions		10 mT CF_4, 150 W
	Time		60 s

- *Metal deposition and lift-off*: Metal deposition is carried out using ebeam evaporation. For both the a-b-c and a-d-e-f processes, lift-off is carried out by soaking the sample in 10% HF for 1 – 2 min.

4.6 Conclusion

In summary, the various techniques utilized to create patterned catalyst films in this thesis work are described in this chapter. Each technique is suitable for a specific pattern size range. Contact lithography is generally used for creation of patterned catalyst films several micrometers in lateral dimension or for creation of relief structures used for nanosphere lithography (NSL), which is used to create hexagonally-packed arrays of perforating holes in a catalyst film. Interference lithography, on the other hand, is more suitable for patterning catalyst films several hundreds of nanometers in lateral dimensions or for patterning relief structures used for block copolymer lithography (BCP), which is used for features on a much smaller size scale (tens of nanometers). By using the various lithographic techniques described in this chapter in conjunction with metal-catalyzed etching, silicon nanostructures of different size and geometry with good fidelity to the original pattern can be fabricated.

Chapter 5. Silicon Nanowires Fabricated Using Block Copolymer Lithography and Metal-Assisted Etching

5.1 Introduction

Semiconductor nanowires have attracted considerable attention due to potential applications arising from their quasi-one-dimensional nature (80), including their high surface to volume ratio. In particular, silicon nanowires (SiNWs) are candidates for applications in nanoscale optoelectronics, sensors, and other devices (81) (82). Much effort has been devoted to the fabrication of vertically-aligned epitaxial Si nanowires with highly controlled diameter, length, and placement.

The most commonly used method for the fabrication of SiNWs is the vapor-liquid-solid (VLS) technique in which metal nanoparticles are used as catalysts for growth by chemical vapor deposition (83) (84). Catalysts for NW growth include gold nanodot arrays patterned by nanosphere lithography (85), and gold colloidal particles (86). One major concern for VLS-grown wires is the diffusion of catalyst metal, typically gold, into the wires at the high temperatures usually required for wire growth. This poses a serious problem for the realization of SiNW electronic and optical devices because gold contamination in silicon creates carrier traps and reduces minority carrier lifetimes. Another challenge for VLS SiNW growth is orientation control. In particular, VLS SiNWs preferentially grow in the <111> direction but

the orientation varies with wire dimension (87). Vertical epitaxial growth on Si(100) wafers is therefore rarely observed and mixed growth in the four crystallographically equivalent <111> directions is observed instead. This limits integration of VLS nanowires with current CMOS technology.

Other methods for nanowire creation through etching processes have also been investigated. Examples include the fabrication of high aspect ratio silicon nanopillars using deep reactive ion etching (DRIE) using a polystyrene colloidal mask (88), and the fabrication of densely packed silicon nanopillar arrays using a Cr mask made by block copolymer lithography (89). Oxidation-etch cycles have also been used to create lithographically defined Si nanowires with both in-plane and vertical orientations (90) (91). Although these techniques are effective, the spacings of nanowires created through oxidation-etch processes are limited to those of the pre-oxidation Si structures, and fabrication of high-aspect ratio 1-D silicon nanostructures using DRIE is limited by mask degradation.

Metal-assisted etching in combination with various film patterning techniques has recently been demonstrated as a promising alternative for SiNW fabrication. Metal-assisted etching has the advantage of being a room temperature process, and can produce features oriented in the <100> direction (53). In this approach, metal particles or films are used to locally catalyze Si etching in a mixture of hydrofluoric acid (HF) and an oxidant. Although the

exact dissolution chemistry of silicon in HF is not well understood, it is generally accepted that the silicon surface is passivated against dissolution unless an electronic hole is available (14). According to the local reduction-oxidation reaction scheme proposed by Li *et al.*, hole injection is provided by the reaction of the oxidant solution at the catalyst metal (57). Since injected holes diffuse rapidly away from the catalyst, etching is confined to areas near the metal. This localized behavior makes metal-assisted etching a simple and effective method for preparing arrays of high-aspect ratio silicon nanostructures.

Several SiNW fabrication methods employing metal-assisted etching have been recently reported. For example, large-area silicon nanowire and nanoribbon arrays were obtained by etching Si in HF and $Fe(NO_3)_3$, using a catalyst consisting of interconnected networks of silver nanoparticles deposited by galvanic displacement from a solution of HF and $AgNO_3$ (51). While effective in producing spatially aligned silicon nanostructures over a large area, precise control over wire shape and spacing is difficult to achieve as a consequence of the random nature of electroless deposition. In addition, SiNW size uniformity is limited by the distribution of Ag catalyst sizes, and wire diameters ranged from 20 to 300 nm (92). Nanosphere lithography based on polystyrene or silica colloidal spheres was used to create antidot arrays in a silver film deposited on Si, from which hexagonal arrays of SiNWs were made (53). Although good diameter control can be achieved, the minimum SiNW diameter is

limited by the colloid size, and full areal coverage of colloidal particles over large areas was difficult to achieve. Recently, Huang et al. used a method based on an anodic aluminum oxide (AAO) mask to pattern SiNW arrays with diameter as small as 9 nm (54). In this case, the AAO is used as a dry etching mask to pattern pits on a silicon substrate. A metal catalyst film is then deposited on the silicon after removal of the AAO. Diameter control was achieved by utilizing the shrinkage of the pores in the metal film as film thickness increases. As a result, the diameter distribution depends strongly on metal deposition conditions. The resulting nanowires had aspect ratios only up to 10, and broadly distributed diameters.

In the next section, we describe a new technique that employs a catalyst film patterned using block copolymer (BCP) lithography to fabricate ~20nm diameter SiNWs with high monodispersity over large areas. Block copolymers microphase separate to form self-organized patterns with lamellar, cylindrical or spherical morphologies and a characteristic length scale that depends on the volume ratio and chain length (71). Block copolymer lithography has been used to pattern catalysts for the fabrication of vertical arrays of carbon nanotubes (93) and metal nanowires (94). The self-organized patterns generally have local close-packed order, but when phase separation is templated with lithographically defined features, they can also have long-range close-packed order (95). Although the block copolymer we used showed less uniform ordering, improved long range order can be attained

through graphoepitaxy of other copolymers. We chose a polystyrene (PS)-*block*-polyferrocenyldimethylsilane (PFS) block copolymer that forms spherical PFS microdomains surrounded by a PS matrix on annealing (96). The organometallic PFS block has a high etch resistance, allowing for good pattern transfer into an underlying film (97). Using topographical templating, we demonstrate patterning of SiNWs at lithographically defined locations over cm-sized substrates.

5.2 Silicon nanowire fabrication: continuous carpets and carpeted channels

The experimental procedure for the fabrication of a continuous carpet of vertically-aligned silicon nanowires is illustrated schematically in **Figure 5.1**, and the resulting structures are shown in **Figure 5.2**. A detailed description of the film-patterning process is discussed in **Chapter 4**, and will only be briefly summarized here. Two diblock copolymers with differing molecular weights were used: 47kg/mol for PS and 15kg/mol for PFS (denoted as PS-*b*-PFS 47/15), and 42kg/mol for PS and 12kg/mol for PFS (denoted as PS-*b*-PFS 43/12). The PS-*b*-PFS was spin-coated from a toluene solution onto a SiO_2 layer deposited on a (100)-oriented silicon substrate. The film thickness, determined by the spin speed and solution concentration, is chosen for which only one BCP monolayer is formed. To achieve microphase separation into arrays of PFS spheres, the spin-coated sample were vacuum-annealed at 140°C

for 44 hours. After the removal of the PS matrix, the PFS pattern was transferred into the underlying oxide layer by reactive ion etching (RIE), forming an array of SiO_2 nanopillars on the Si(100) substrate. 12 nm of gold was deposited by electron-beam (ebeam) evaporation onto the oxide pillar arrays, and the pillars were removed by immersion in dilute HF for a short time, leaving an Au antidot array. Finally, ordered arrays of SiNWs with good fidelity to the original block copolymer pattern were obtained by etching the silicon under the gold in a mixed solution of HF, H_2O_2, and water (10 wt. % HF and 1.5 wt. % H_2O_2) for 5-15 minutes in ambient light. Post-etching drying was carried out in a critical point drier (Tousimmis AutoSamDri 815) after rinsing consecutively in 50%, 75%, and 90% alcohol for 3 min each, followed by 3 rinses in 100% alcohol.

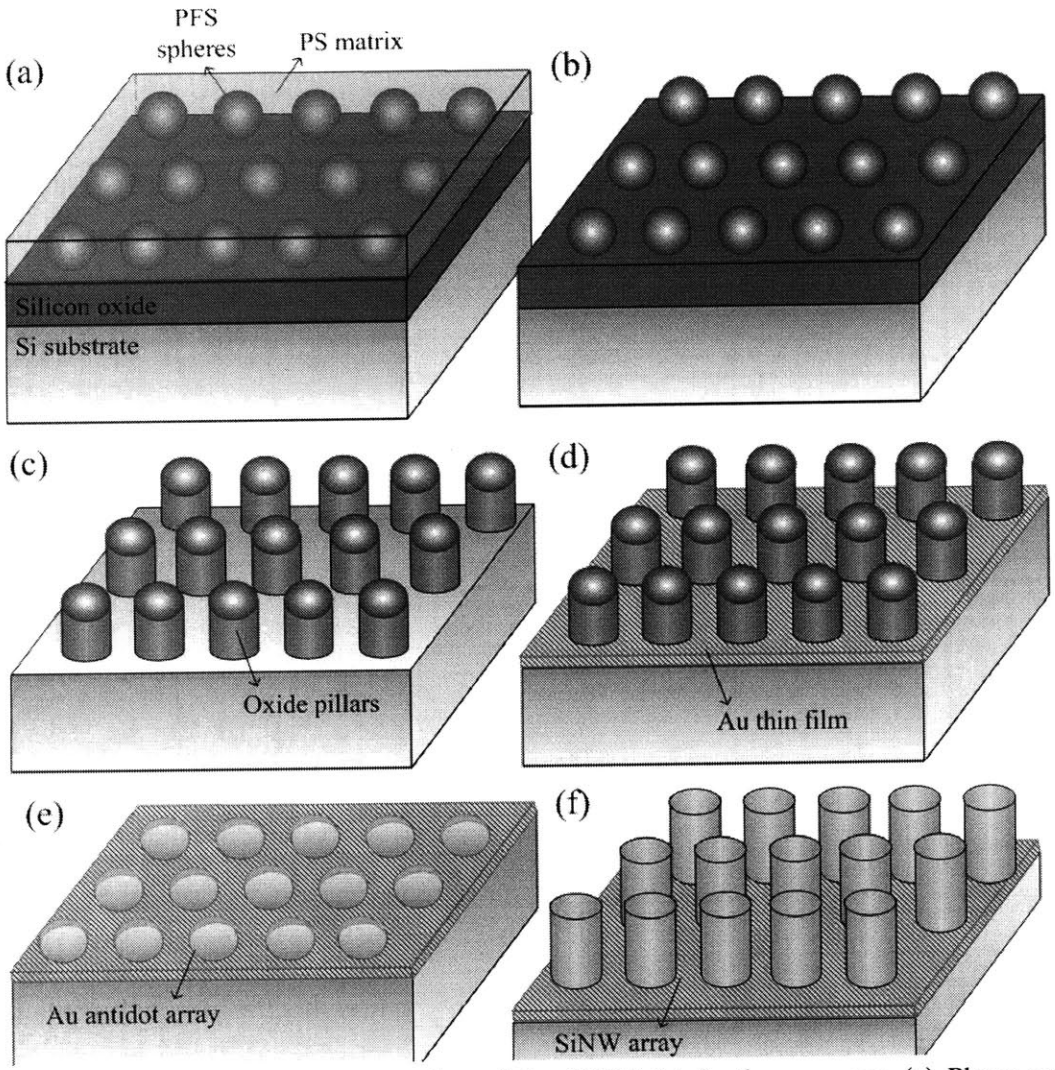

Figure 5.1 Schematic representation of the SiNW fabrication process: (a) Phase-separated polystyrene (PS)-*block*- polyferrocenyldimethylsilane (PFS) domains after spinning a block copolymer film onto a silicon substrate coated with silicon oxide and vacuum annealing; (b) Partly oxidized PFS spherical domains after the PS matrix is removed using oxygen reactive ion etching; (c) Pattern transferred into the oxide layer to form silicon oxide pillar arrays; (d) Au deposition over the oxide pillars; (e) Au antidot array after HF lift-off; (f) Silicon nanowire array after etching in a solution of hydrofluoric acid and hydrogen peroxide.

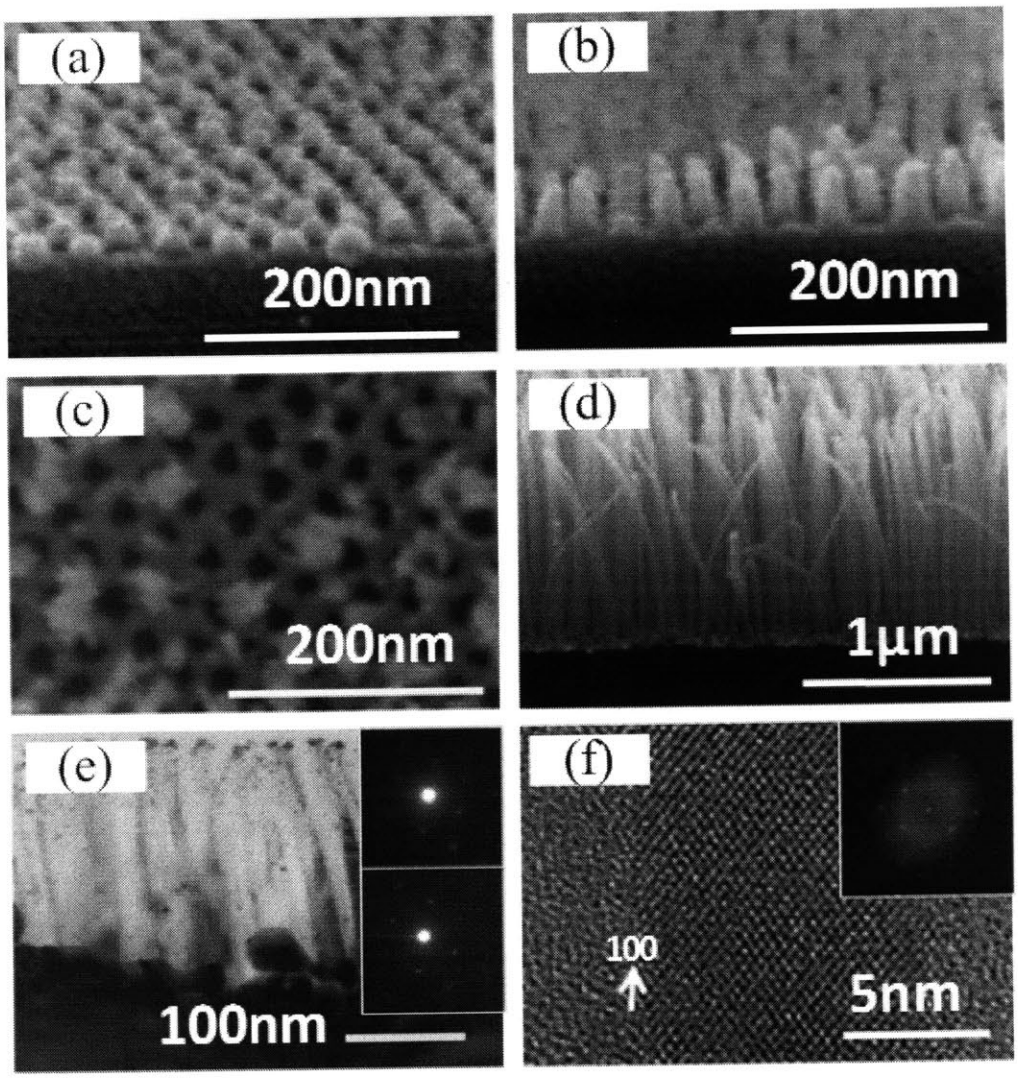

Figure 5.2 Scanning electron microscope images showing steps in the SiNW fabrication process flow: (a) PS-*b*-PFS 47/15 on a silicon substrate coated with silicon oxide after PS matrix has been removed by oxygen RIE; (b) Oxide pillars after CF_4 RIE; (c) 12 nm thick Au anti-dot array after liftoff of the pillars. Some silica material remains (bright contrast); (d) Silicon nanowire array after metal-assisted etching; (e) TEM image of a wire array (made from PS-*b*-PFS 43/12). Inset shows the selected-area electron diffraction (SAED) pattern on the [011] zone axis of different regions. The upper inset corresponds to a region encompassing mostly the substrate, and the lower inset corresponds to a region encompassing mostly the wire array; (f) TEM image of a single wire. Inset is the fast Fourier transform (FFT) pattern corresponding to a region in the nanowire showing the [011] zone axis.

For the growth of *templated* SiNWs, we used a Lloyd's mirror interference lithography system to fabricate gratings in a layer of a polymeric anti-reflection coating (ARC) which served to order the PFS sphere array. The process flow for a SiNW-in-channel structure is illustrated in **Figure 5.3(a)**. Scanning electron microscope (SEM) images of the resulting structures are shown in **Figure 5.4**. PS-*b*-PFS 47/15 was spin-coated into the ARC gratings and annealed under vacuum at 140°C for 44 hours. During annealing, the polymer flows from the grating mesas into the trenches, leaving the mesas polymer-free. The spherical PFS microdomain pattern and the grating pattern were transferred into the oxide layer by RIE to form arrays of oxide pillars inside oxide gratings. Both the oxide pillars and gratings served as an ebeam deposition mask. Lift-off of the Au catalyst film was performed in HF to obtain narrow stripes of Au containing ordered arrays of nano-sized holes. Finally, SiNW arrays inside Si trenches were achieved by immersing the samples in a mixture of 10 wt. % HF and 1.5 wt. % H_2O_2. SEM images of the final wire-in-channel structures with two different periods are shown in **Figure 5.4(e)** and **(f)**. The curved bottom may be the result of poor mixing of the etchant solution at the bottom of the trenches.

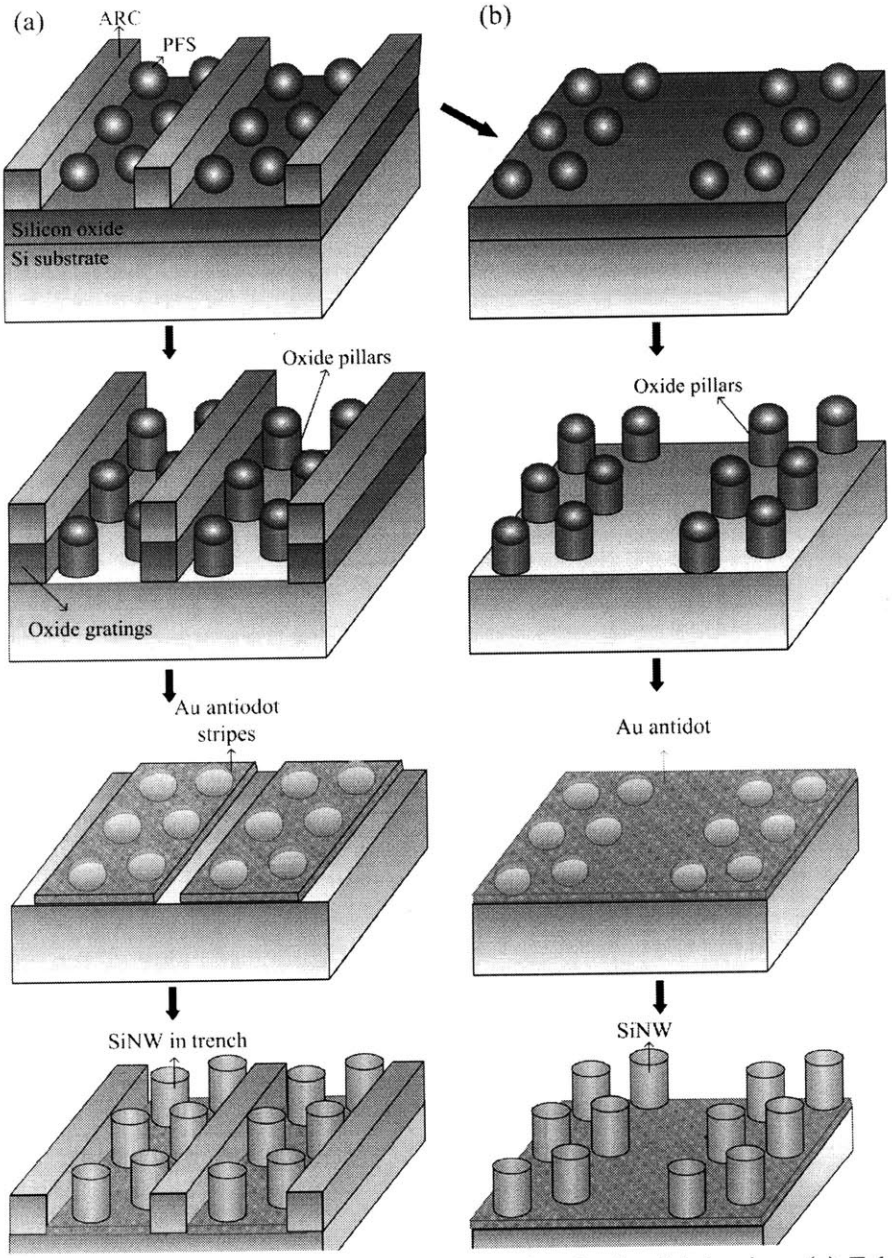

Figure 5.3 Schematic of the process flow for templated wire fabrication: (a) Fabrication of SiNW-in-trench structure: PFS spherical domains after annealing and removal of the PS matrix; Oxide grating and oxide pillars after RIE using the PFS spheres and ARC grating as etch masks; Au thin film stripes with nanohole arrays after lift-off in HF; SiNW arrays inside trenches after metal-assisted etching; (b) Fabrication of ordered SiNW array using a removable ARC grating: Removal of ARC grating; oxide pillar arrays after RIE using the PFS spheres as etch masks; Continuous Au thin film with stripes of nanohole arrays; SiNW clusters on a flat substrate.

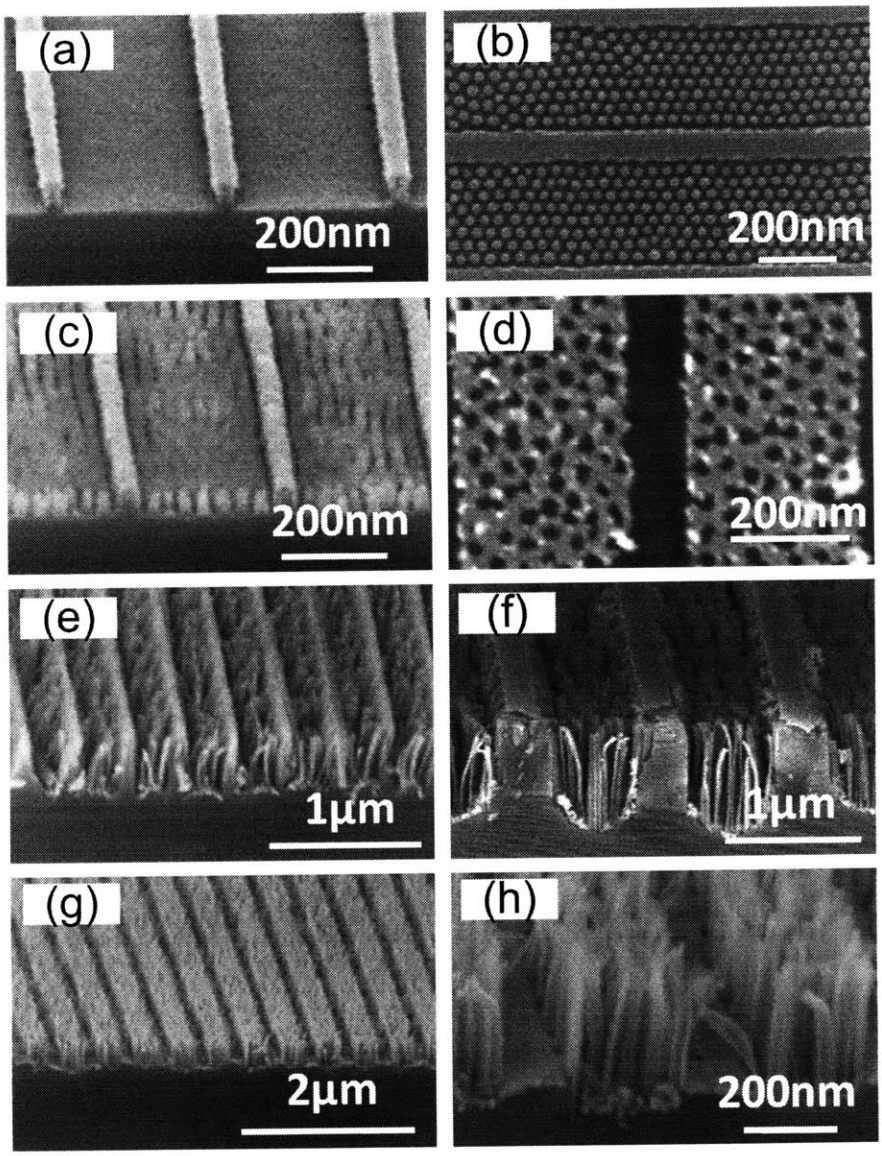

Figure 5.4 SEM images of templated SiNW fabrication: (a) ARC gratings (period = 350 nm) fabricated using interference lithography; (b) PS-*b*-PFS 47/15 self-assembled inside gratings, shown after the PS matrix has been removed by oxygen RIE; (c) Oxide pillar arrays in oxide gratings; (d) 10 nm thick Au antidot arrays after HF lift-off; (e) Final wire-in-trench structure after etching in a solution of hydrofluoric acid and hydrogen peroxide; (f) Wires etched in a different grating with a 1000 nm period (made from PS-*b*-PFS 47/15); (g) Strips of SiNW arrays patterned using a removable ARC grating (made from PS-*b*-PFS 43/12); (c) Higher magnification image of wire arrays without the trench structure.

A variation of the nanowire-in-channel process was used to form SiNW arrays without the trench structure, which is illustrated schematically in **Figure 5.3(b)**. After templated self assembly of PS-*b*-PFS microdomains in ARC gratings and removal of the PS matrix, the ARC gratings were removed by soaking in n-methyl pyrrolidone (NMP) to leave behind only rows of PFS spherical microdomains (79). The polymer was protected against dissolution in solvents by an inorganic oxide shell formed during the oxygen RIE process. A gold thin film was then deposited through the oxide pillars. Patterned nanohole arrays in a continuous gold thin film extending over the entire substrate were created using HF lift-off. Etching in HF/H_2O_2 led to formation of rows of free-standing silicon nanowire clusters on a flat substrate, as shown in **Figure 5.4(g)** and **(h)**.

5.3 Control of wire size distributions, aspect ratios, densities, and locations

The control of the size, density, and location of nanowires is critical for array-type device applications. In our process, the monodispersity of the SiNWs is governed both by the size distribution of the PFS spheres, and by the fidelity of pattern transfer into the gold and subsequently into the Si. The size distributions of wires patterned using PS-*b*-PFS 47/15 and PS-*b*-PFS 43/12 are plotted in **Figure 5.5**. The wire diameters were measured using a public domain image processing software ImageJ from SEM images taken at several locations on the

sample. The average and standard deviation of the diameters measured for wires made using PS-*b*-PFS 47/15 and PS-*b*-PFS 43/12 were 22.06 nm ±14.14% and 19.55 nm ±18.11%, respectively, while the average diameter and standard deviation of the etched PFS domains were 24.92 nm ±12.24% for 47/15 and 21.68±16.01% for 43/12, and the period was 35 nm for 47/15 and 29.5 nm for 43/12. The average diameters of the wires were 2-3 nm smaller than that of the PFS spheres due to shrinkage of spheres during the subsequent dry etching steps.

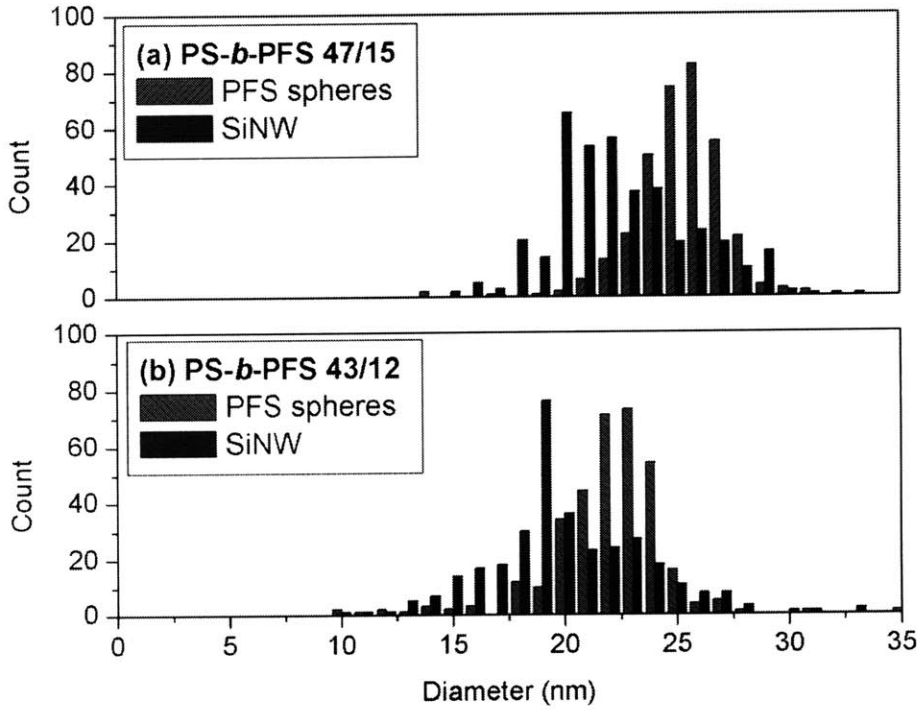

Figure 5.5 Diameter distributions for the wires and the PFS spherical microdomains: (a) PS-*b*-PFS 47/15 diblock copolymer, and (b) PS-*b*-PFS 43/12 diblock copolymer.

Comparing the standard deviations in PFS sphere and SiNW diameters, it is clear that the variability in NW diameters originates primarily from dispersity in the PFS sphere sizes, and

the subsequent liftoff and metal-assisted etching processes lead to only a minor broadening in NW diameter distribution. The distribution in sphere sizes is attributed to kinetic limitations during the microphase segregation of the PS-b-PFS. The polymers used in this study have a larger molecular weight than the PS-b-PFS 33/10 used in our previous work, and a correspondingly lower diffusivity and higher dispersity in sphere sizes. For comparison, a PS-b-PFS 91/21 spherical morphology block copolymer with period 56 nm, annealed at a higher temperature of 180°C for 48 hr, was used as an etch mask to form metal 'dots' with a standard deviation in of the diameter distribution of 9% (98). The low diffusivity of PS-b-PFS 47/15 and 43/12 is also believed responsible for the relatively poor long range ordering of the PFS spheres within the topographical templates [e.g. **Figure 5.4(b)**] compared to PS-b-PFS 33/10, which can order in grooves over defect-free distances of several microns (99).

The SiNWs made by this method are distinguished by a very high aspect ratio. It is commonly observed that high aspect-ratio structures cluster at their tips, due to van der Waals or electrostatic charges on the newly formed surfaces (100), facilitated by capillary forces present during drying after liquid immersion (101). If the attractive forces between wires are greater than the force required to bend the wires, sheaf-like structures result as the wires stick together, as shown in **Figure 5.6(a)**. The capillary force present during drying results primarily from surface tension at the solid-liquid interface as the liquid evaporates. To

circumvent this problem, the sample is subjected to critical point drying (CPD) in which the liquid-to-vapor phase transition occurs continuously at the critical point. This is accomplished by heating a liquid in a closed system to reach the critical pressure at the critical temperature. The liquid and gas states of a substance are no longer distinguishable at this point. The liquid within the specimen can therefore pass from the liquid to gas phase with zero surface tension. In our system, CO_2 serves as the medium for the CPD procedure. Since it is not miscible with water, the water is first replaced with alcohol as an intermediate fluid. The result of the CPD process is shown in **Figure 5.6(b)**. Silicon nanowires with aspect ratios as high as 220 with very little clustering were fabricated using this technique.

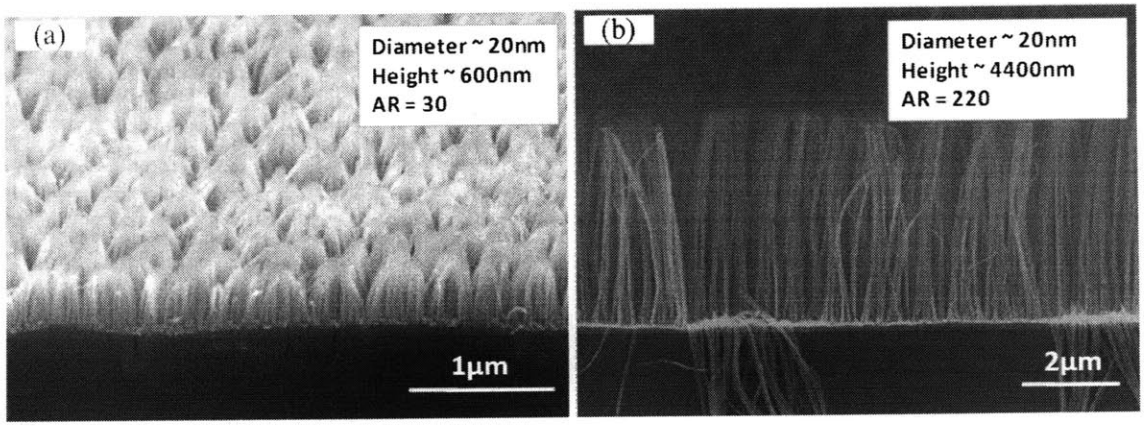

Figure 5.6 (a) SiNW arrays without critical point drying show clustering at the wire tips at a relatively low aspect ratio of 30; (b) SiNW arrays with critical point drying show much less bending at aspect ratios as high as 220. PS-*b*-PFS 47/15 was used in both cases.

The crystallinity of the SiNWs was investigated using high resolution transmission electron microscopy (HRTEM). **Figure 5.2(e)** shows a typical TEM image of a wire array and

Figure 5.2(f) shows a HRTEM image of a single SiNW. The single crystallinity and crystallographic orientation of the wires were investigated by selected area electron diffraction (SAED) of regions encompassing both the wires and the substrate, and fast Fourier transform (FFT) of a single wire. As shown in the insets of **Figure 5.2(e)**, the SAED patterns of the Si (100) substrate (upper inset) and the wires (lower inset) are nearly identical. The smearing of the diffraction patterns of the wires can be attributed to wire bending from the embedded epoxy. The FFT pattern also shows that the axial orientation of the SiNW is along the [100] direction. The result was expected as the wires were directly etched from the [100] single-crystal silicon substrate. In addition to the good crystallinity of the nanowires, we also expect little diffusion of gold into the wires because the complete wire forming process is carried out at room temperature. The gold catalyst film can be readily removed by immersing the sample in commercially available iodine-based gold etchants.

5.4 Conclusion

We fabricated dense arrays of high-aspect ratio, single crystalline silicon nanowires using a combined approach consisting of metal-assisted etching and block copolymer lithography. The high aspect ratio was made possible through use of critical point drying, which significantly reduced clustering at the wire tips. We also demonstrated fabrication of silicon nanowire arrays at lithographically defined locations by first assembling the block copolymer

in topographic features. Although the process was demonstrated using gratings, it can be easily applied to other physical template geometries. The excellent control that is possible in the placement accuracy, size, and geometry of block copolymer microdomains (95) (102), which includes the formation of both square symmetry (103) and close packed arrays, allows for extensive flexibility in the placement of wires at desired locations over a large areas. This will facilitate broad use of such arrays in photonic and sensing devices, in which high device densities and/or high surface-to-volume ratios are critical for optimum performance.

Chapter 6. Vertically Aligned Polysilicon and Amorphous Silicon Nanowire Arrays by Etching Direction Confinement: Effect of Catalyst Geometries

6.1 Introduction

Silicon nanowires have attracted considerable attention owing to novel properties arising from their quasi-one-dimensional nature (104). To date, a wide range of applications including electronic devices (81) (105) , biochemical sensors (106), energy storage devices (107), and thermoelectrics (92) have been demonstrated using silicon nanowires as building blocks. Currently, the most commonly used method to produce silicon nanowires is by vapor-liquid-solid (VLS) growth where metal catalysts such as gold are used to catalyze nanowire growth in a chemical vapor deposition (CVD) process (84). However, integration of VLS-grown wires with current silicon technology remains challenging due to issues such as in-diffusion of catalyst metal at elevated growth temperatures, and orientation control (87). In addition, control over wire morphology, which is key to successful property characterization and device applications, is very difficult to achieve using the VLS method.

Metal-catalyzed etching provides a promising alternative tool for the fabrication of high-aspect-ratio silicon nanostructures. In this approach metal particles or perforated films are used to facilitate the etching of silicon in a solution consisting of hydrofluoric acid and an oxidant. We and many others have demonstrated the use of metal-catalyzed etching in

conjunction with various metal catalyst film patterning techniques for the fabrication of single-crystal silicon nanowires from single-crystal wafers (51)' (54) (108) (55). However, despite recent progress in both the fabrication and application of chemically-etched silicon nanowires, relatively little is known about the etching mechanisms. In particular, the crystallographic-orientation dependence of the etching behavior is an important aspect one must understand in order to achieve good orientation control.

Recently, Huang *et al.* reported a systematic study of the catalyst-morphology dependence of the metal-assisted etching of Si(110) single-crystal substrates (109). Their results showed that in the case of isolated metal particles or relatively small patches of metal films with perforating nanoholes, the etching direction was predominantly <100>, and in the case of a continuous metal film with perforating holes extending over a sufficiently large area, the direction of etching can be confined to the vertical $[\bar{1}\,\bar{1}\,0]$direction. Utilizing this etching suppression behavior, they successfully fabricated vertically-aligned silicon nanowires on Si(110) substrates using a porous anodic alumina template as a silver deposition mask. In a similar study on substrate orientation dependence, Zhang *et al.* also showed that etching proceeded predominantly in the <100> direction when a silver network deposited using electroless deposition was employed as the catalyst (100).

In this chapter, we build upon these results and show that the key to vertical etching lies in other critical dimensions of the metal mesh; i.e. for any given area of the metal mesh, vertical

confinement depends on the relative ratio of the hole spacing to the film thickness. The hole spacing in a mesh is defined as the distance between two nearest-neighbor nanoholes for both hexagonal and square arrays, as shown in **Figure 6.1**. We present a systematic investigation of metal-assisted etching of Si(100), Si(110), and Si(111) substrates using metal catalysts with three varying morphologies: isolated particles, metal mesh with small hole spacings, and metal mesh with large hole spacings. We also demonstrated that the metal catalyzed etching method can be extended to the fabrication of vertically-aligned one-dimensional polysilicon and amorphous silicon nanostructures.

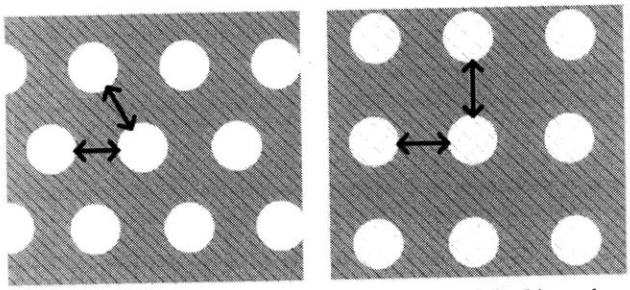

Figure 6.1 Schematic drawing of metal meshes with hexagonal (left) and square array of holes (right). The hole spacing (represented by the arrows) is defined as the nearest-neighbor distance between two nanoholes.

6.2 Etching direction dependence on catalyst geometries

Both n- and p-type silicon substrates with orientations (100), (110), and (111) were used in this study. The general etching behavior was similar for both doping types and only results of n-type silicon are presented here. The resistivity was chosen to be 1-25 Ω-cm for all substrates to eliminate any possible effect that the doping level may have on the etching behavior. Au was chosen as the catalyst and was deposited using electron beam (ebeam) evaporation for all three

types of catalyst morphologies. For isolated Au particles, 2 nm of Au was deposited directly onto the silicon substrates. The discontinuous Au film morphology is best described as irregularly shaped Au islands of different sizes. For Au mesh with very fine hole spacings, the as-deposited catalyst film was patterned using block copolymer (BCP) lithography (55). The block copolymer used in this work was polystyrene- *block*-polyferrocenyldimethylsilane (denoted as PS-*b*-PFS) with a molecular weight of 47kg/mol for PS and 15kg/mol for PFS. The period was approximately 35 nm and the average diameter of a nanohole was 22 nm, giving a hole spacing of roughly 13 nm. The gold film thickness in this case was 12 nm. Finally, for Au mesh with relatively large hole spacings, interference lithography (IL) was used to pattern the as-deposited catalyst film (108). A square array of anti-reflection coating (ARC) pillars was first fabricated after a series of exposure and dry etching steps. 12 nm of gold was subsequently deposited through the ARC mask. A gold film with square arrays of perforating holes was obtained after removal of the ARC pillars. The array period was 400 nm and the hole diameter was 140 nm, giving a hole spacing of 260 nm. A detailed description of the film patterning processes for both BCP lithography and IL is discussed in **Chapter 4**. Scanning electron microscope (SEM) images of the three different Au morphologies are shown in **Figure 6.2**.

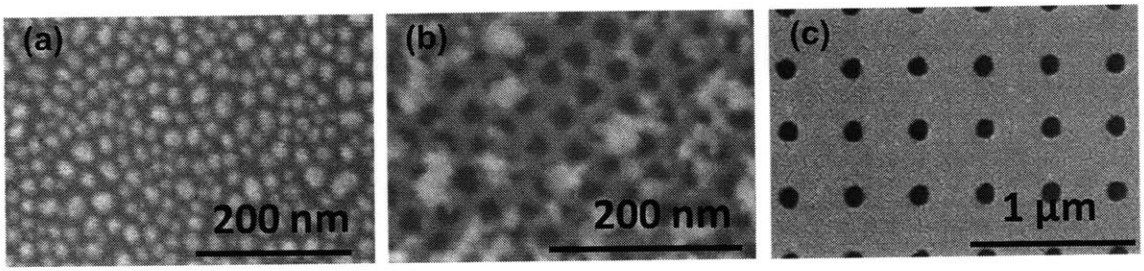

Figure 6.2 SEM images of metal catalysts of three different morphologies: (a) isolated Au islands deposited using direct electron beam (ebeam) evaporation; (b) Au mesh with small hole spacings patterned using block copolymer (BCP) lithography; (c) Au mesh with relatively large hole spacings patterned using interference lithography (IL).

After catalyst deposition, etching was carried out by immersing the samples in a mixed solution of hydrofluoric acid (HF), hydrogen peroxide (H_2O_2), and water (10 wt% HF and 1.5 wt% H_2O_2) for 5-15 minutes in ambient light. Post-etching drying for the BCP-patterned sample was done in a critical point drier after thoroughly rinsing with alcohol several times, as these high aspect ratio structures otherwise tend to cluster at their tips to form sheaflike structures due to the capillary force present during conventional drying (55). This was not necessary for the interference-lithography-patterned sample since the aspect ratio of the pillar is smaller, so that the pillars are stiffer and cannot be bent by capillary forces sufficiently to cause tip stiction. The IL-patterned samples were rinsed with isopropanol and blow-dried with nitrogen after the etching procedure.

Figure 6.3 shows representative SEM images of the silicon nanostructures that resulted from etching. Each of the three columns shows images from substrates of three different crystal orientations – N(100), N(110), and N(111) silicon. Each of the three rows shows images from Au catalysts of three different morphologies – isolated nanoparticles, fine metal

mesh with small hole spacings, and wide metal mesh with large hole spacings. Comparing silicon nanostructures etched using isolated Au nanoparticles (a, b, and c) and metal mesh with large hole spacings as catalysts (g, h, and i), the former case clearly shows etching in the <100> direction, whereas the latter shows vertical etching. This result is consistent with earlier results presented by Huang *et al.*, in which the crystallographically preferred <100> direction was suppressed and vertical etching resulted for a metal film with perforating nanoholes extending over a large area on the substrate (109).

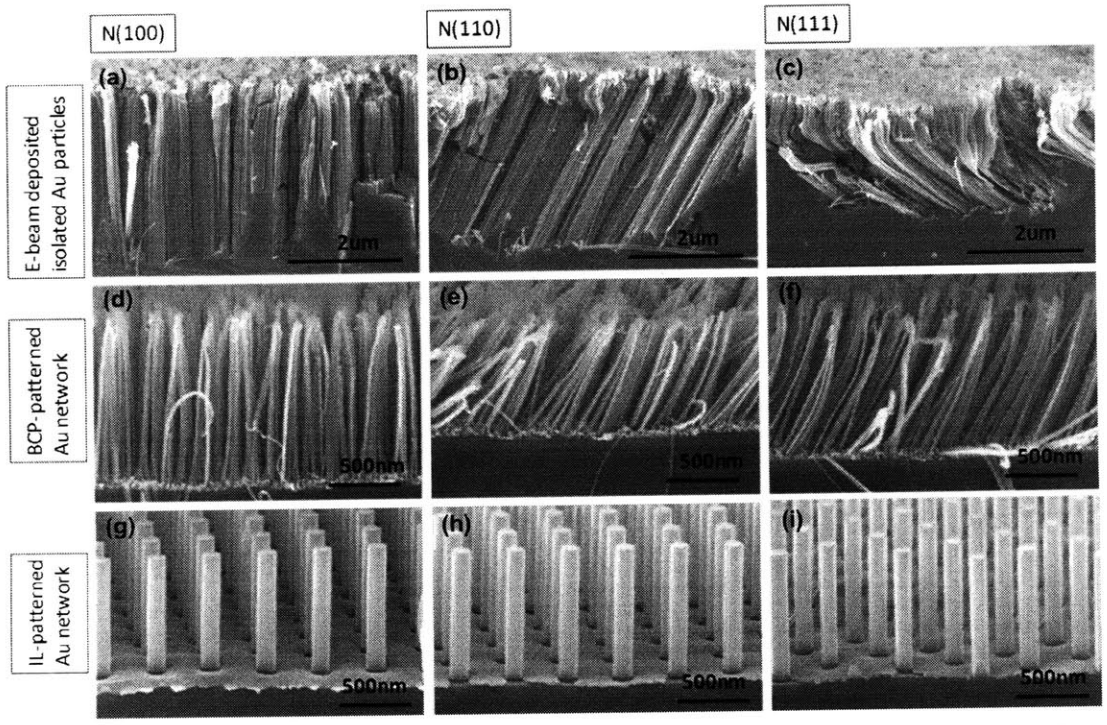

Figure 6.3 SEM images of etching results from silicon substrates three different crystallographic orientations and Au catalysts of three differet morphologies: (a)-(c) isolated Au islands deposited using ebeam evaporation on N(100), N(110), and N(111) silicon substrates, respectively; (d)-(f) Au mesh with small hole spacings patterned using BCP lithography on N(100), N(110), and N(111) silicon substrates, respectively; (g)-(i) Au mesh with relatively large hole spacings patterned using IL on N(100), N(110), and N(111) silicon substrates, respectively.

By comparing silicon nanostructures etched using metal meshes with large hole spacings (g, h, and i) to those made using very small hole spacings (d, e, and f), we further conclude that the hole spacing also plays an important role in determining the etching direction. In contrast with the vertical etching of the IL-patterned samples, in the case of a BCP-patterned fine metal mesh, etching occurred in the preferred <100> direction. The variation in angle of the fine nanowires in the SEM image is an artifact of cleaving for cross sectional SEM sample preparation. This is different from previous results presented by Huang *et al.*, in which etching occurred in the <100> direction for small-area patches of metal network (e.g. a Ag mesh originally covering a large substrate area broken into smaller patches due to Ag dissolution in the etchant solution) and should provide further insight into how to better control the orientation of the etched nanowires. In other words, even if the overall catalyst film area is sufficiently large (in our case over centimeter-scale area), if the hole spacing is too narrow, inclined etching will still occur. On the other hand, even if the overall catalyst film area is sufficiently small, if the hole spacing is large enough, the etching direction can be confined in the normal direction to the substrate surface. The latter can be further confirmed by patterning a small area Au catalyst mesh with large hole spacings on Si n(110) substrate. Etching was still confined to the vertical direction even though the film was only micrometers in size, as shown in **Figure 6.4**. The templated nanosphere lithography process is discussed in greater detail in **Chapter 4**.

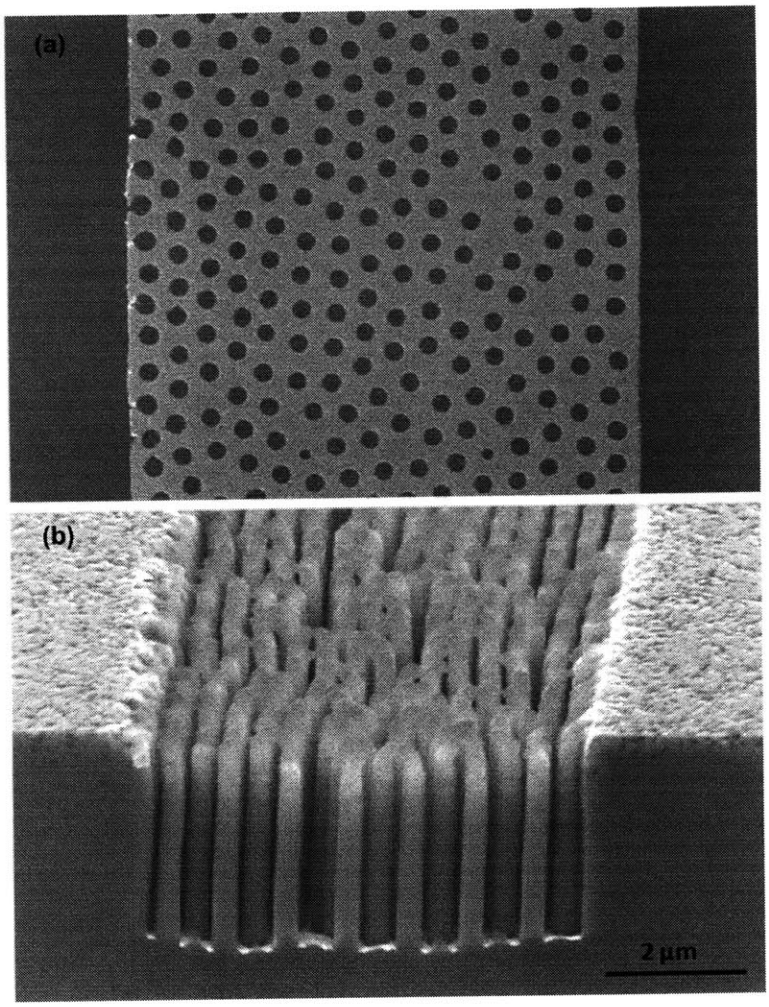

Figure 6.4 SEM images of (a) a small patch of metal film with perforating hole arrays on a Si N(110) substrate, and (b) vertical silicon nanopillar arrays after metal-assisted etching.

If we regard the inclined etching as a result of the vector addition of vertical and lateral movement, as shown in **Figure 6.5**, we expect etching for isolated particles to proceed in the preferential <100> direction as the catalyst is free to move in either the vertical or the horizontal direction. In contrast, for a large-spacing metal mesh, catalyst movement is confined in the vertical direction as lateral movement is severely restricted. The BCP-patterned fine metal mesh has a hole spacing of 13 nm, comparable to the metal film

thickness which was 12 nm; i.e. in cross section, the interconnected Au lines should have roughly the same width as the thickness. As a result, lateral etching is not as restricted as for the IL-patterned mesh, thus allowing etching to proceed in the crystallographically preferred <100> direction. In addition to the etching direction dependence on catalyst geometries, Huang *et al.* also observed well-defined domains for isolated Au particles in which etching occurred in one of the two preferred $[\bar{1}00]$ or $[0\bar{1}0]$ directions for Si(110) substrates. In our case, no domain formation was observed for etching using the BCP-patterned metal catalyst since the interconnected network forces etching to proceed in one direction over the entire substrate.

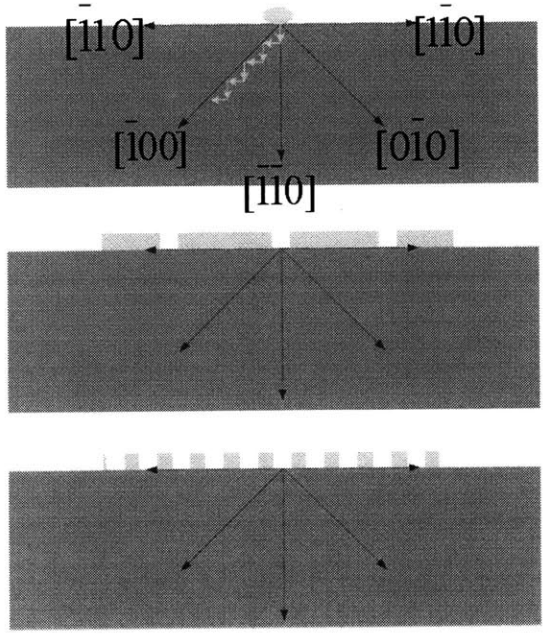

Figure 6.5 The inclined etching can be regarded as a vector addition of the horizontal and vertical movement of the catalyst. An example is illustrated for a (110)-oriented silicon substrate. Three different catalyst geometries are shown: isolated particles (top), metal mesh with large hole spacings (middle), and metal mesh with small hole spacings (bottom).

6.3 Fabrication of amorphous and polysilicon nanowire arrays

By utilizing the confinement effect associated with relatively large hole spacings, we have successfully shown that vertically-aligned 1D silicon nanostructures can be obtained regardless of crystallographic orientation of the silicon from which they are etched, as demonstrated for both n- and p-type Si(100), (110), and (111) substrates. The method can be further extended to fabrication of vertically-aligned polycrystalline and amorphous silicon nanostructures by suppressing etching directions other than those normal to the original surface.

To form amorphous and poly-silicon nanostructures, un-doped amorphous and poly-silicon thin films were deposited on p-type Si(100) substrates with a film thickness of approximately 1.2 and 1.1 μm, respectively. The amorphous silicon thin film was deposited using ebeam evaporation at room temperature, and the polysilicon thin film was deposited using low pressure chemical vapor deposition (LPCVD) at 625°C. Both samples were used in the as-deposited state without any further annealing. **Figure 6.6(a)** and **(b)** show SEM images of the as-deposited samples.

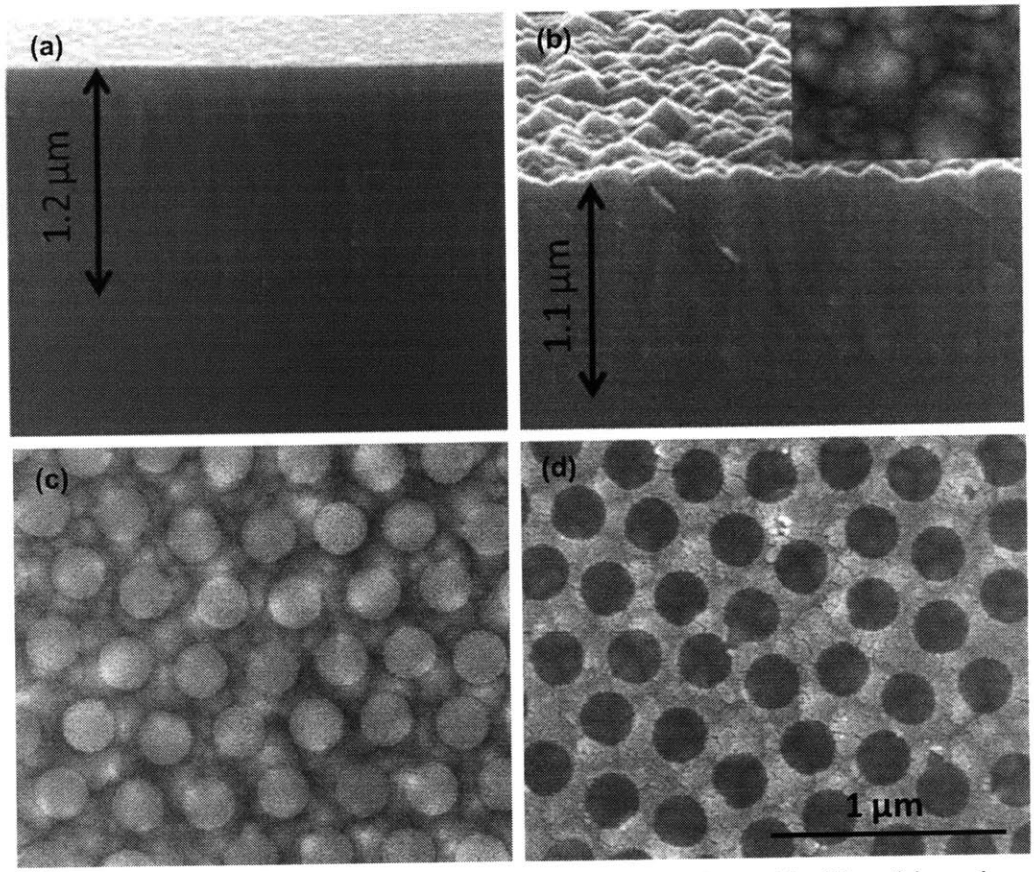

Figure 6.6 SEM images of (a) as-deposited amorphous silicon thin film; (b) as-deposited polysilicon thin film on p-type Si(100) substrates. (c) and (d) are SEM images of polystyrene nanospheres with reduced diameter serving as a metal deposition mask, and gold catalyst film with a hexagonal array of perforating holes, respectively, on a polysilicon sample.

Au films with nominal thicknesses of 2 nm and in the form of isolated islands were deposited using electron beam evaporation onto both types of substrates. For comparison, Au meshes were patterned using nanosphere lithography (53). A monolayer of polystyrene spheres with an average diameter of 330 nm was first coated onto the substrates by dip-coating using a home-built dip-coater. A dry etching step was carried out using reactive ion etching (RIE) in an oxygen plasma to reduce the sphere diameter. A gold mesh with a relatively large hole spacings (> 120 nm) was obtained after ebeam evaporation of Au through the polystyrene

mask and lift-off in toluene to remove the gold-coated spheres. The polystyrene metal deposition mask after RIE and the resulting gold mesh are shown in **Figure 6.6(c)** and **(d)**, respectively. Etching was then carried out in a solution consisting of HF, H_2O_2, and water (10 wt% HF, 0.15 wt% H_2O_2). The concentration of the H_2O_2 was reduced by a factor of 10 compared to the etchant concentration used for single-crystal silicon etching to slow down the etch rate as etching occurred very rapidly and violent bubble formation was otherwise observed for amorphous silicon.

Figure 6.7 shows etching results for both polycrystalline and amorphous silicon thin films. In the case of isolated gold particles on polycrystalline silicon, etching proceeded in different directions for each particle. As shown in **Figure 6.7(a)**, only under a certain particles did the Au catalyst etch through the polysilicon thin film to continue into the underlying single-crystal Si(100) substrate, where vertical etching was observed. This was expected as isolated catalyst particles tend to move in the <100> direction. As a result of the random etching directions in the polycrystalline silicon, some of the Au particles never reached the polysilicon/substrate interface. For isolated gold particles on amorphous silicon, etching appeared to be mostly vertical with the particles moving collectively in the same direction. Although the actual etching direction could not be determined as the resulting structure lacked structural integrity and collapsed very easily, the vertical etching in the amorphous silicon layer can be confirmed by the relatively high ratio of Au particles that reached the amorphous/substrate interface and

continued to catalyze etching into the Si(100) substrate, as shown in **Figure 6.7(b)**. The collective movement suggested some type of interaction with neighboring particles. The vertical etching direction could be attributed to the formation of an intermediate oxide state due to a high local current density, analogous to the vertical etching of non-(100) oriented single crystal silicon when a high oxidant concentration is used (45). However, more detailed studies are required to understand the etching behavior in amorphous silicon. In contrast to isolated catalyst particles, in the case of metal mesh with relatively large hole spacings, etching proceeded in the vertical direction for both polycrystalline and amorphous films. **Figure 6.7(c)** and **(d)** show catalytically-etched polycrystalline silicon and amorphous silicon nanopillars, respectively.

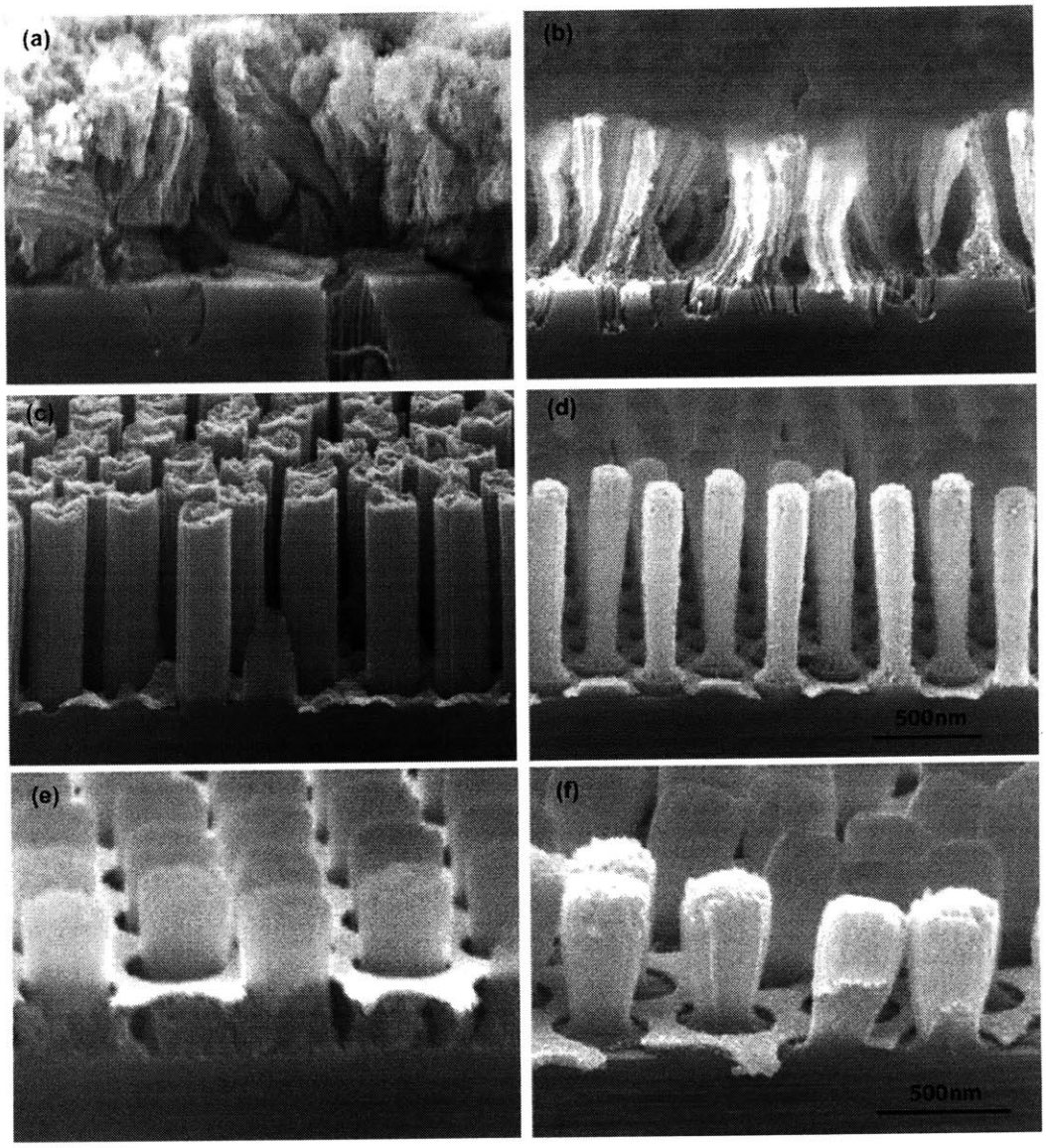

Figure 6.7 SEM images of results of metal-assisted etching of (a) isolated Au particles on polycrystalline silicon; (b) isolated Au particles on amorphous silicon; (c) A Au mesh with relatively large hole spacings on polysilicon; (d) A Au mesh with relatively large hole spacings on amorphous silicon; (e) After etching for only 1 min, with the Au mesh etching only partially through the 300 nm-thick amorphous silicon thin film; (f) After etching for 3 min, resulting in the baseball-bat-like shape of the amorphous silicon nanopillars.

Pillar or wire arrays made from polyscrystalline and amorphous films are of special interest for device applications because they can be formed on a very wide array of substrates, including large-area, conformable substrates, and are not restricted by the use of costly single

crystal wafers. In addition, polycrystalline and amorphous films can be deposited at relatively low temperatures, allowing further flexibility in substrate selection and the possibility of stacking of nanowire arrays without severe constraints. For example, solar cells based on planar amorphous silicon (110) and microcrystalline silicon (111) have well-established commercial markets. High surface-to-volume ratio nanostructures based on amorphous and polysilicon patterned arrays may be desirable as potential materials for solar cell photoanodes. Although vertically oriented amorphous nanowires can be synthesized using evaporation methods based on the solid-liquid-solid (SLS) growth mechanism (112), the high temperature requirement severely limits the substrates that can be used. Polycrystalline silicon nanowire synthesis has also been demonstrated using VLS-based methods (113). However, this method faces similar challenges associated with the high growth temperature as in the case of VLS-grown single crystal silicon nanowires. A room temperature process to achieve these nanostructures such as presented here is therefore particularly attractive.

Upon closer examination, the polysilicon nanopillars are characterized by a vertical side wall similar to their single-crystal counterparts,. On the other hand, the amorphous silicon nanopillars exhibit a "baseball bat" shape where the diameter gradually decreases towards the bottom of the pillars. One possible explanation may lie in the extremely fast etch rate of amorphous silicon in comparison to crystalline silicon. For example, for the same etchant concentration (10 wt% HF, 0.15 wt% H_2O_2), the time required to etch approximately 1 μm into

the silicon thin films was 3 min for amorphous silicon and 10 min for polycrystalline silicon. As a result of the etch rate difference, the vertical movement of the Au mesh was slowed down significantly when it reached the silicon substrate. It is commonly believed that in metal-assisted etching, the metal significantly enhances the silicon etch rate by catalyzing reduction of the oxidant in the etchant solution. Chartier *et al.* suggested that one reason that holes are consumed at the perimeter of the catalyst could be that a charge depletion layer exists around the metal catalysts, leading to a lower energy barrier for holes at the interface (58). They also suggested that since HF must have access to the metal/Si interface during the etching process, the metal/Si contact must be intermittent at best. For amorphous silicon, the dissolution of silicon may have advanced much further into the depletion layer than it would have for crystalline silicon before the metal film loses contact with the sidewalls of the etched structures and proceeds to sink deeper into the silicon thin film. This can be seen in **Figure 6.7(e)** where the pillar diameter is clearly smaller than the diameter of the perforating holes in the Au thin film. In this case, since the Au film only moved down partially through the amorphous thin film, the sidewalls of the nanopillars still remained vertical. As the vertical movement of the Au catalyst film was slowed down at the interface, further catalyzed dissolution of the amorphous silicon near the interface can occur for a longer period of time, resulting in the bat-like shape as shown in **Figure 6.7(f)**.

It is worth noting that the structure of the amorphous silicon pillars appears to be very

spongy and therefore lacked good structural integrity. This may be the result of the low density of amorphous films deposited at room temperature. Similar to the case of high aspect ratio silicon nanowires patterned using BCP lithography, when the surface tension force exerted on the nanowires during drying exceed the force required to bend the wires, sheaflike structures result as the wires stick together at the tip. Since the amorphous wires are much less stiff in comparison to their crystalline counterparts, the nanostructures easily collapse even at a much smaller aspect ratio. SEM images of such collapsed structures are shown in **Figure 6.8**. For the case of amorphous silicon nanopillars, the attractive forces between pillars are so great that the pillars detached from the crystalline silicon substrate and stuck together in sheaves. In order to eliminate surface-tension-induced stiction, post-etching drying must be done in a critical point drier.

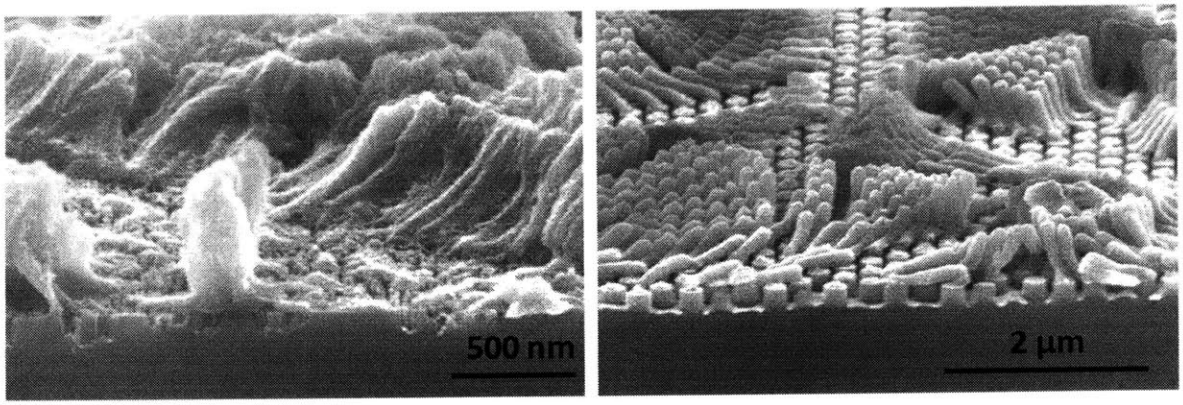

Figure 6.8 Amorphous silicon etching with both isolated Au nanoparticles (left) and Au mesh (right) without critical point drying.

To further investigate the structure of the polycrystalline and amorphous silicon nanostructures, transmission electron microscopy (TEM) was carried out. Error! Reference

ource not found.**(a)** shows a typical TEM image of a polysilicon nanopillar array that has not etched all the way through the polysilicon thin film. The grain structure is clearly columnar. The polycrystalline nature of the pillars can be further confirmed by the ring pattern in selected area electron diffraction (SAED), as shown in the inset. **Figure 6.9(b)** shows a typical TEM image of an amorphous silicon nanopillar array. Although there appears to be a coating surrounding the pillars in the image, this is actually a result of sample preparation. As the TEM foil becomes thicker towards the right of the image, multiple layers of pillars are shown. The lighter color contrast of the pillars in contrast to the substrate indicates a smaller silicon density.

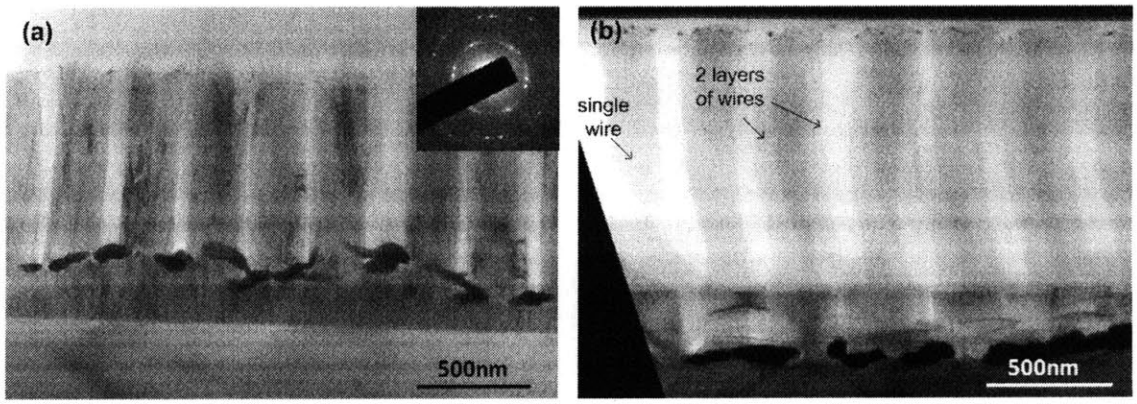

Figure 6.9 Transmission electron microscope (TEM) images of (a) polycrystalline silicon nanopillars, and (b) amorphous silicon nanopillars. Inset in (a) shows the selected area electron diffraction (SAED) pattern.

6.4 Conclusion

In summary, we have demonstrated that in addition to having a mesh structure, the spacing between the perforations (e.g. holes) is a critical factor in determining the catalytic etching direction. For isolated catalyst nanoparticles and catalyst mesh with small hole spacings, etching occurs in the preferential <100> direction. An explanation for the inclined

etching was presented. Where both vertical and lateral movement of the catalyst are unrestricted, as in the case for isolated particles and the BCP-patterned films where the hole spacing is comparable to the film thickness, etching in the <100> direction is preferred. By having a mesh with relatively large hole spacings, etching is forced to proceed in a single direction normal to the silicon surface as a result of restricted horizontal movement for the mesh. Based on these results, we have shown that mesh geometries can be chosen for which the crystallographic orientation of the silicon substrate *does not* affect the orientation of the etched wires. This was demosntrated for both n- and p-type Si(100), (110), and (111) substrates.

We have also demonstrated that by properly choosing the mesh geometries, nanowire arrays of polycrystalline and amorphous silicon can be created using metal-catalyzed etching. For isolated Au nanoparticles, etching occurred in different directions for each particle on polycrystalline silicon. On the other hand, collective movement of the catalyst particles in the vertical direction was observed on amorphous silicon substrates. Vertically-aligned nanopillar arrays were obtained for both poly- and amorphous silicon when mesh with relatively large hole spacings was employed for catalysis. Although we have demonstrated nanopillar fabrication on crystalline silicon substrates, this process can be used to fabricate functional silicon nanowire arrays using silicon films of *any* crystal structure (i.e. single crystal, polycrystalline, or amorphous) deposited on *any* substrate including those of very large sizes or

even flexible plastic substrates. This will enable the use of metal-catalyzed etching to form functional silicon nanowire arrays and thereby fabricate silicon-nanowire-based devices in much more flexible and much lower-cost ways.

Chapter 7. Fabrication of Silicon Nanopillar-Based Nanocapacitor Arrays

7.1 Introduction

Even after more than a decade of research, energy autonomy continues to be a major challenge for portable electronic devices, with batteries remaining the dominant choice as an energy source. Despite recent developments in battery technology, a practical compromise still has to be made between energy capacity versus the size and weight of the batteries. Accordingly, significant resources are being put toward research and development of alternative energy solutions that are high-capacity, lightweight and compact. Some examples include miniature fuel cell (114), plastic solar cells (115), and energy harvesting systems (116).

In all the cases above, energy buffering is often needed to maintain continuous and stable power output to the connected devices. For example, fuel cell systems are generally known to have slow start-up time and slow dynamics. A hybrid system in which the fuel cell supplies the base power and the energy buffer supplies the start-up power is therefore desired (117). Energy scavenging systems which rely on environmental energy sources such as thermal, vibration, and solar energies are an alternative to high capacity batteries. However, these sources are not constantly available so that buffering is needed to ensure uninterrupted device operation. Furthermore, when the peak load demand goes beyond what is achievable by these power generation systems, buffering can provide the required power to satisfy the peak demand.

Generally speaking, the energy buffer can either be a battery or a capacitor. One important drawback of using a battery is its limited discharging efficiency. Capacitors, on the other hand, allow for much higher discharging current due to its lower internal resistance. Other advantages of using an ultracapacitor as an energy buffer include longer life cycles and high power density. While batteries generally have higher energy capacities, ultracapacitors can be used when high capacities are not needed, or can be used in conjunction with batteries when both high capacity and high discharge rates are needed.

In addition to the advantages discussed above, with proper materials and structural design, ultracapacitors can also be scaled down relatively easily compared to batteries. Much effort has been expended on reduction of the footprint of capacitors while maintaining high capacitance densities. Approaches include introduction of new materials such as high-k dielectrics, and three-dimensional (3D) capacitor designs such as stacked and deep-trench capacitors to achieve a larger capacitor electrode area. In the latter case, a larger capacitor electrode area is achieved by building the capacitor either in the silicon surface (trench capacitor) or above the silicon surface (stacked capacitor). For stacked capacitors, it is difficult to increase the surface area indefinitely and is therefore necessary to use high-k materials to further reduce cell sizes. In contrast, the total effective surface area of deep-trench capacitors can be increased simply by etching deeper trenches. High aspect ratio trenches combined with metal deposition techniques with good step coverage can help significantly increase the

capacitance density. For example, capacitance densities of up to 440 nF mm^{-2} has been demonstrated with trench capacitors containing multiple metal-insulator-metal(MIM) layer stacks deposited by atomic-layer deposition (ALD) (118).

In addition to the above-mentioned conventional 3D capacitor architectures, other innovative methods to achieve high capacitance structures by increasing capacitor areas have also been demonstrated. These methods include surface roughening and the introduction of high aspect-ratio structures such as nanotubes, nanowires, and coated nanopores as electrodes. One example of surface roughening is the use of a diblock copolymer template as an etch mask for silicon reactive ion etching (RIE). An increase of 30% in capacitance over planar structures has been demonstrated using this technique and further increase is expected by etching deeper into the silicon (119). However, high aspect ratios may prove to be difficult to achieve as the dry etching method is often limited by the degradation of the block copolymer mask. Similar limitations also apply to silicon pillar structures fabricated using conventional lithography and dry etching processes. A bottom-up approach using grown nanowires and nanotubes as well as anodic aluminum oxide (AAO) templates provides an alternative solution. For example, capacitance-voltage studies for small arrays of vertical InAs nanowires have been carried out using vapor-liquid-solid (VLS) grown wires (120). A metal-insulator-carbon nanotube-metal (MICNM) capacitor structure based on vertically-grown carbon nanotube arrays has also been demonstrated (121). Recently Banerjee *et al.* has reported the use of AAO in conjunction with

ALD to fabricate metal-insulator-metal capacitors with capacitance densities up to 100 $\mu F\ cm^{-2}$ for a 10 μm-thick AAO layer (122). However, although significant capacitance density increases have been achieved with these methods, they also have some limitations when it comes to integration with current silicon technologies with respect to both fabrication and operation. For example, growth of wires and tubes requires relatively high growth temperatures which might become problematic. AAO on silicon requires deposition of a thick aluminum layer which can lead to film delamination caused by stress during anodization, also making integration with current silicon technologies difficult. In addition, atomic layer deposition, while providing excellent step coverage and uniformity, still faces challenges such as throughput in high-volume production due to the tens and hundreds of pulse and purge cycles of the heated chemical precursors required to achieve useful thicknesses.

7.2 Nanocapacitor array fabrication

Here, we propose a simple capacitor design and fabrication method based on metal-assisted etching of silicon and electrodepostion. Metal-assisted etching in combination with different film patterning techniques has been demonstrated as a promising tool for high aspect ratio silicon nanostructure fabrication. We and many others have reported Si nanowire fabrication using this technique (51) (53) (54) (55). Electrodeposition is a film deposition process that provides good conformity and can be easily scaled up and automated for high volume production. Both processes share the advantages of low cost and high throughput and are

therefore suited for the fabrication of nanoscale capacitors in energy buffering systems and other applications such as dynamic random access memories (DRAMs), on-chip decoupling capacitors, and ferroelectric non-volatile memories (FERAMs).

The experimental procedure for the fabrication of a silicon nanopillar-based ultracapacitor array is illustrated schematically in **Figure 7.1** and scanning electron microscope (SEM) images of the resulting structures are shown in **Figure 7.2**. Detailed experimental procedures are discussed in **Chapter 4** and will only be briefly described here. Interference lithography was used to pattern the catalyst thin film. A trilayer stack consisting of BARLi anti-reflection coating (ARC), electron beam-deposited silicon oxide, and PFI-88 positive photoresist were first coated on a n^+ Si(100) substrate (Phosphorous-doped, resistivity = 0.001 – 0.005 Ω cm). A square array of photoresist posts was created after a two-beam exposure. The pillar pattern was subsequently transferred into the bottom ARC layer through a series of reactive ion etching steps. A gold catalyst film with a square array of perforating nanoholes was obtained after electron beam (ebeam) evaporation and lift-off. Finally Ordered arrays of silicon nanopillars with square symmetry were etched into the silicon substrate in a mixed solution of hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). A thin oxide layer serving as the dielectric was thermally grown over the nanopillar structure in a tube furnace in dry oxygen after removal of the gold catalyst. Since the oxide layer is insulating, a thin metal seed layer is required for subsequent electrodeposition. Some examples of the seed layer metals we used include gold,

gold-palladium, and tungsten deposited either by sputtering or electron-beam (e-beam) deposition. The Ni electrode was then electro-deposited using a teflon cell in a commercially available Ni plating solution (LECTRO-NIC® 10-03, Enthone) with a platinum anode. A constant current density of 3 - 9 mA/cm^2 was applied. Typical deposition time was 10 – 30 min. Aluminum was deposited using ebeam evaporation as the back electrode. As shown in **Figure 7.2(b)**, the deposited Ni formed a conformal layer covering the high aspect-ratio silicon nanostructures. Finally, a back aluminum electrode was deposited using e-beam deposition after the removal of the oxide on the back of the silicon. It should be noted that aside from the oxidation step, all other parts of this fabrication sequence was carried out at room temperature.

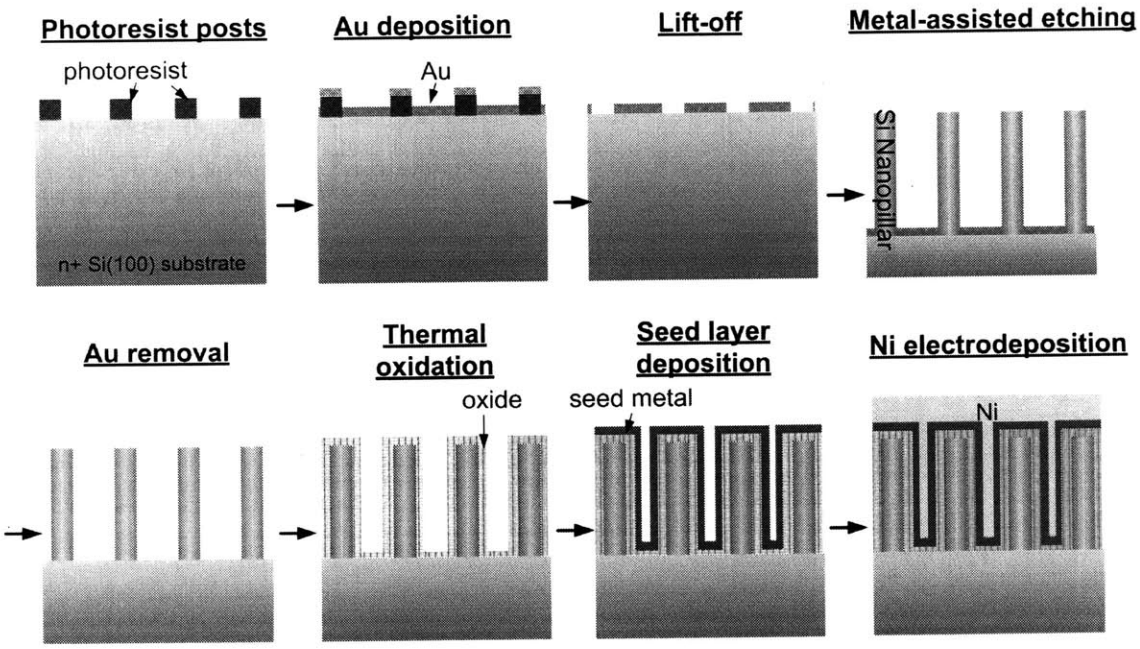

Figure 7.1 Schematic of the ultracapacitor array fabrication process: Photoresist posts fabricated using interference lithography; metal catalyst film deposited using electron beam deposition with the posts serving as a deposition mask; Au anti-dot array after lift-off of the pillars; silicon nanopillar array fabricated by metal-assisted etching with the remaining Au

catalyst film; silicon nanopillar array after removal of the Au catalyst; thermal growth of an oxide layer as the capacitor dielectric; thin metal layer used as a seed layer for electrodeposition deposited by either sputter deposition or electron beam deposition; Ni electrode deposited by electrodeposition.

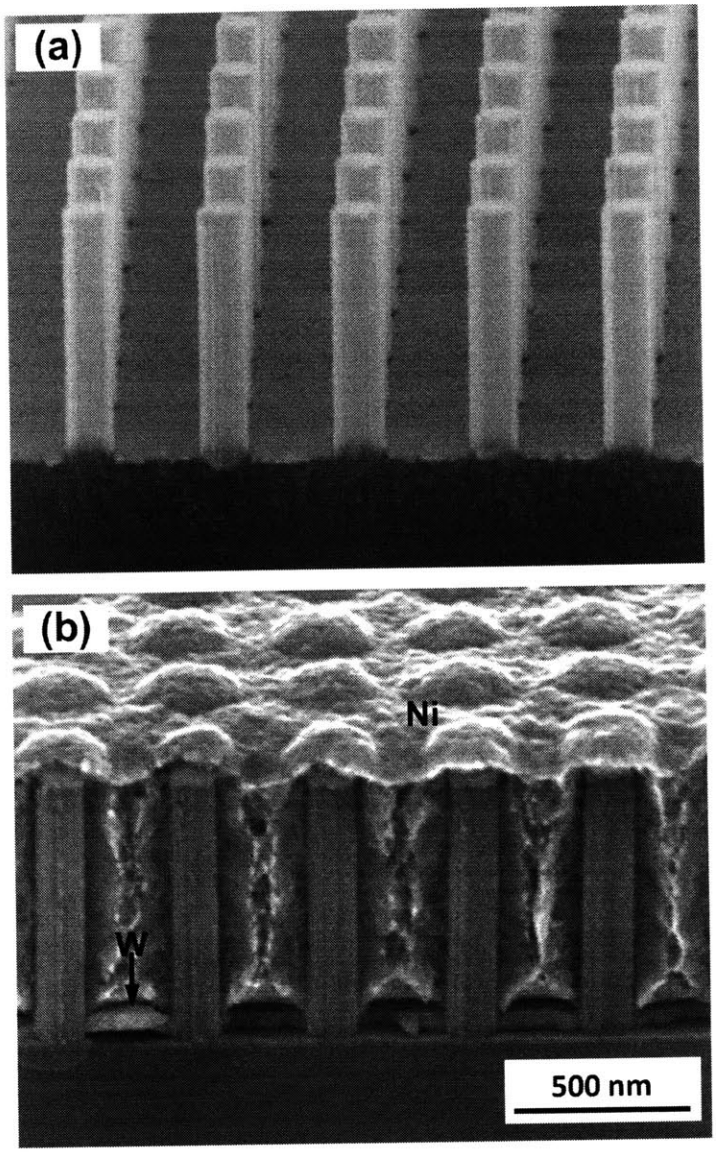

Figure 7.2 Scanning electron microscope (SEM) images showing (a) a silicon nanopillar array after metal-assisted etching using an interference lithography-patterned gold layer as the catalyst; (b) capacitor array after thermal oxidation, seed layer deposition (tungsten), and Ni electrodeposition.

7.3 Capacitance measurement results

The capacitance of the fabricated device was measured using an Agilent 4284A capacitance meter operating at 1 kHz. The measurement was carried out using a pre-calibrated fixture with copper foils serving as the front and back contact to the nanocapacitor device. We can estimate the expected capacitance value by considering the ultracapacitor structure as an array of cylindrical capacitors connected in parallel. For a single cylindrical capacitor, **Equation [7.1]** can be used to express the capacitance (123):

$$C_{single} = 2\pi\varepsilon_0\varepsilon_r l/\ln(b/a) \qquad [7.1]$$

where ε_0 is the permittivity in vacuum, ε_r is the dielectric constant, l is the height of the nanopillars, b is the coaxial diameter of the dielectric layer (SiO_2 in this case), and a is the inner diameter of the silicon pillar. Considering only a square array of cylindrical capacitors with period p and a nominal electrode area A (i.e. disregard the planar area in between the pillars), the total capacitance can be estimated as a sum of the capacitance values of all the capacitors in the electrode, as shown in **Equation [7.2]**:

$$C_{total} = \frac{C_{single}}{p^2} \cdot A = \frac{2\pi\varepsilon_0\varepsilon_r l/\ln(b/a)}{p^2} \cdot A \qquad [7.2]$$

According to this equation, high capacitance densities are achieved with a tall pillar height and a small period array. For example, for the tallest pillars arrays with the smaller periods we have fabricated (l = 1500 nm, p = 200 nm, b = 120 nm, a = 100 nm), the estimated capacitance density is 5.26 $\mu F/cm^2$, approximately a 12-fold increase compared to a parallel plate capacitor with the same oxide thickness footprint.

The capacitance density can be easily controlled by varying the pillar height and the period of the pillar array. According to **Equation [7.2]**, the capacitance scales linearly with the pillar height and inversely with the square of the period. **Figure 7.3(a)** shows the capacitance density measurement results (i.e. total capacitance divided by the electrode area) of several different period and pillar height combinations (left Y-axis). The triangles represent capacitor devices made from pillars with a 200 nm period, and the squares represent those with a 400 nm period. The measured capacitance density values showed the expected linear trend with pillar height. Comparing the 200 nm and 400 nm period values with the same pillar height of 800 nm and taking into account the different coaxial and pillar diameters in each case, the inverse relationship between the capacitance value and the square of the period was demonstrated. The factor increase in capacitance density of the pillar arrays over planar devices with the same oxide thickness is also plotted **Figure 7.3(a)** (right Y-axis).

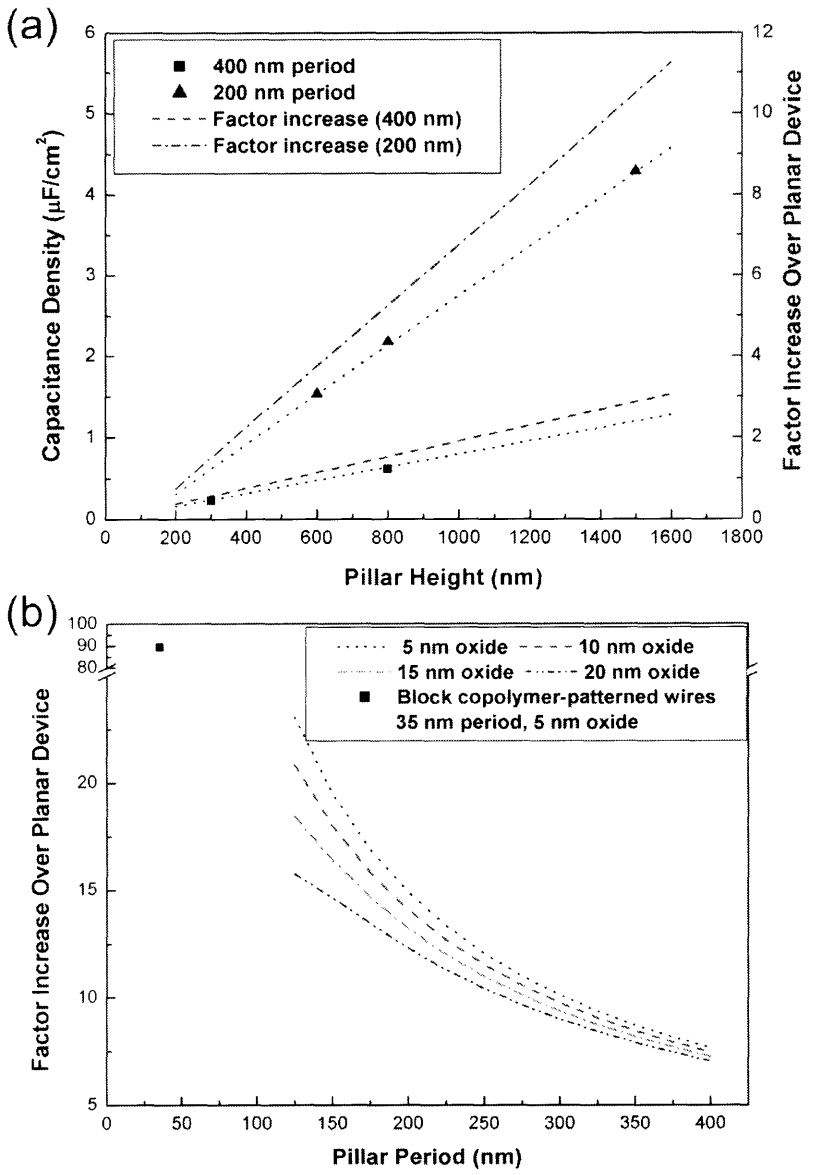

Figure 7.3 (a) Capacitance density measurements for two different periods, 400 nm (squares) and 200 nm (triangles), as a function of pillar height. The dotted lines show a linear fit to the experimental data and the dot-dash lines show the factor increase over planar devices with the same oxide thicknesses; (b) predicted capacitance density increase over planar devices for different pillar periods and oxide thicknesses. The diameter of oxidized pillars is assumed to be half of the period.

Figure 7.3(b) shows a plot of the predicted factor increase as a function of the pillar period based on **Equation [7.2]**. The oxidized pillar diameter is assumed to be half of the period in the calculation. A series of curves are plotted for different oxide thicknesses. As shown in the plot, the capacitance density increases with decreasing period; i.e. increasing pillar density. Higher densities than what can be obtained using the current interference lithography method can be achieved using self-assembly techniques. For instance, we have demonstrated the use of block copolymer (BCP) lithography in conjunction with metal assisted etching to fabricate dense arrays of high-aspect ratio silicon nanowires (55). Calculating the capacitance density based on the period and wire diameter we obtained using BCP lithography (approximately 35 nm and 20 nm, respectively), and assuming an oxide thickness of 5 nm, the expected factor increase in capacitance density over a planar device with the same oxide thickness is close to 90.

It is worth pointing out that in calculating the expected capacitance density values, the oxide thickness is assumed to be uniform along the entire length of the silicon nanopillars. However, as shown in **Figure 7.4**, transmission electron microscope (TEM) images revealed a thicker oxide near the tip of the pillars. This could be attributed to an enhanced oxidation rate near the tip where the surface is rough due to prolonged exposure to the HF-containing solution (92). Since the top of the pillar was exposed to the corrosive solution much longer, the effect was most pronounced in this region. As a consequence, the measured capacitance density

values are slightly lower than predicted values (based on **Equation [7.2]**).

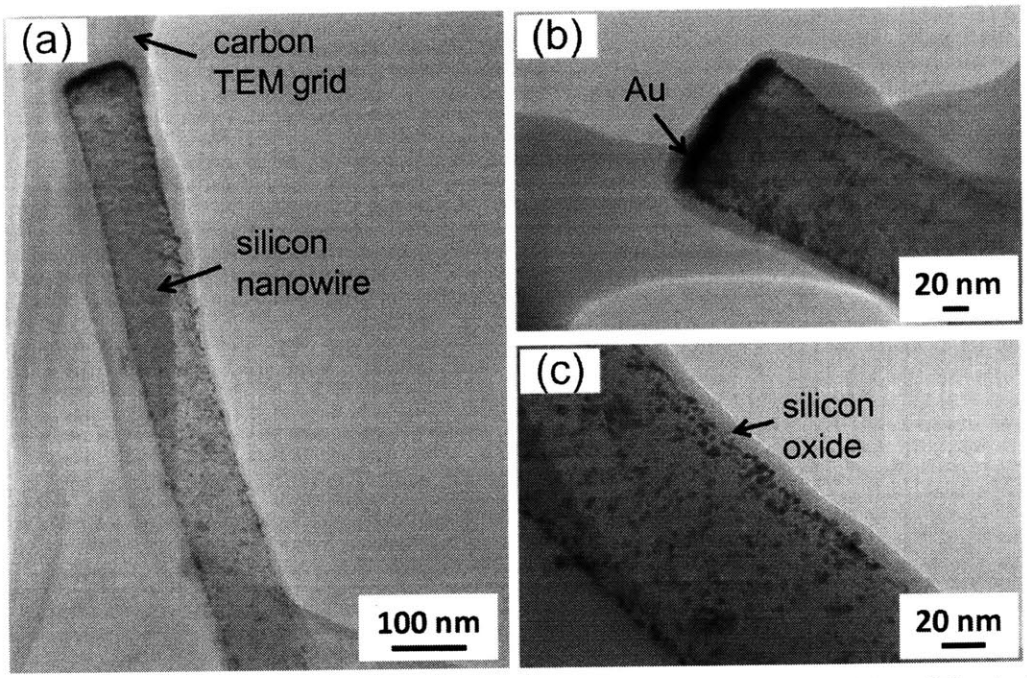

Figure 7.4 Tunneling electron microscopy (TEM) images showing (a) oxidized silicon nanopillars from a 200 nm period sample; (b) the tip of a single pillar with a thicker oxide layer; (c) a more uniform oxide thickness along the length of the pillar.

In addition to capacitance measurements, we also measured a leakage current of 1.15 x 10^{-5} A cm^{-2} at a bias of 2 V. This value is higher than what is generally measured with other capacitor structures (119) (121) (122). One possible reason for the discrepancy is oxide quality. Some dark spots are observed on the pillar surface from the TEM images in **Figure 7.4**. These spots could be Au residue from the pillar synthesis process. The presence of Au may have an effect during oxidation. Further studies are required to clarify the effect. Nevertheless, it is possible to remove any residual metal catalyst on the pillar surface and thereby improve the oxide quality by carrying out an additional cleaning step prior to thermal oxidation. For example, a quick aqua regia etch step could be used to remove the gold catalyst in place of the

commercially available iodine-based gold etchant that we currently use.

7.4 Summary

In summary, we fabricated a silicon nanopillar-based ultra capacitor array using metal-assisted etching and electrodeposition. The high aspect ratio made possible by the catalyzed etching provided for an increased effective electrode area. Electrodeposition made possible the deposition of a conformal metal layer over the high aspect ratio silicon nanostructure as the electrode. Capacitance measurements showed the expected trend as a function of pillar height and array period. Further improvements to increase the capacitance values can be made by optimizing the fabrication process and employing different metal catalyst patterning techniques to achieve a higher device density. The approach developed here for fabrication of silicon nanowire capacitors is simple and can be readily carried out in conjunction with other silicon microfabrication processes. With incorporation of known self-assembly based patterning to form nanowire arrays, capacitance increases of two orders of magnitude over plate capacitors with the same footprint should be achievable.

Chapter 8. Summary and Future Work

8.1 Summary

Since the first report over half a century ago, a significant amount of work has been directed towards obtaining an understanding of the fundamental formation mechanisms of porous silicon. Although the anodic etching of silicon remains the most extensively studied method for porous silicon fabrication due to its long history, electroless etching, and particularly metal-assisted etching, are quickly gaining interest as versatile and controllable methods for etching arbitrarily patterned structures, such as silicon nanopillars and nanowires.

The research described in this document was aimed at understanding, utilizing, and applying metal-assisted etching to controllably create silicon nanowires applicable in array-type devices. The electrochemical nature of the etching process was confirmed by carefully studying the etch rate dependence and silicon morphology as a function of the thickness and lateral dimensions of patterned catalyst films, as reported in Chapter 3.

In Chapter 5, the feasibility of catalytically etching to form ultra high aspect ratio silicon nanowires was demonstrated by combining metal assisted etching with block copolymer lithography. Since neither reactive ion etching of the catalyst metal nor direct lift-off using the block copolymer mask is practical, a new process involving a sacrificial silica pattern transfer layer was developed. In addition, by first assembling the block copolymer in topographic features, we demonstrated fabrication of silicon nanowire arrays at pre-defined locations with

pre-defined geometries. The versatility of this approach will facilitate broad use of such wire arrays in devices in which high densities, high surface-to-volume ratios, and accurate device placement are critical for optimum performance.

Studies of the effect of catalyst geometries in controlling the silicon morphology were described in Chapter 6. These were carried out through a systematic investigation of metal-catalyzed etching of both n- and p-type Si (100), (110), and (111) substrates using gold catalysts with three varying geometrical characteristics: isolated particles, metal meshes with small hole spacings, and metal meshes with large hole spacings. It was shown that for both isolated particles and metal meshes with small hole spacings, etching proceeds in the preferential <100> direction, whereas etching is confined to the direction normal to the substrate surface when a metal mesh with large hole spacings is used. Based on this new insight, we extended metal-assisted etching to create arrays of vertically-aligned polycrystalline and amorphous silicon nanowires from deposited silicon thin films. This allows exploitation of the etching process to fabricate functional silicon nanowire arrays using silicon films of any crystal structure deposited on any etch-compatible substrate. Since many nanowire-based applications such as batteries, capacitors, and sensors, do not require single crystal wires, this result is of practical importance as it enables the fabrication of silicon-nanowire-based devices in much more flexible and low-cost ways.

Finally, in Chapter 7, we demonstrated fabrication of a nanocapacitor device based on

silicon nanopillar arrays fabricated using metal-assisted etching and counter electrode fabrication using electrodeposition. Metal-assisted etching was used to create heavily doped silicon nanopillar arrays to serve as one electrode. The high aspect ratio achievable by the catalyzed etching technique helps increase the effective electrode surface area and hence the capacitance density. Electrodeposition was used to form a conformal metal layer over the silicon nanopillars as the opposing electrode. The fabrication approach is simple, low cost, compatible with current silicon technology, and easily scalable.

8.2 Future work

Through the work described in this thesis, we have demonstrated the feasibility of etching vertically-aligned arrays of high aspect ratio silicon nanostructures using metal assisted etching in conjunction with various metal catalyst patterning techniques. In Chapter 2 and 6, we carried out a systematic study of silicon etching as a function of different geometric characteristics of the catalyst, including both isolated pads and meshes. A systematic investigation of the etching behavior as a function of electrolyte composition and catalytic abilities of the metal catalysts were beyond the scope of this thesis. However, such a study would be very useful in terms of controlling the final silicon morphology by predicting the onset of different etching regimes for a particular metal catalyst in an electrolyte with a particular composition.

In Chapter 7, we demonstrated the fabrication of a silicon-nanopillar-array-based

capacitor device. We showed through experiments that the capacitance density trends with the geometric characteristics of the nanopillar arrays in a predictable and expected manner. We also showed in simple calculations that the capacitance density can be increased significantly via patterning techniques such as block copolymer lithography (discussed in **Chapter 5**). In future work, such a device should be evaluated for use in applications such as energy buffers. The integration of a nanocapacitor device in an energy harvesting system is schematically illustrated in **Figure 8.1**, where the nanocapacitor device serves a dual purpose of maintaining a stable power output and providing the peak load. Issues such as designing a process sequence that is compatible with the energy harvesting components, as the components may not be etch-resistant, and making contacts to both the energy source and actual device must be solved.

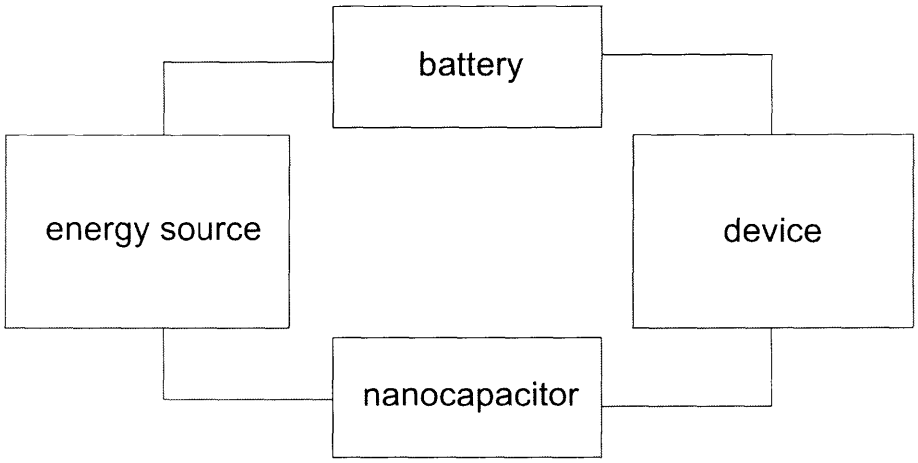

Figure 8.1 A schematic illustration of the integration of a nanocapacitor device in an energy harvesting system.

Finally, throughout the work described in this thesis we have demonstrated the versatility of metal-assisted etching in fabricating silicon nanostructures of all doping types and

concentrations as well as crystal structures with excellent control over the diameter, period, geometry, and placement. This makes silicon nanostructures fabricated using metal-assisted etching ideal candidates for array-type devices. In addition to the nanocapacitor work described in Chapter 7, other devices such as sensors could also benefit from the high surface-to-volume ratio of the silicon nanowires. For example, a field effect transistor (FET) type sensor device which is capable of detecting relatively small changes of electric charges can be fabricated by starting with an epitaxially-grown PNP or NPN silicon stack, as shown in **Figure 8.2**. The high sensitivity due to the small size of the nanowire is further enhanced by having a narrow gate region. Binding to the surface of the gate region can lead to depletion or accumulation of carriers. The gate potential and hence the measured current is determined by how much charge the to-be-detected chemical or biological species possess, and the density of coverage of the target molecule. Moreover, by combining metal-assisted etching with templated self assembly, we have shown that silicon nanowire arrays can be integrated into channels in one etching step. Such a structure can be useful for microfluidic-type sensor devices in which nanopillar-based sensor arrays are integrated into a set microchannels, allowing for controlled handling of small volumes of aqueous solutions on a planar chip, as well as detection of multiple different target molecules in a single microfluidic system.

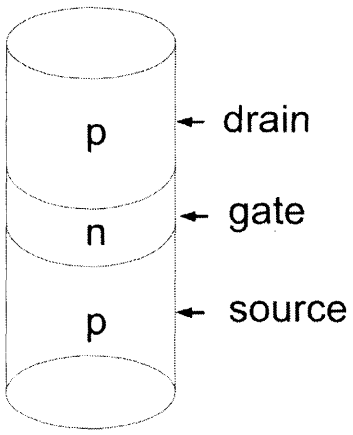

Figure 8.2 A silicon nanowire or pillar field-effect-transistor-based (FET-based) sensor element.

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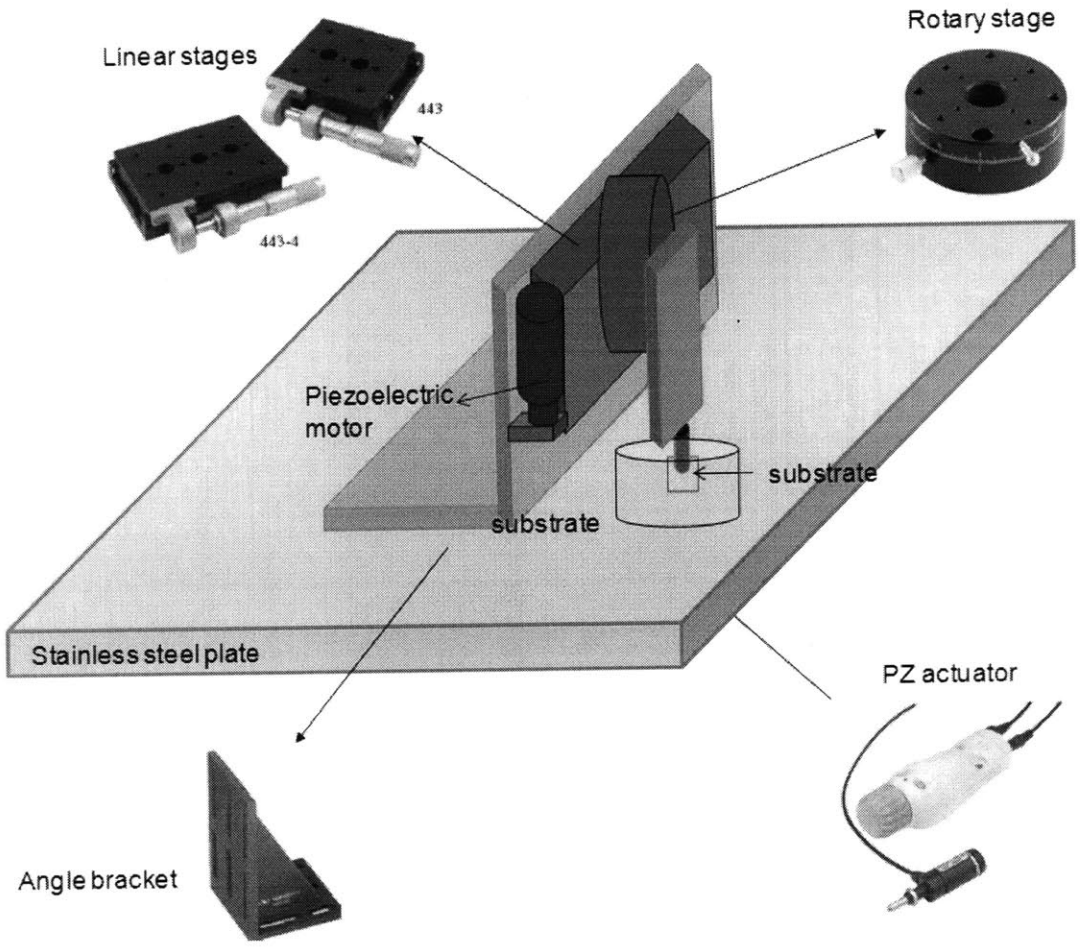
Appendix

A home-built dip-coater was used to coat polystyrene spheres for nanosphere lithography. A stainless steel bottom plate was used to minimize vibration during operation. A piezoelectric motor mounted on a linear stage was used to control the vertical motion of the coater. The angle of the substrate can be controlled using a rotary stage. The sample is mounted using a sample clamp screwed into a stainless steel plate mounted on the rotary stage. A schematic of the dip-coater is shown in the following figure.



The manufacturer and part number of each part is listed in the following table.

Parts	**Manufacturer**	**Parts #**
Rotary stages	Edmund Optics	NT55-040
Angle bracket	Newport	M360-90
Actuator kit (actuator/controller /power supply/cable)	Newport	PZC200-KT
Converter	Newport	NSC-485-232-I

The specifications of the piezo microstepping motor (PZA 12) are summarized in the following table.

Average Full-Step Size	Approx. 160 nm (16 micro-steps per full-step)
Travel Range	12.5 mm
Minimum Incremental Motion	0.3 μm
Maximum Speed	0.2 mm/s
Axial Load Capacity	50 N