LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

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Abstract

We have designed and fabricated a very low noise preamplifier and shaper to replace the existing ATLAS Liquid Argon readout for use at the Large Hadron Collider upgrade (sLHC). IBM's 8WL 130nm SiGe process was chosen for it's radiation tolerance, low noise bipolar NPN devices, wide voltage rand and potential use in other sLHC detector subsystems. Although the requirements for the final design can not be set at this time, the prototype was designed to accommodate a 16 bit dynamic range. This was accomplished by using a single stage, low noise, wide dynamic range preamp followed by a dual range shaper. The low noise of the preamp is made possible by the low base spreading resistance of the Silicon Germanium NPN bipolar transistors. The relatively high voltage rating of the NPN transistors is exploited to allow a gain of 650V/A in the preamplifier which eases the input voltage noise requirement on the shaper. Each shaper stage is designed as a cascaded differential operational amplifier doublet with a common mode operating point regulated by an internal feedback loop. Measurement of the fabricated circuits indicates their performance is consistent with the design specifications including the radiation tolerance targets.

I. Introduction

Although some components of the present Liquid Argon (LAr) electronics design may be adequate for use in SLHC the lack of spares and elimination of the processes that custom ASICs were designed in will mean that the complete ATLAS LAr electronics chain will need to be redesigned for operation at SLHC.

The ATLAS LAr Calorimeter is constructed of a series of cathode and anode plates submerged in liquid argon. Charged particles traversing it ionize argon atom electrons and create a current pulse on the positively charged anode that lasts for the 400ns electron drift time. The signal is conveyed to the front end electronics, located outside of the detector via a 5 meter, 25Ω cable. This part of the detector is expected to remain in the upgraded system [1]. The complete set of design goals for the upgraded detector await input from the operation of the current LAr system at high luminosity. For this work we assumed that the performance goals of the current LAr front end electronics would be sufficient with the added requirement that the front end electronics be able to withstand an exposure to 300kRad of ionizing radiation and 10^{13}n/cm^2 [2]. Table 1 summarizes the basic design goals.

Table 1 Design Goals for the upgraded LAr Front end electronics.

Dynamic Range	16 bits in 2 ranges
INL	0.1% within each range
ENI	75nA
Max Signal Current	5mA
Shaping Time Const. (RC)	15ns
Shaping Function	$(RC)^2$-CR
Ionizing Radiation Tol.	30kRad
Neutron Equivalent Dose	10^{13} n/cm^2

II. LAPAS Circuit Blocks

Figure 1 shows a block view of the LAr front end. The detector is modelled as a 1nF capacitance followed by a 25Ω transmission line, preamplifier and shaper. This work concerns the design of a prototype preamplifier and $(RC)^2$-CR shaper circuit on a single ASIC substrate. It is important to note that the shaping elements are constructed using the ASIC process passive components.

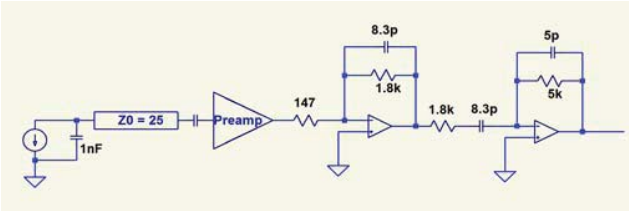

Figure 1 shows the Liquid Argon Front End Electronics blocks with detector modelled as a current source in parallel with a 1nf Capacitance followed by a transmission line and decoupling capacitor. The LAPAS ASIC contains the preamp and shaping sections shown to the right.

A. Technology

The wide dynamic range and associated low noise requirement for the preamplifier led to the selection of a bipolar technology. IBM's 8WL process that features Silicon Germanium (SiGe) bipolar transistors along with a wide selection of 130nm CMOS transistors was selected for this first prototype based on it's radiation hardness [3] low value of intrinsic base resistance and availability passive components with tightly controlled parametric spread. Figure 2 shows a Monte Carlo prediction of the output amplitude spread for the $(RC)^2$-CR shaper transfer function due to part to part passive component variation based on history of 50 runs of the 8WL process.

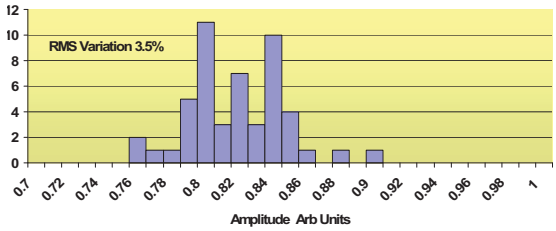

Figure 2 MonteCarlo simulation of the shaper output amplitude variation due to passive component variation based on the history of IBM's 8wl process runs.

B. Preamplifier Design

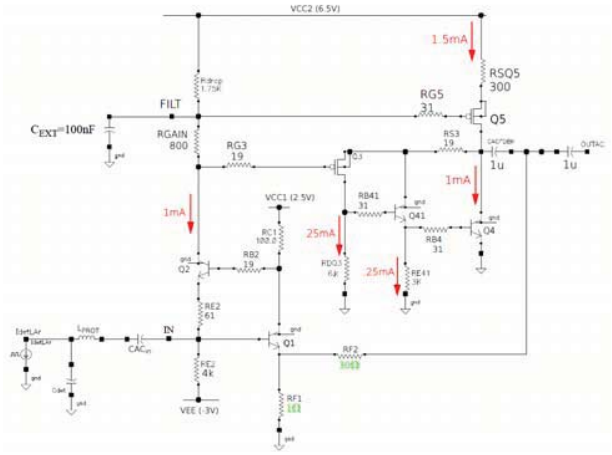

Figure 3 Super common base Preamp similar to that used in the ATLAS LAr Calorimeter. Note that the C1 and C2 are external components.

The schematic of the preamp is shown in Figure 3. It is based on the "super common base" architecture used on the presently installed in the LAr front-end boards described in previous publications [4],[5]. Thanks to the low spreading base resistance of the SiGe technology it employs an input transistor of manageable size (emitter length 4 x 20µm, 2 emitter stripe geometry) biased at 8mA collector current. Simulations predict that the preamplifier achieves good integral non-linearity (INL< 1%) and an overall equivalent series noise of ~0.26nV/√Hz, while dissipating 42mW.

C. Shaper Design

This design, in particular the shaping function benefits from earlier work done by the LAr group to optimize the tradeoffs between the relatively long LAr drift time and the high LHC interaction rates. In this design the shaper is AC coupled by an external capacitor to the preamp or other source. To help eliminate common mode pickup on and off the ASIC a two stage cascaded differential operational amplifier design has been employed (see Figure 4). All passive components except the four 100 Ω load resistors at ADC_A,B are fabricated on the ASIC. As shown in Figure 4 the first stage is used to accomplish some amplification and provide one of the two R-C integrations in the feedback loop. This stage is AC coupled to the second using a C-R differentiation. Placement of the differentiation here decouples the two stages allowing independent biasing of the second stage. The second RC integration is implemented in the feedback of this stage.

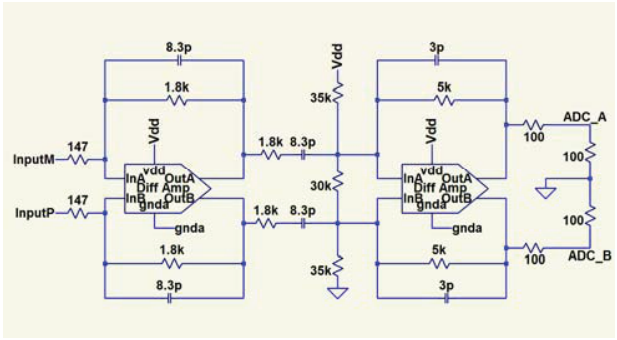

Figure 4 Shaper block schematic.

The amplifying element of the shaper design is a differential operational amplifier constructed using an operational transimpedance amplifier (OTA) gain block followed by a unity gain voltage amplifier. A simplified schematic of the OTA is shown in Figure 5. To maintain acceptable noise performance Q1 and Q2 are operated at a relatively high current density of 800µA each. Half of this current is removed by R1 and R2 before entering the OTA's mirror transistors U19 and U8. This allows lower power operation of only about 16mW for this stage. The supply voltage for the shaper is 5V in order to satisfy the wide dynamic range requirements. Although the SiGe NPN transistors can easily operate with this voltage across the base emitter junction, it was necessary to use thick gate CMOS devices in the current mirror structures. To achieve good matching the PMOS mirrors were cascoded (U4,U5,U6,U13,U16,U9). Intentional miller capacitance was introduced in the input stage to prevent the high bandwidth NPN transistors (*ft* ~ 60GHz) from introducing unwanted oscillations. In addition a fast feedback path across the outputs (OdfA and Odfb) was added.

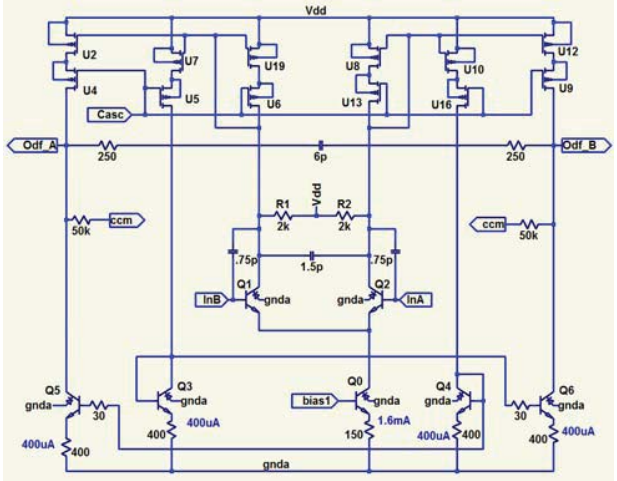

Figure 5 The OTA block of the differential operational amplifier.

A relatively low gain common mode amplifier (not shown) compares the voltage at node CCM with an internal reference to maintain a stable a DC operating point. The shaper realizes a CR-$(RC)^2$ transfer function where the product of each coupled R and C is 15ns. By selecting low valued resistors for the shaping in the high gain (10X) stage an equivalent input voltage noise of about 2.2nV/√Hz is achieved.

III. Layout and Fabrication

The prototype ASIC fabricated through MOSIS consists of four independently powered preamplifiers and two dual gain shaper stages on a 1.6 X 2.1mm die housed in a 9X9 mm open cavity QFN64 package. Packaged ASICS were received in March. The layout of the fabricated die is shown in Figure 6.

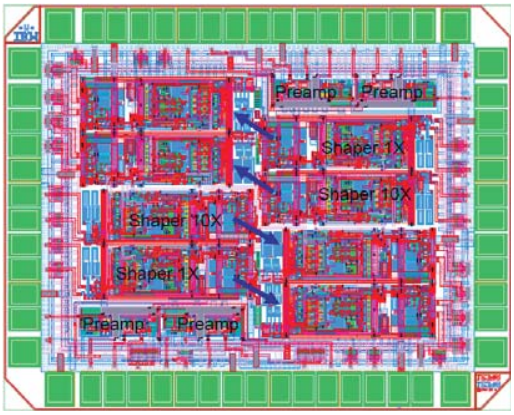

Figure 6 Layout of th LAPAS ASIC with 4 preamplifiers and two combination 1X, 10X shaper stages.

IV. Measurements

Measurement of the fabricated ASIC's show that all preamp and shaper circuits are functional with gain, shape and dynamic range close to that predicted by SPICE simulation of the extracted layout. Figure 7 shows the response of the preamplifier to an input waveform shaped to mimic the detector signal after the transmission line.

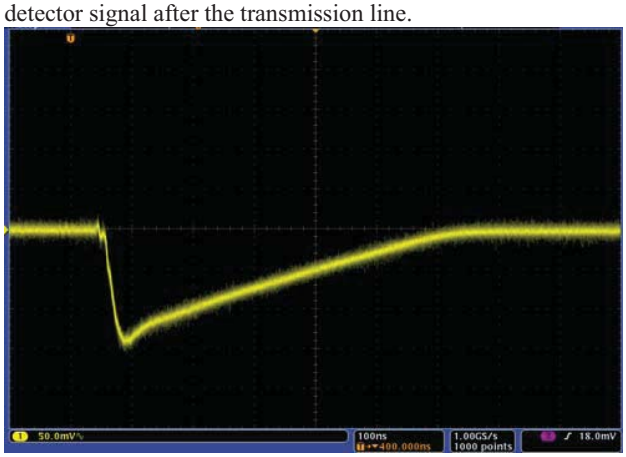

Figure 7 Measured Preamp response for a peak input current input of 250µA with an input rise of 20ns and fall time of 450ns.

The two traces in Figure 8 show the response of the shaper 1X and 10X outputs to the same preamplifier signal. The 14.1mV and 153mV peaks correspond to a nearly 10X difference in response.

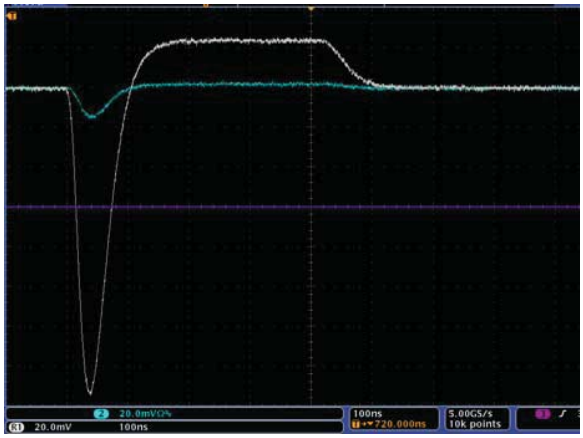

Figure 8 Measured response of both the 1X and 10X shaping amplifier inputs for a 20mV peak preamplifier output signal. The unusual signal shape reflects the differentiation of the triangular shaped preamp signal.

Figure 9 shows the measured Integral Non Linearity (INL) of the high gain stage. The high gain (10X) shaper output noise for this stage has been measured to be 130µV. This corresponds to an input referred current of 34nA well below the calculated 65nA equivalent input noise of the preamp.

Given the preamplifier gain of 650V/A and the full scale calorimeter input current of 5mA the preamplifier output will be slightly larger than 3V. This range is covered by the 1X stage that is linear for inputs up to 4V while the high gain (10X) stage covers the range between 0 and 300mV. Both shaper stages exhibit a highly linear response with an INL of less than 0.1%.

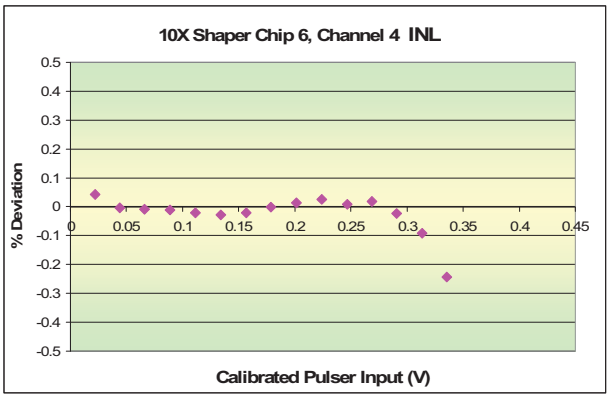

Figure 9 Measured Integral Non Linearity of the high gain shaper stage. The maximum deviation over the 300mV dynamic range is 0.05%. At 450mV the deviation (not shown) is 2%.

We have characterized 18 prototype ASICs and find the part to part gain variation is less than 3% except for one failed ASIC. Figure 10 shows the 1X shaper amplitude distribution for 17 of 18 chips with an input of 165mV. The RMS deviation is 1.8mV reflecting a 2% variation among channels, well within the measurement error of our socketed test equipment.

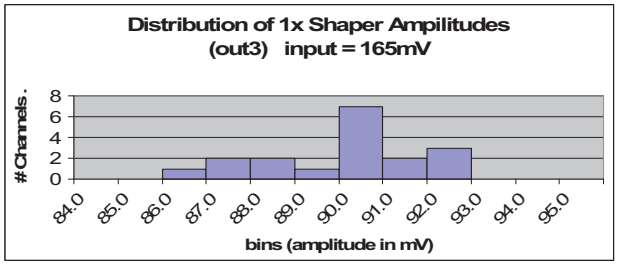

Figure 10 Distribution of amplitudes among 17 ASIC's for a 165mV preamp input signal. The RMS deviation is 1.8mV.

V. Preliminary Radiation Studies

Three ASICs were exposed to ionization doses of 200, 500 and 1000krad in three steps. The chips were exposed at Brookhaven National Laboratory's Gamma Irradiation Facility then measured and returned for additional exposure. Our measurements indicate no significant change in linearity and little or no change in gain (See Figure 11) to within the sensitivity of our test apparatus. A small increase in gain was observed with the 500krad data but this change is consistent with what we might expect due to a change in equipment

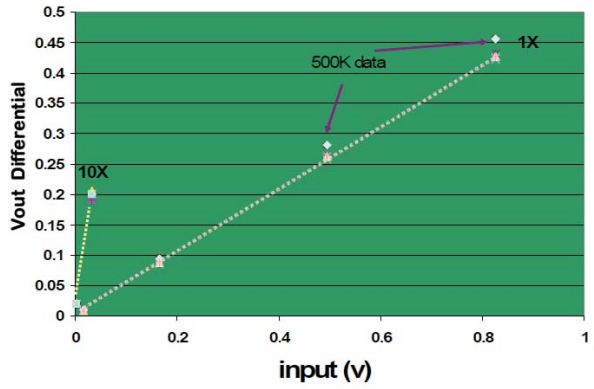

Figure 11 The plot above shows output amplitude measurements of Chip 8 after 0, 200, 500 and 1000krad exposure to ionizing radiation at the BNL Gamma Irradiation Facility.

status over a the several week period between measurements in rise time or amplitude of the pulser and charge injector inputs. Further measurements will be performed to understand to validate these results.

VI. Results and Conclusions

We have designed, fabricated and tested a first prototype of the ATLAS LAr front end electronics for the upgraded detector. Measurements with a socketed test board have confirmed many of the design objectives. Our future plans include continued testing with a LAPAS ASIC assembled on a printed circuit board for improved testability of the preamplifier. These tests will naturally lead to inclusion of the LAPAS into a more complete readout chain. The IBM 8WL technology appears to be robust in both it's performance and radiation tolerance for use in the upgraded LAr detector.

VII. References

[1] F. Gianotti et al., "Physics potential and experimental challenges of the LHC luminosity upgrade", Europ. Phys. J. Vol. C, no. 39, pp. 293-333, 2005.

[2] ATLAS Radiation Task Force predicted radiation levels, ATL-GEN-2005-001

[3] J.D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," Proc. IEEE., vol. 93, pp. 1559 – 1582, 2005.

[4] R. L. Chase and S. Rescia "A linear low power remote preamplifier for the ATLAS liquid argon EM calorimeter." IEEE Trans. Nucl. Sci., 44:1028, 1997.

[5] R.L. Chase et al., "Transmission Line Connections Between Detector and Front End Electronics in Liquid Argon Calorimetry", Nucl. Instrum. Meth. A 330 (1993) 228.