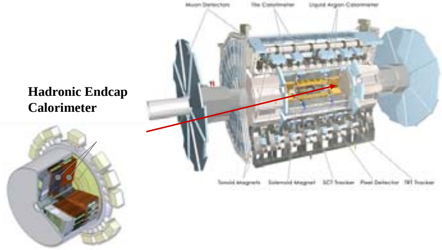

Upgrade of the Cold Electronics of the ATLAS HEC Calorimeter for sLHC

Generic Studies of Radiation Hardness and Temperature Dependence

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Hadronic End-cap Calorimeter (HEC) at the Large Hadron Collider (LHC)

HEC Wheel on assembly stand

3 HEC Modules interconnected

LHC up to 2016:
- Located at CERN (Geneva, Switzerland)
- Ring with 27 km circumference
- proton-proton collisions at 40 MHz
- 14 TeV center-of-mass energy
- 10^{34} cm^{-2} s^{-1} instantaneous luminosity

super-LHC (sLHC) from 2016:
- Upgrade of accelerator and experiments
- 10^{35} cm^{-2} s^{-1} instantaneous luminosity
- 10 times higher radiation background
- new readout system foreseen for LAr

HEC
- $1.5 < |\eta| < 3.2$
- 2 End-cap cryostats with 2 wheels each
- 32 modules per wheel
- 5236 readout channels

Radiation Hardness for HEC

For 10 years at sLHC (=10^{35} cm^{-2} s^{-1})
Neutrons 1.5 * 10^{15} n / cm^2
Photons 50 kGy
Protons 1.2 * 10^{12} p / cm^2

Cold Electronics of the ATLAS HEC Calorimeter
- Signal amplification and summation electronics operated in liquid argon (LAr) at circumference of HEC wheels inside the cryostats.
- Present electronics designed for operation at irradiation levels expected for the LHC.
- Irradiation levels at sLHC expected factor 10 higher than at LHC: New amplifier system.
- Presently investigation of technological possibilities:

Emphasis on operation at LAr temperatures (~87 K) and under high irradiation.

Technology Overview

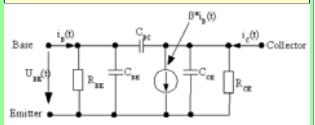
Material	SiGe			Si			GaAs	
Transistor	Bipolar HBT			CMOS FET			pHEMT (FET)	
Foundry	IHP	IBM		AMS	AMS	IHP		Triquint	Sirenza
Process	SGB25V 250nm	8WLBiCMOS 130nm: HB Break down voltage 4.7V	8WLBiCMOS 130nm: MB Break down voltage 3.4V	BiCMOS 350nm	BiCMOS 350nm	SGB25V 250nm		CFH800 250nm	250nm
Type	npn	npn	npn	npn	nmos	nmos	pmos	pHEMT	pHEMT
Emitter area (µm²)	0.84* 0.42	0.12* 1*2	0.12* 1*2	24	10*0.35	350* 0.24	350* 0.24	800*0.4	600*0.5
		0.12* 12*2	0.12* 12*2	48		750* 0.24	750* 0.24		300*0.25
		0.12* 3*4	0.12* 3*4	96					
		0.12* 8*1	0.12* 8*1						
		0.12* 16*6	0.12* 16*6						

HB: High break down
MB: Medium break down
HBT: Hetero Bipolar Transistor
pHEMT: p high electron mobility transistor

RF measurement of device parameters

- Measured in frequency domain (Amplitude, Phase)
- Measurement of reflected & incident voltages with a reference impedance (50Ω system)
- Advantage: current measurements are not necessary
- Disadvantage: Calibration has to be done
- Transformable to other parameter sets (h, Z, Y, …)

Example: Bipolar transistor



Small signal circuit model

Definition of S-Parameter

Two-Port Network schematic

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+}, \quad S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+} \Big|_{a_2=0} \qquad S_{12} = \frac{b_1}{a_2} = \frac{V_1^-}{V_2^+}, \quad S_{22} = \frac{b_2}{a_2} = \frac{V_2^-}{V_2^+} \Big|_{a_1=0}$$

Definition of Voltage Transfer-function (Gain)

$$tf = \frac{V_l}{V_s} = \frac{S_{21}(1+\Gamma_l)(1-\Gamma_s)}{2(1-S_{22}\Gamma_l)(1-\Gamma_{in}\Gamma_s)}$$

with

$$\Gamma_l = \frac{Z_l - Z_o}{Z_l + Z_o} := 1$$

$$\Gamma_s = \frac{Z_s - Z_o}{Z_s + Z_o} := -1$$

$$\Gamma_{in} = S_{11} + \left(S_{12}S_{21}\frac{\Gamma_l}{(1-S_{22}\Gamma_l)} \right)$$

Short circuit input admittance

$$\frac{1}{R_{BE}} + j\omega(C_{BE} + C_{BC}) = \frac{1}{Z_0}\frac{1 - S_{11} + S_{22} - \Delta S}{1 + S_{11} + S_{22} + \Delta S}$$

Current transfer function (current gain)

$$\beta = \frac{-2S_{21}}{1 - S_{11} + S_{22} - \Delta S} \quad \text{with: } \beta\left(1 + j\frac{f}{fg}\right) \sim \beta_0$$

feedback admittance

$$-j\omega C_{BC} = \frac{1}{Z_0}\frac{-2S_{12}}{1 + S_{11} + S_{22} + \Delta S}$$

fg : upper frequency limit
ß0 : DC current gain measure for small f

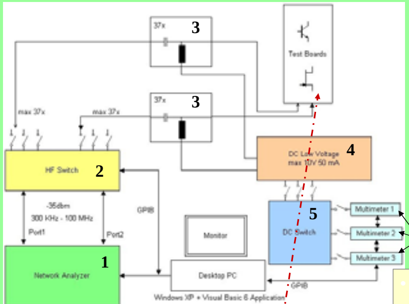
Short circuit output admittance

$$\frac{1}{R_{CE}} + j\omega(C_{BC} + C_{CE}) = \frac{1}{Z_0}\frac{(1 + S_{11} - S_{22} - \Delta S)}{(1 + S_{11} + S_{22} + \Delta S)}$$

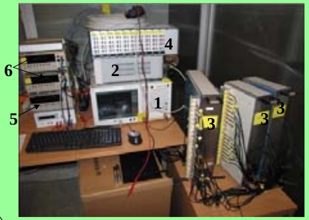
With: $Z_0 = 50\Omega$ $\quad \Delta S = S_{11}S_{22} - S_{12}S_{21}$

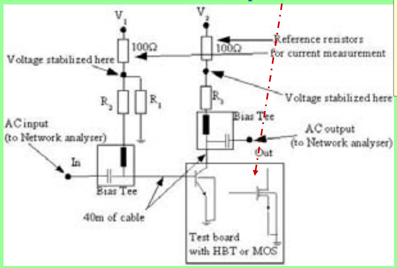
What we gain from S-Parameter measurements:
- Interesting (critical) parameters: Input impedance, gain, output impedance;
- Full characterization in frequency-domain
- Due to Calibration, „40m" long distance-measurement is possible -> „live"-measurement under radiation

S-Parameter Measurement Setup



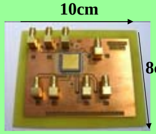
S-Parameter measurement setup





Circuitry for transistor measurement

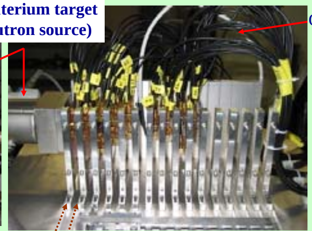
Testing up to 37 devices (transistors)
- Measuring DC-values and S-parameters
- Measurement during neutron irradiation
- Frequency Range: 300kHz – 100MHz



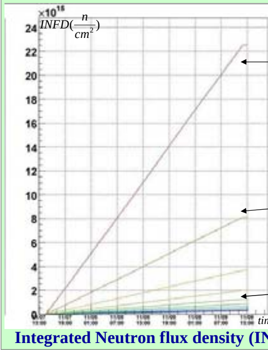
Test Board for 4 transistors

Neutron Irradiation Setup

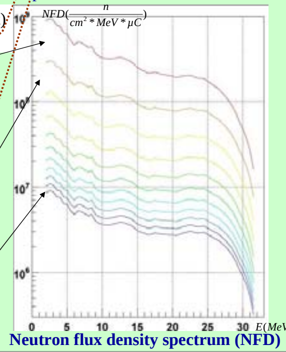
Setup in Cyclotron Hall at Rez



Up to 11 boards with devices

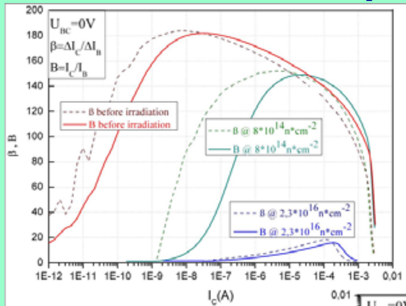


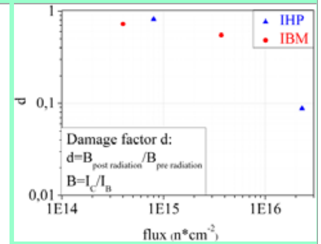
Integrated Neutron flux density (INFD)



Neutron flux density spectrum (NFD)

SiGe HBT– Gummel Plots - Impact of Neutron Irradiation

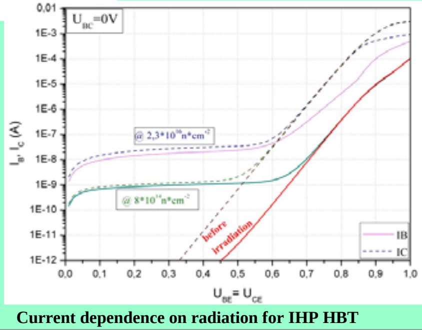




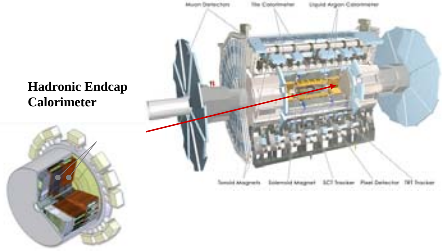
Damage factor for different transistors
U_{BE} is chosen at maximum of B

Loss of current gain due to irradiation for different IHP transistors of same size

- ⇒The transistors are measured before and after irradiation;
- ⇒ Radiation levels correspond to slot position of the board in the beam;
- ⇒ I_B,I_C increases with radiation for low U_{BE}
- ⇒Small variations in the damage factor for transistors of several sizes & fabrication foundries indicate that present SiGe technologies are quite robust against neutron irradiation up to 2*10^{15}n*cm^{-2}.



Current dependence on radiation for IHP HBT



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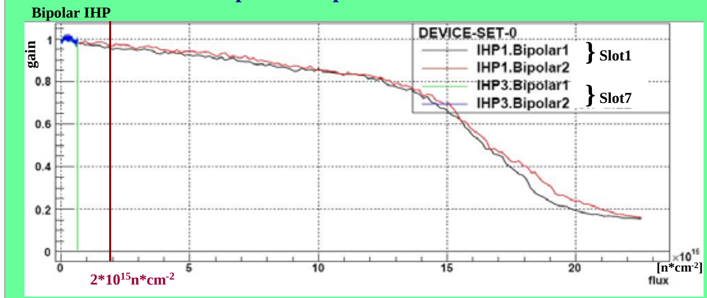
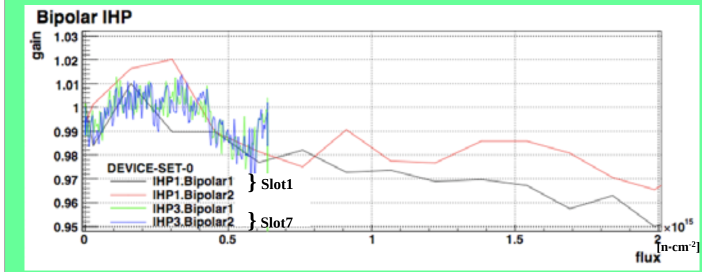
Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)

SiGe Bipolar – Impact of Neutron Irradiation

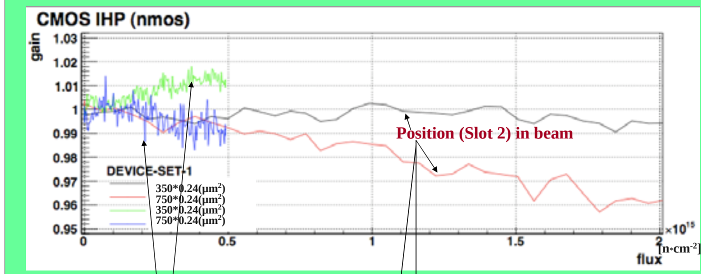


Loss of Gain @ 40MHz up to $2{,}3*10^{16}n*cm^{-2}$ for 2 equal transistors of IHP as example

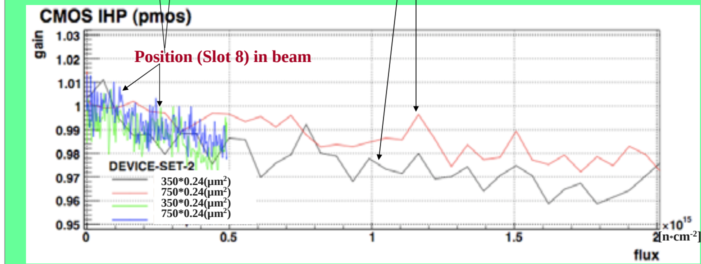


Loss of gain @ 40MHz over irradiation for 2 equal transistors up to $2{,}3*10^{16}n*cm^{-2}$

Si MOS FET – Impact of Neutron Irradiation

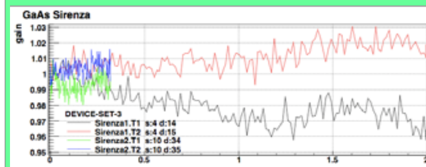


Loss of gain @ 40MHz during irradiation for IHP nmos transistors as example



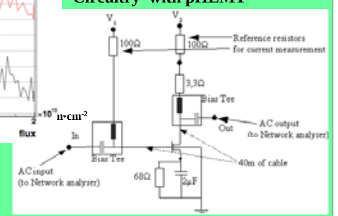
Loss of gain @ 40MHz during irradiation for IHP pmos transistors as example

GaAs pHEMT– Impact of Neutron Irradiation



Gain change @ 40MHz during irradiation

Circuitry with pHEMT



Remark for all pHEMT GaAs: Measuring with the same circuitry as for MOS or HBT devices, an immediate gain drop under irradiation can be observed. To avoid this, see circuitry above.

All Technologies – Impact of Neutron Irradiation

Material	SiGe				Si			GaAs	
Transistor	Bipolar HBT				CMOS FET			FET	
Foundry	IHP	IBM MB	IBM HB	AMS	IHP		AMS	Triquint	Sirenza
Type	npn	npn		npn	nmos	pmos	nmos	pHEMT	
Gain change@ $2*10^{15}n*cm^{-2}$	3%	2%	2%	5%	2%	3%	3%	2% $1.2*10^{15}$	2%
Gain change@ Max.rad.($n*cm^{-2}$)	75% $2.2*10^{16}$	11% (3.6	20% 7.8)$*10^{15}$	55% $2.3*10^{16}$	8% $8*10^{15}$	11% $8*10^{15}$	22% $2.3*10^{16}$	2% $1.2*10^{15}$	2% $2*10^{15}$

All values @ 40 MHz

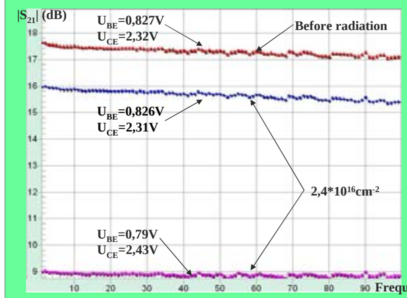
SiGe –Bipolar AMS Transistors: DC Operation Point – Voltage Correction after Radiation

AMS Transistor A	Irradiation ($n*cm^{-2}$)	U_{BE} (V)	I_B (µA)	U_{CE} (V)	I_C (mA)	ß	$\|S_{21}\|$ (dB) @ 40MHz	Change In $\|S_{21}\|$
24µm²	0	0,827	6,64	2,32	2,59	390	17,4	100%
	$2{,}4*10^{16}$	0,790	47,9	2,43	0,91	19	8,9	51%
	$2{,}4*10^{16}$	0,826	112,8	2,31	2,72	24	15,7	90%

@ $2{,}4*10^{16}n*cm^{-2}$ change of U_{BE} is significant; for stabile $|S_{21}|$ a correction is necessary

AMS Transistor B	Irradiation ($n*cm^{-2}$)	U_{BE} (V)	I_B (µA)	U_{CE} (V)	I_C (mA)	ß	$\|S_{21}\|$ (dB) @ 40MHz	Change In $\|S_{21}\|$
24µm²	0	0,828	8,29	2,33	2,56	309	17,4	100%
	$3{,}5*10^{15}$	0,82	16,9	2,34	2,4	142	16,5	95%
	$3{,}5*10^{15}$	0,829	24,2	2,28	3,22	133	18,3	105%

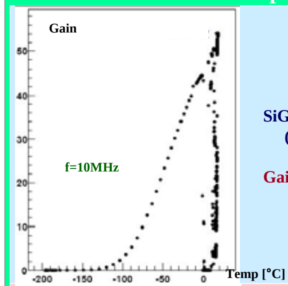
@ $3{,}5*10^{15}n*cm^{-2}$ (approximately required) , for stabile $|S_{21}|$ no correction needs to be done!



AMS transistor A (24µm² emitter area) for different DC operation points & irradiation levels

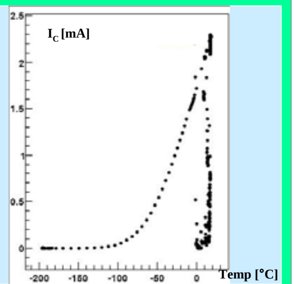
Voltage level of U_{BE} is adjusted after irradiation.
- Level of I_C is approximately similar to the beginning of irradiation
- I_B is much higher after irradiation
- ß is significant smaller (see Fig. Loss of current gain during irradiation)
- $|S_{21}|$ is nearly the same
- Radiation effects can be reduced by operation point stabilization.

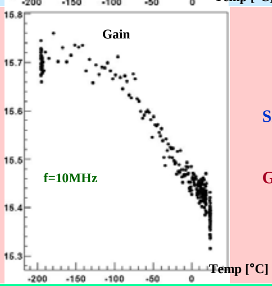
Temperature Dependence



SiGe IHP npn HBT (as example)

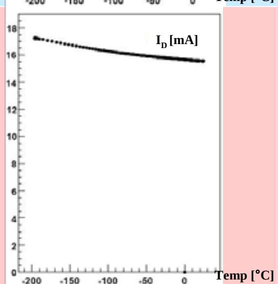
Gain change 100%





Si IHP N-MOS FET (as example)

Gain change 2%



- The operation point for HBT and MOS is set with voltages;
- Setting voltages leads to a stabile gain in liquid nitrogen for MOS transistors, but not for HBTs .

SUMMARY

Radiation test results:
- Loss of current gain of at most 6% have been measured for all technologies tested up to the required irradiation level of $2*10^{15}$ n/cm² All devices tested are radiation hard.
- A change of the operation point with irradiation is observed for some technologies, in particular for the AMS bipolar devices. A stabilization might be necessary.
- The operation points of the MOS FETs tested are stable under irradiation. Stabilization is not necessary for losses due to irradiation.

Temperature results
- Gain and operation points of the MOS FETs tested are stable within the required limits of the specifications over a temperature range from room temperature to LAr temperature.
- Large gain variations are observed for all bipolar devices tested over a temperature range from room temperature to LAr temperature. A change of the bias point is necessary for operation at LAr temperature.

OUTLOOK

- The IC architecture for sLHC will remain the same as for LHC:
- The basic element of the cold HEC electronics is an integrated chip consisting of eight preamplifiers and two summing amplifiers.
- The concept of 'active pads' is employed: each preamplifier is connected to one pad of the calorimeter cells, the individual signals being amplified.
- The read-out channels are formed by summing signals from 2 / 4 / 8 or 16 pads to the required output granularity with subsequent amplification. This concept results in an optimal signal to noise ratio.
- Next steps: Measurement of transistor behaviour in cold, choice of technology, design of amplifier stages as well as tests of the design criteria:
- IC power consumption should not exceed 200 mW in order to avoid boiling of LAr
- Gain difference between individual preamplifier channels of one IC has to stay below 1%
- Gain difference of a read-out channel between warm and cold not be more than a factor of two
- Noise level should not exceed the present low level
- Dynamic range of the preamplifier has to be 12-bit, that of the summing amplifier 13-bit
- IC has to be safe with respect to potential HV discharges in the gaps of the HEC