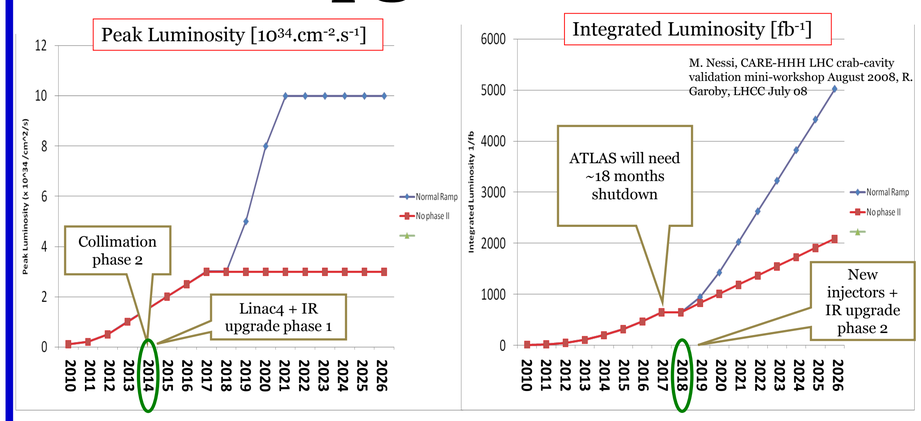
# Digital Architecture of the New ATLAS Pixel Chip FE-I4

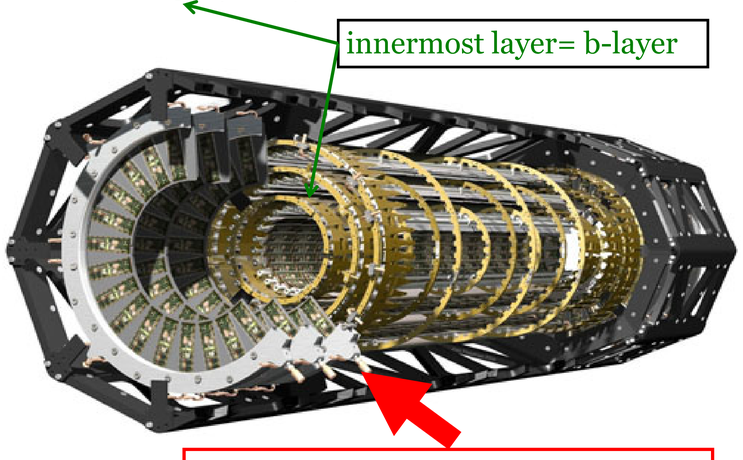
## ATLAS Upgrades Timeline



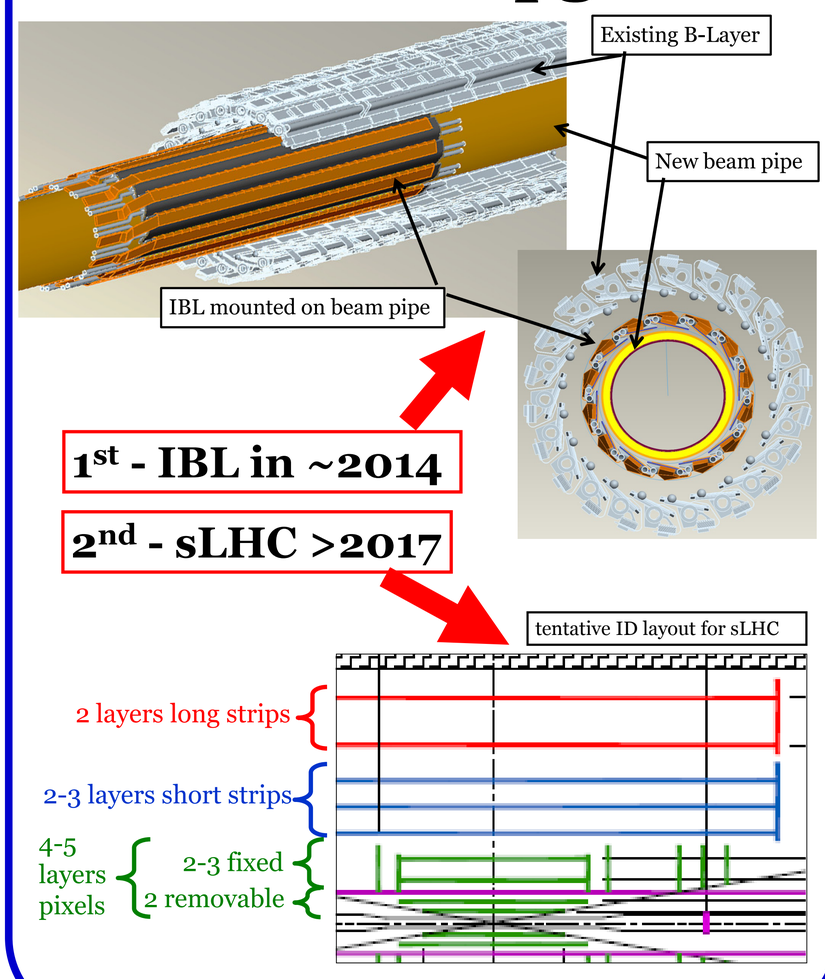

**GOALS OF UPGRADE:**
- ATLAS phase-I upgrade: record 550 fb⁻¹ & cope with ~75 pile-up events each BC.
- ATLAS phase-II upgrade: 10 times peak luminosity (up to ~400 pile-up events each BC).

## ATLAS Pixel Detector

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm



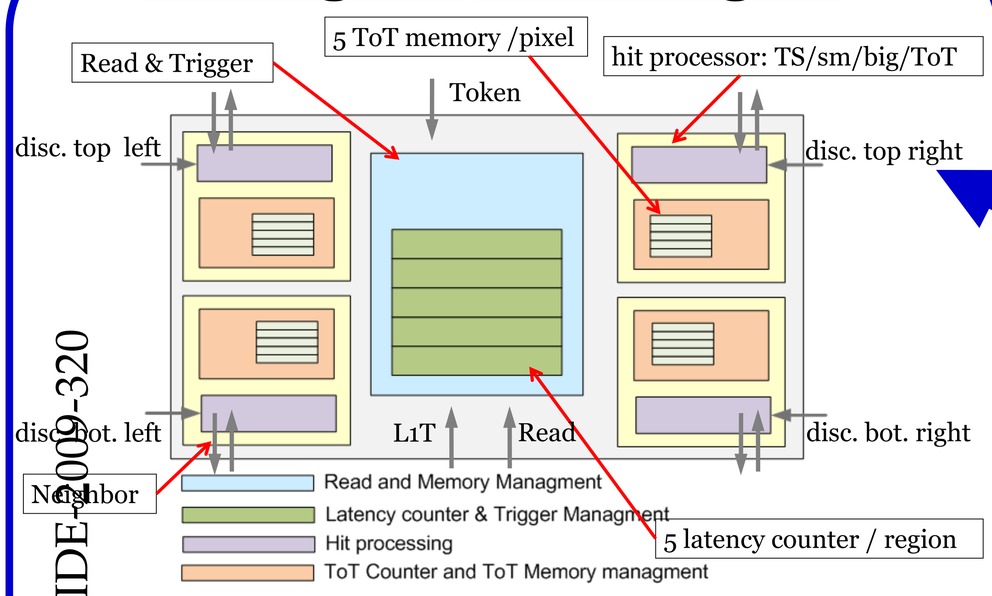

## ATLAS Pixel Upgrades




## FE-I4, ATLAS Pixel FE for Higher Luminosity

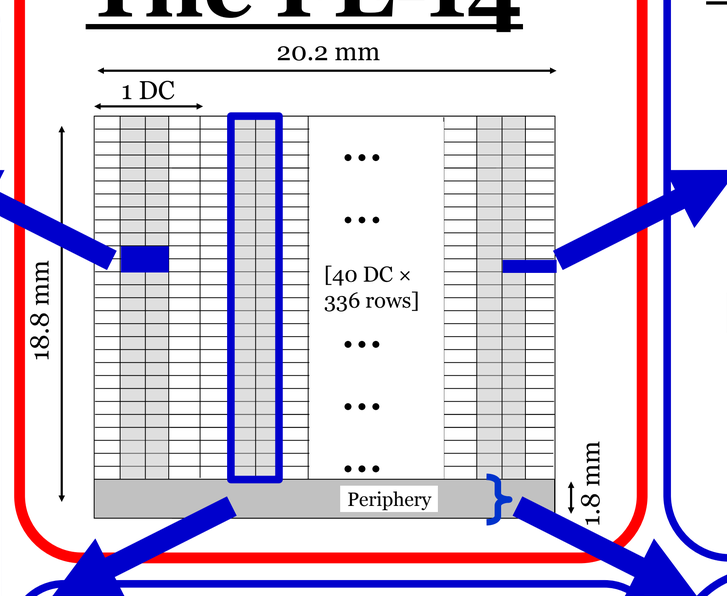
- Targets IBL & outer layers sLHC: Good fit for both projects (radiation environment, hit rate, schedule).
- Technology: 130nm. Integration of more digital functionalities, high radiation tolerance (no enclosed layout needed).
- Geometry: 336 by 80 pixel array, 50 by 250 μm² pixels, overall ~20.2 by 18.8 mm² FE → highest in HEP to date.
- Powering: Analog I~80 mA/cm², V=1.4 V; Digital I~80 mA/cm², V=1.2 V. Compatible w. Serial Powering & DC-DC.
- Data Output Block: On-chip PLL, 8b10b coder, pseudo-LVDS output → BW: 160Mb/s DC-balanced data streaming.

## The Digital 4-Pixel Region

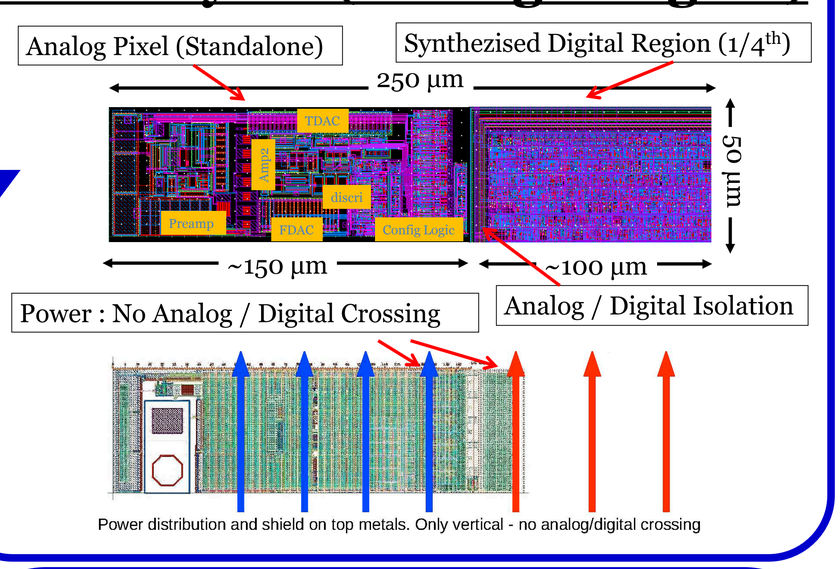



- 4 Pixels digitally tied together: Common Read / Memory / Trigger management units, Latency Counters (5 per 4-pixel region) → Saves power & area, gains efficiency. New functionality available: time-walk-less recording of small hits.
- Single-pixel functionalities: Hit processing (Time Stamping, digital discrimination, ToT), 5 ToT memories / pixel.

## The FE-I4



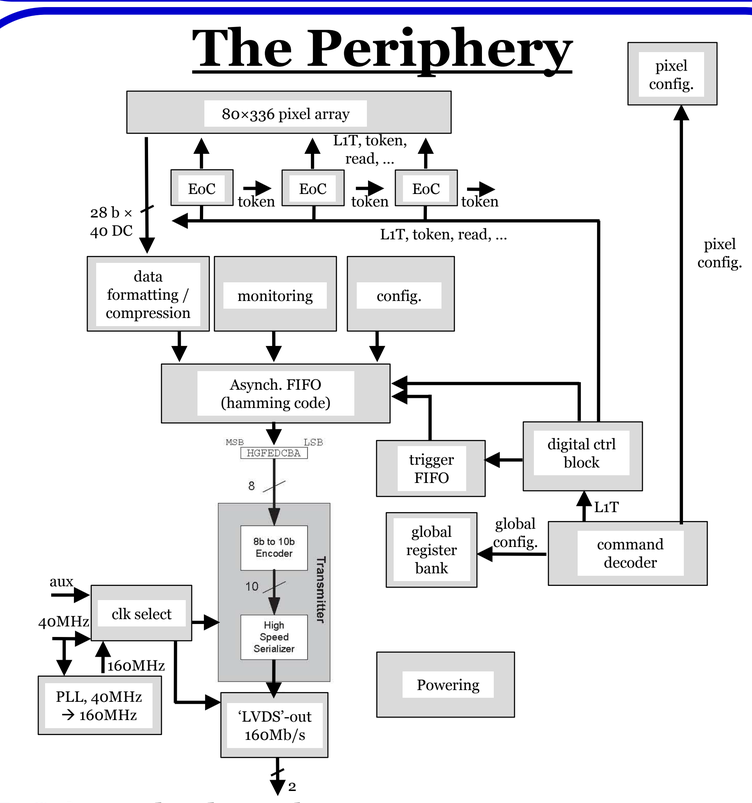

## Pixel Layout (Analog + Digital)




## Digital Double-Column

An 8 times 21-region structure with:
- → Skew compensated clock routing.
- → Buffering scheme for read signals.
- →Triple redundant read token + Majority voting.
- → Hamming coded pixel data and address (thermal encoder for yield optimization).
- → Redundant configuration register.
- → An efficient power routing scheme.

## The Periphery




## Conclusion

- FE-I4 is the new ATLAS Pixel FE for IBL & outer layers of sLHC.
- Digital architecture in 130nm allows high level of integration; radiation-hard.
- Regional architecture, tuned to demanding environment: efficient, low power, with new functionalities.
- Periphery assures compatibility to current pixel detector and allows pursuing innovative concepts.

- **Target: full size FE-I4 by end 2009.**

EoC → 3-redundant token.
Data formatting → 8b format & data compression.
Readout FIFO → Storage.
Digital Control Block → Controls pixel hits readout.
Command Decoder → Configuration, resets & L1T.
Data Output Block: 8b10b encoder, PLL serializer & pseudo-LVDS output → Use 40MHz bunch-crossing clock, compatible with current pixel detector, 160 Mb/s data output for IBL.
Powering → DC-DC & Serial Powering supported.

## Digital Pixel Performances

**Regional Buffer Overflow**

| Memory Depth | Simulation | | Analytical | |
|---|---|---|---|---|
| | IBL | 10xLHC | IBL | 10xLHC |
| 5 | 0.047% | 2.19% | 0.029% | 2.25% |
| 6 | 0.01% | 0.65% | 0.003% | 0.57% |
| 7 | <0.01% | 0.16% | <0.01% | 0.13% |

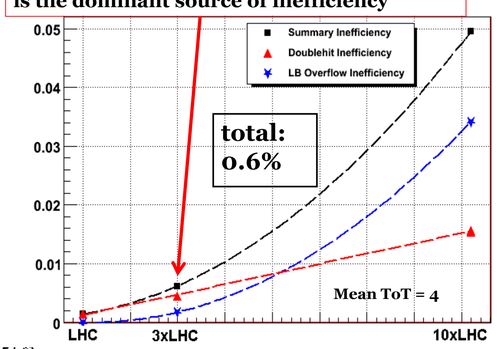
Average for 4-pixel region. IBL occupancy

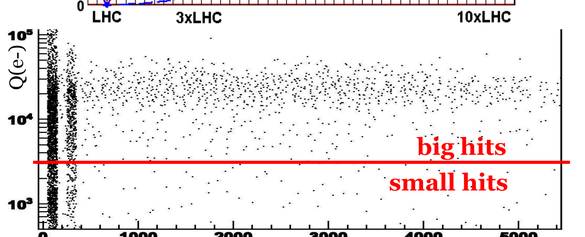
| Simulation type | Power (avg) [uW] |
|---|---|
| type 1 | 42.28 |
| type 2 | 25.19 |
| type 3 | 24.69 |
| type 4 | 24.73 |
| type 5 | 35.12 |
| type 6 | 27.64 |
| type 7 | 30.98 |

@1.2V

**Digital power at IBL occupancy below 10μW/ pixel (simulation)**

**@ IBL rate, analog pixel pile-up inefficiency is the dominant source of inefficiency**




**Spatial association of small hits well tuned to clustered nature of real hits!**

- **Performances:**
- Efficient (~0.6%).
- Low power (< 10 μW / pixel).
- Optimized for real physics hits.

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