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A 40MHz Trigger-free Readout Architecture for the LHCb experiment at CERN

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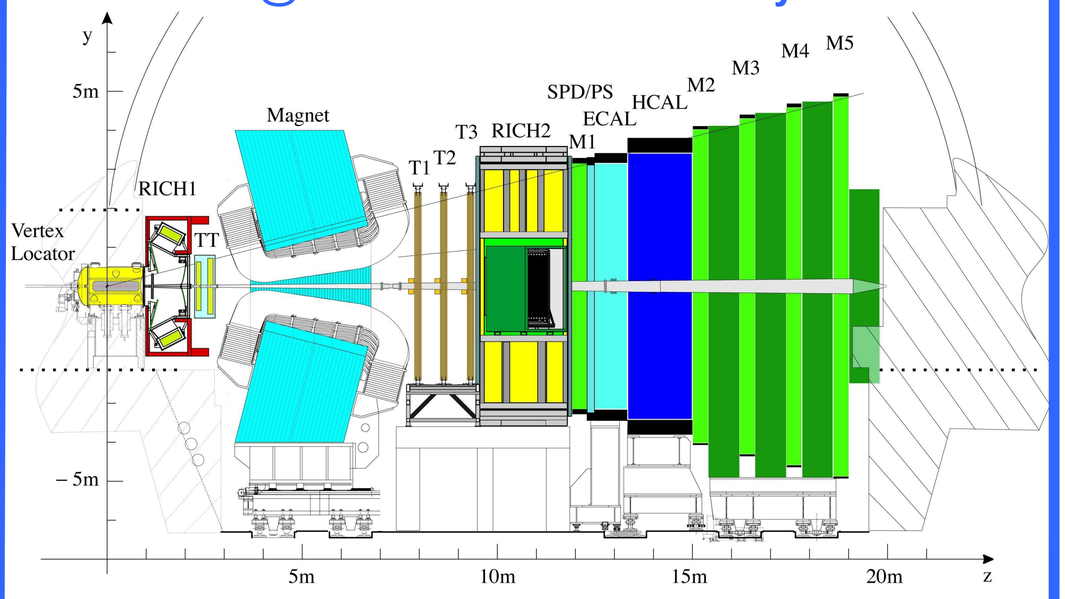
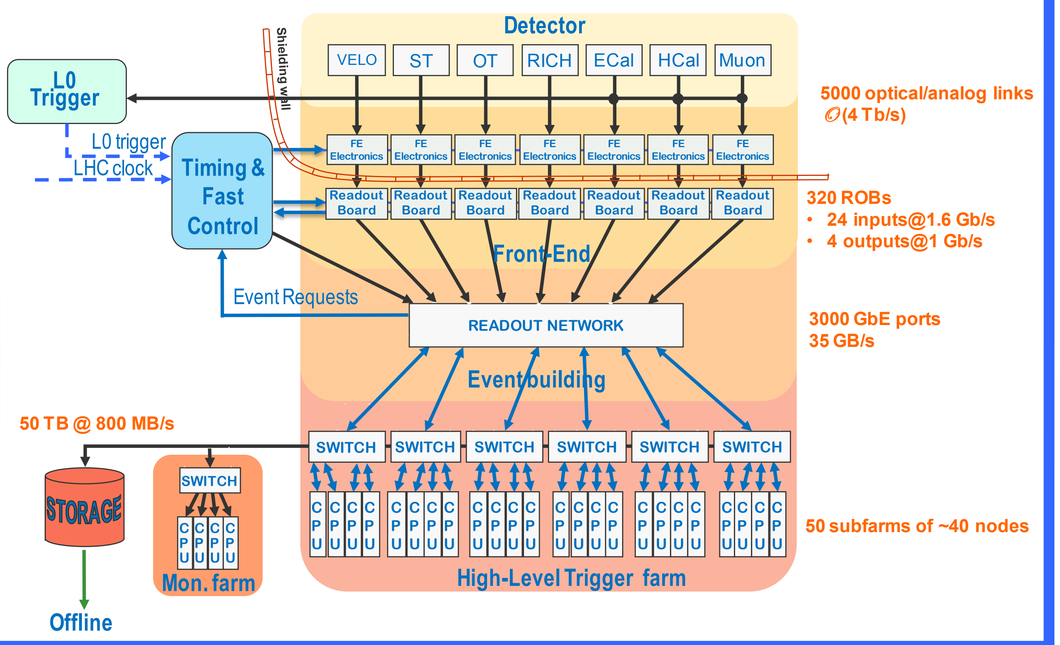
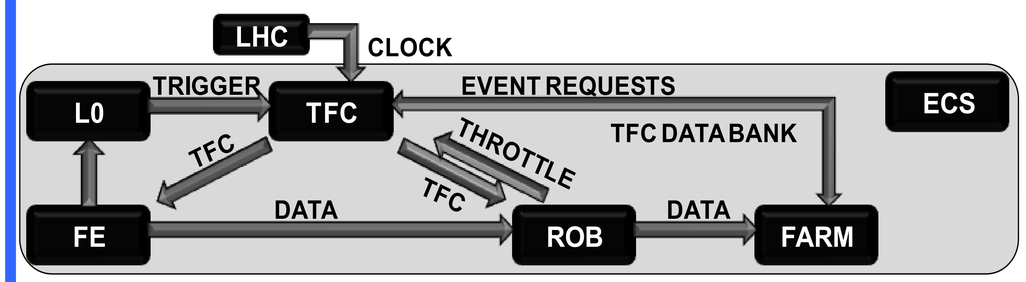
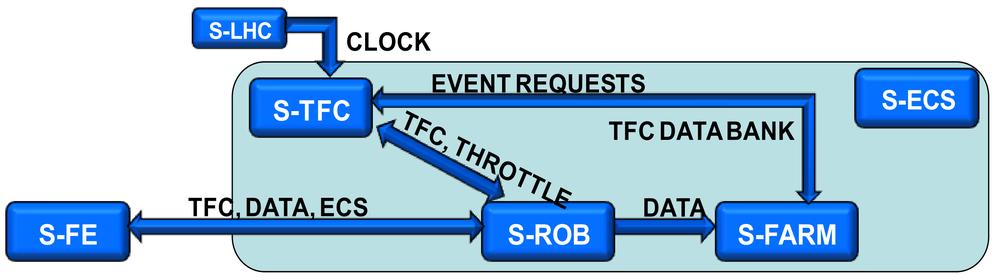
Intro: LHCb @ CERN & LHCb Readout System in 2009





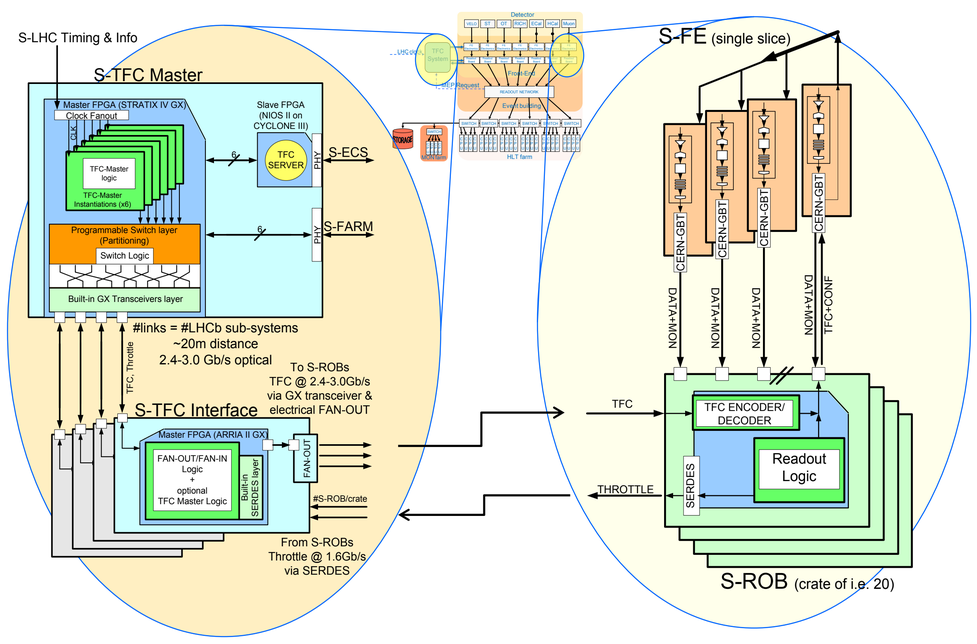
1. Architectures of Readout System: Old vs. New





1. No First-Level Trigger (L0)
2. Point-to-point bidirectional high-speed optical link
   -> Same technology and protcol type for DATA, TFC and THROTTLE signals
   -> Reducing number of links to FE by relaying ECS and TFC info via ROB
3. Partitioning as a crucial aspect for stand-alone tests and sub-detector developments
4. An “event requests” mechanism based on IP destination control is needed in order to balance the load in the processing farm
5. A data bank has to contain info about the identity and source of an event for event management

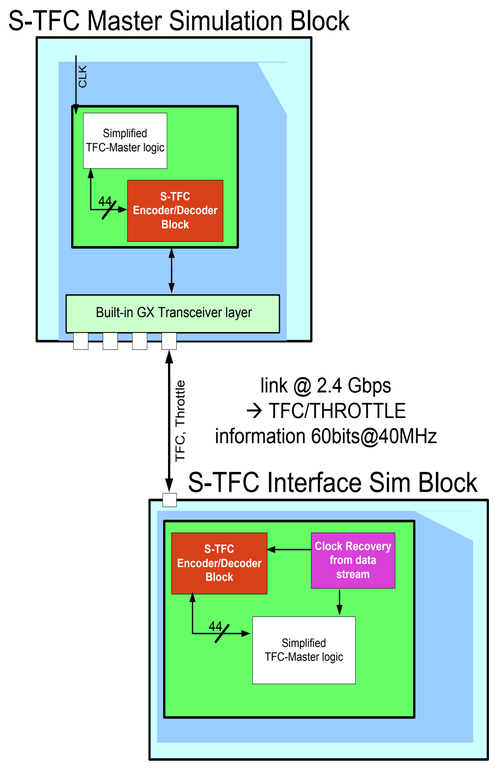
2. Full Simulation Framework of the new S-FE/S-ROB/S-TFC Architecture



What? A synthesizable “clock level-fidel” simulation of S-TFC component and links [1][2][3] clock level emulation of FE+ROB model with variable parameters

Why? Implement and test the TFC functionality and to study the optimum design parameters for the different sub-detector FEs

3. S-TFC Link Simulation



S-TFC Master <-> S-TFC Interface link preliminary protocol

1. TFC control info fully synchronous 60bits@40MHz
   -> 2.4 Gb/s (max reachable 3.0 Gb/s)

EVENT ID (4-12 bits)	TFC information (40-32 bits)	ReedSolomon-FEC (16 bits)

   -> Reed Solomon encoding used on TFC links for maximum reliability (header ~ 16bits) [4]
   -> Asynchronous readout: TFC info must carry Event ID

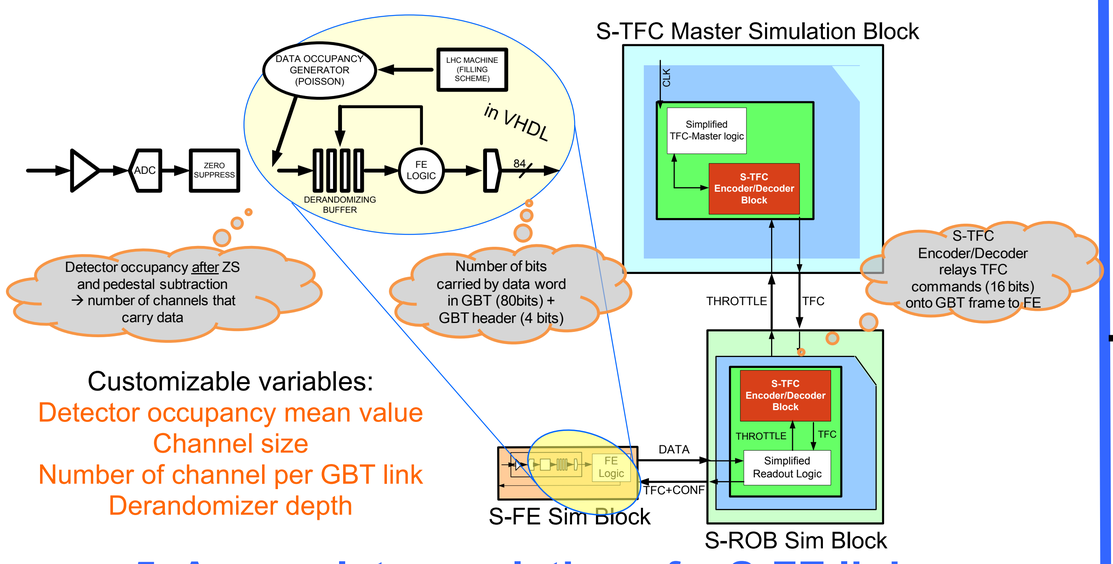
2. Throttle (“trigger”) protocol

EVENT ID (4-12 bits)	THROTTLE information (20 bits)	OTHERS	ReedSolomon-FEC (16 bits)

   -> Must carry Event ID and will require alignment as for TFC protocol

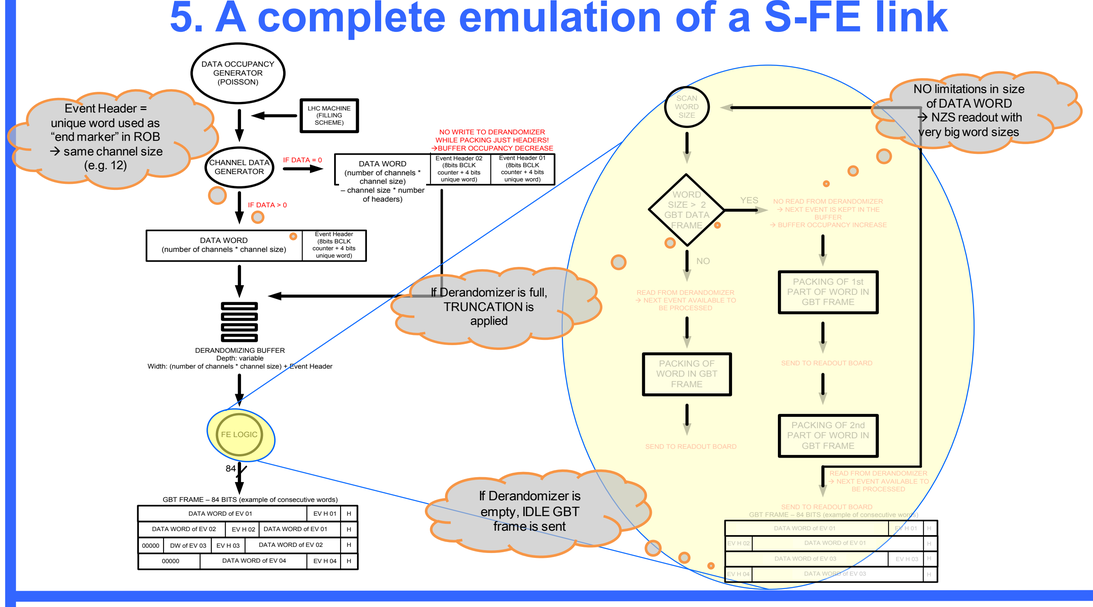
S-TFC links were successfully simulated
-> Additional firmware logic implemented to control the latency and the phase of the clock w.r.t. the data stream over commercial high-speed transceivers in FPGAs (ALTERA GX)
-> Plan to test the link on a (real) board

4. Fully Configurable S-FE/S-ROB/S-TFC Model



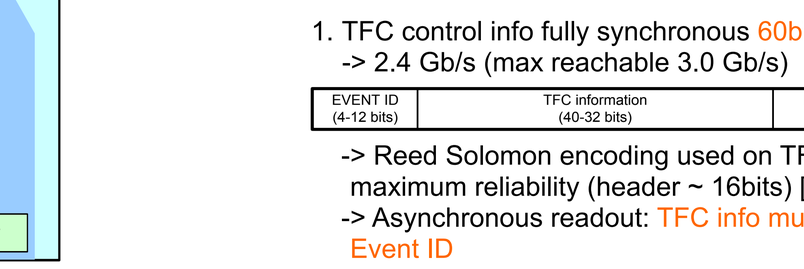
Customizable variables:
Detector occupancy mean value
Channel size
Number of channel per GBT link
Derandomizer depth

5. A complete emulation of a S-FE link



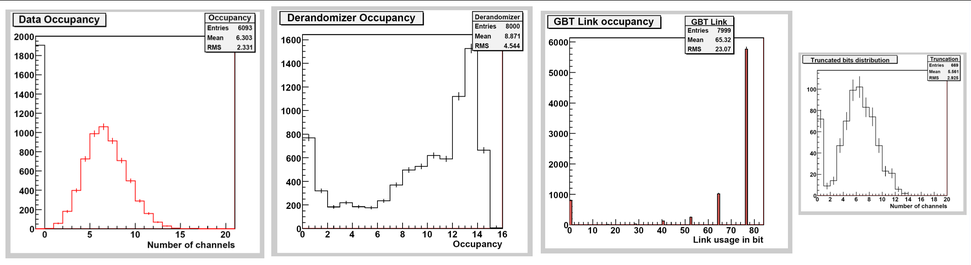
6. “Testing the simulation testbench”: examples

Example 1:
<Detector occupancy> = 30%
#channels/GBT link = 15
  -> ~ 4.5 channels/GBT after ZS
Derandomizer depth = 16
Channel size = 12
(e.g. ADDR = 4bits + ADC_DATA = 8bits)



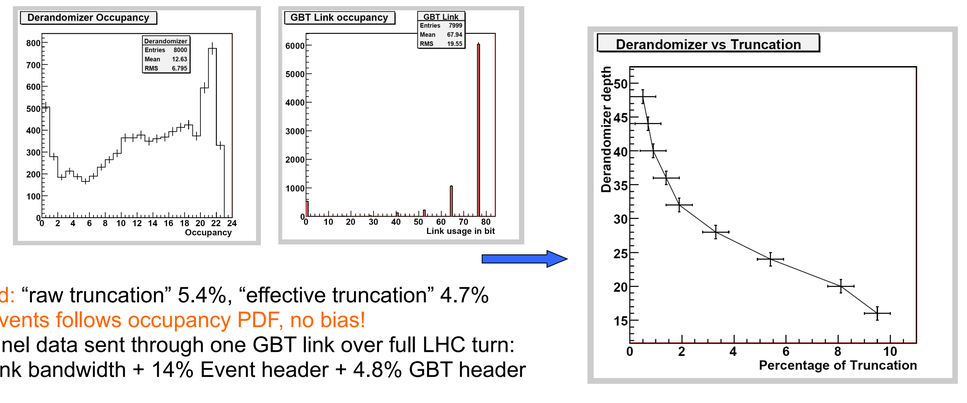
No truncation occurred: system undercommitted
-> 145kbits of channel data sent through one GBT link over full LHC turn:
48.3% of GBT link bandwidth + 14% Event header + 4.8% GBT header

Example 2:
<Detector occupancy> = 30%
#channels/GBT link = 21
  -> ~ 6.3 channels/GBT after ZS
Derandomizer depth = 16
Channel size = 12
(e.g. ADDR = 5bits + ADC_DATA = 7bits)



Truncation occurred: “raw truncation” 10.5%, “effective truncation” 9.5%
Size of truncated events follows occupancy PDF, no bias!
-> 184kbits of channel data sent through one GBT link over full LHC turn:
61.6% of GBT link bandwidth + 14% Event header + 4.8% GBT header

Example 3:
<Detector occupancy> = 30%
#channels/GBT link = 21
  -> ~ 6.3 channels/GBT after ZS
Derandomizer depth = 24
Channel size = 12
(e.g. ADDR = 5bits + ADC_DATA = 7bits)



Truncation occurred: “raw truncation” 5.4%, “effective truncation” 4.7%
Size of truncated events follows occupancy PDF, no bias!
-> 193kbits of channel data sent through one GBT link over full LHC turn:
64.4% of GBT link bandwidth + 14% Event header + 4.8% GBT header

References:

[1] F.Alessio, Z. Guzik, R.Jacobsson, “Timing and Fast Control and Readout Electronics Aspects of the LHCb Upgrade”, LHCb Public Note, LHCb 2008-072
[2] F.Alessio, Z. Guzik, R.Jacobsson, “A 40 MHz Trigger-free Readout Architecture for the LHCb experiment”, 16th IEEE-NPSS Conference, 10-15 May 2009, Beijing, China, submitted to IEEE TNS
[3] Marin F., Grassi T., Moreira P., Soos C., Cachemiche J-P., Baron S, “Implementing the GBT data transmission protocol in FPGAs”, TWEPP09 Plenary Session 6, Programmable Logic, Boards, Crate and Systems
[4] Moreira P, “The GBT Project”, TWEPP09 Parallel Session B5, Optoelectronics and Links