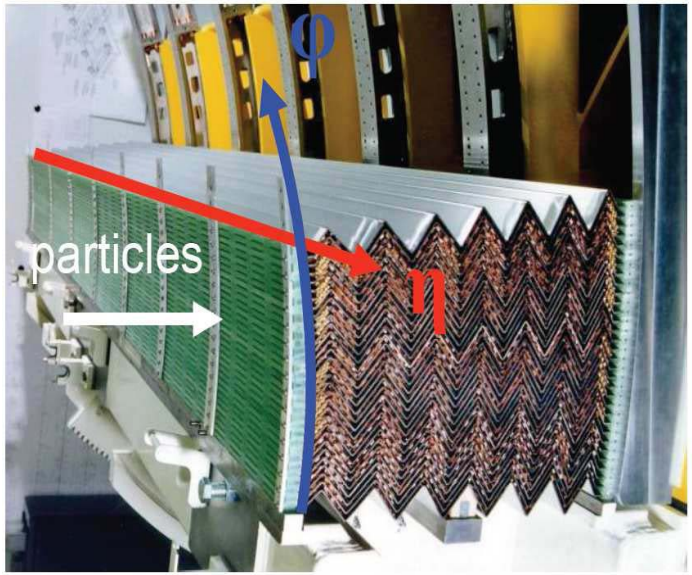
LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

Mitch Newcomer
On Behalf of the ATLAS LAr Calorimeter Group*

*Special Acknowledgment of the significant contributions of Emerson Vernon, Sergio Rescia (BNL) and Nandor Dressnandt (Penn) to this work.

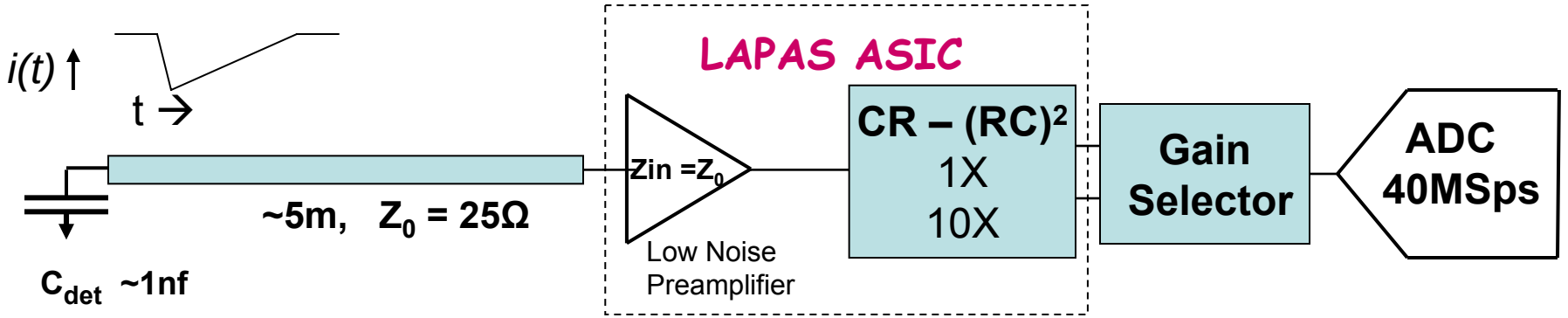
FEE Design Constraints / Goals for a LAr Barrel Calorimeter at SLHC



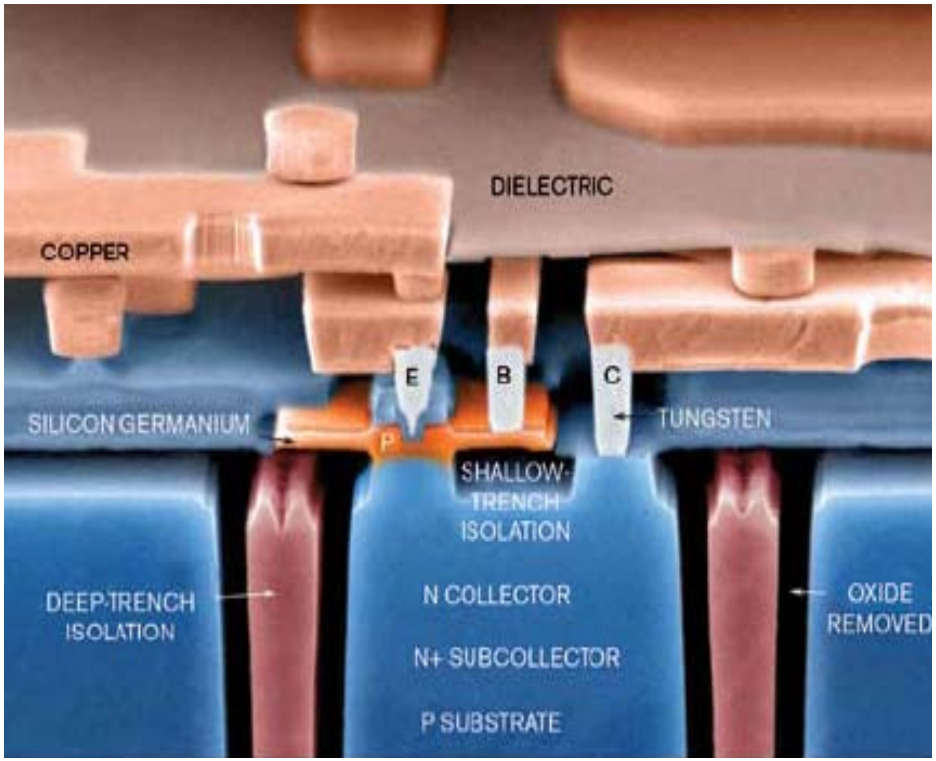
Physics Requirement
- Dynamic energy range: 20MeV - 2 TeV,
- Good energy resolution
- Minimize Pileup

Drift time 400ns.
Signal 25ns rise (1nF 25Ω rin), 400ns fall.
Readout Dynamic Range ~16 Bits
Noise referred to input. ENI < 75nA RMS

FEE **Rad Tolerance** TID~ 300Krad,
Neutron Fluence ~10^{13} n/cm^2



SiGe Bipolar Technology



***EDN 9/18/2008 credited to IBM**

Strained Lattice (Si-Ge)

- **Epitaxial Ge film in base layer.**
- **Increases base emitter band gap for holes.**
- **Improves Radiation Tolerance.**
- **Reduces recombination in the base.**
- **Increases mobility → High f_t**
- **Excellent Low temp gain stability.**
- **Allows higher doping in base.**
  Lowers rbb'

***SiGe** technology was first introduced to the HEP community by John Cressler :
Assessing SiGe HBT Technology For Front-end Electronics Applications
5th International Meeting on Front-end Electronics Snowmass, CO, June 2003

IBM **8WL SiGe BiCMOS**

Pro's

- Excellent Bipolar Analog performance. Possible to use Vdd > 5V
- Excellent radiation hardness well beyond requirement.
- IBM support for the foreseeable future (> 5 years)
- CMOS Digital Libraries in use for other CERN projects should be available for use with these BiCMOS processes.
- 8WL is the least expensive 130nm SiGe bipolar process available from IBM.

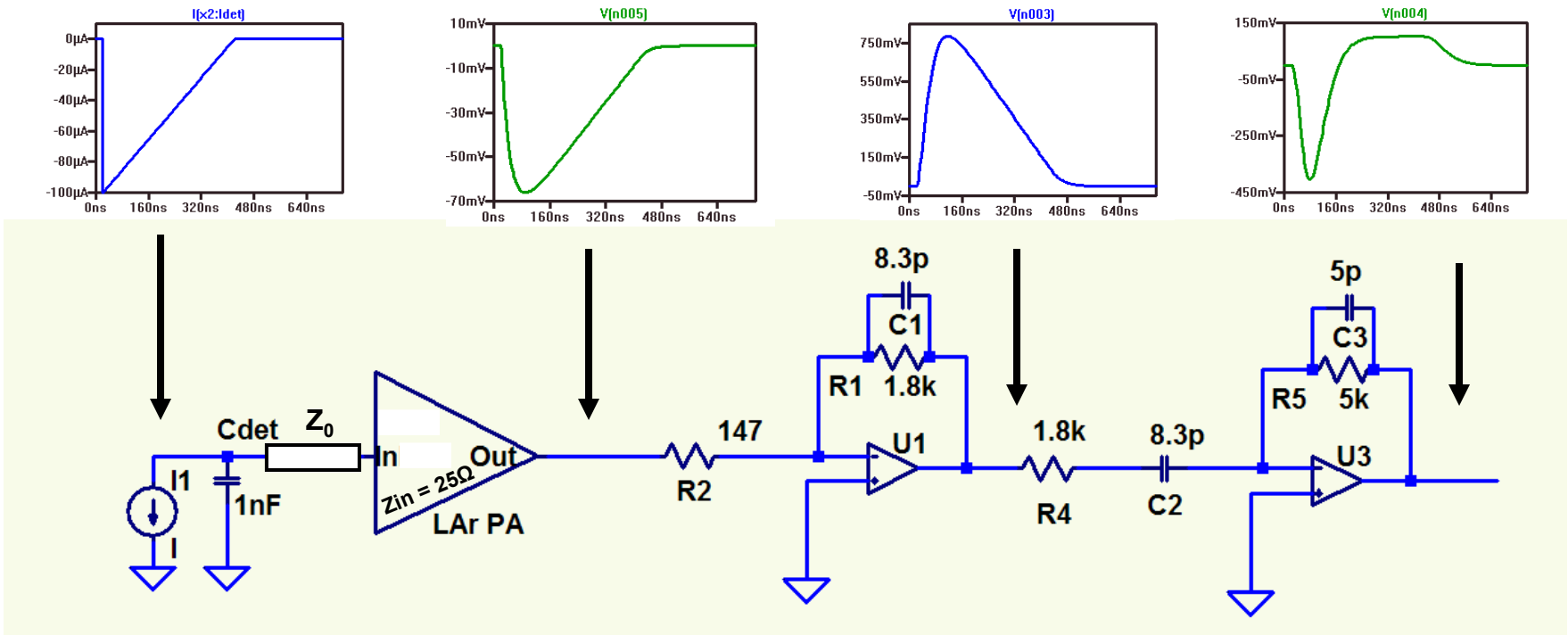
Con's

- No PNP's. Must use PMOS.
- Complex process design rules.
- Potential increased (npn) SEU susceptibility *compared* with 8HP
- More complex process than CMOS which has a significant cost premium. (May be reduced as competitive processes come online.)

FEE LAr Signal Processing

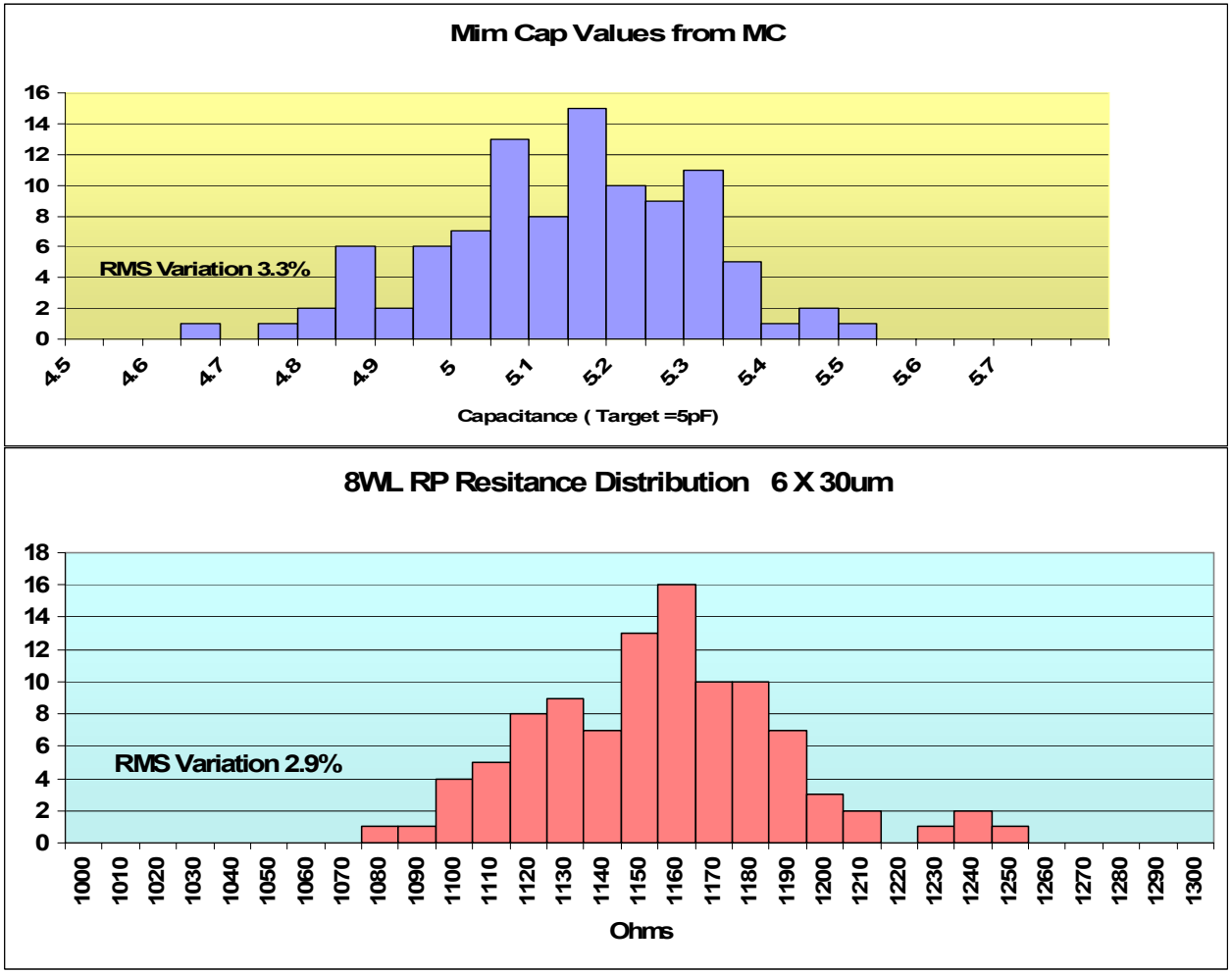
All RC = 15ns

Sampled at 40MSPS



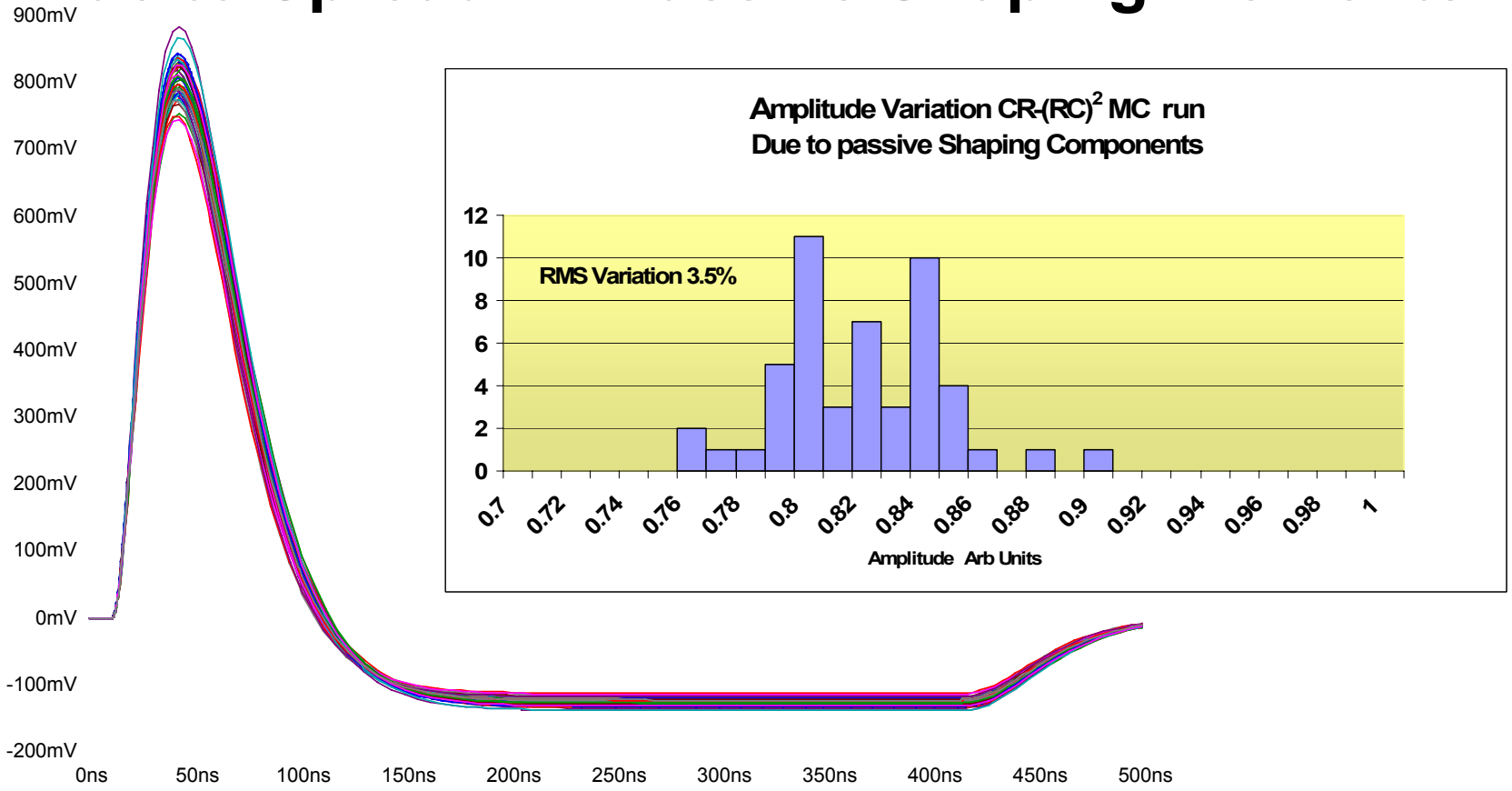
Shaping Primarily dependent on ASIC Passive elements

Predicted Precision of SiGe Process Passive Shaping Elements



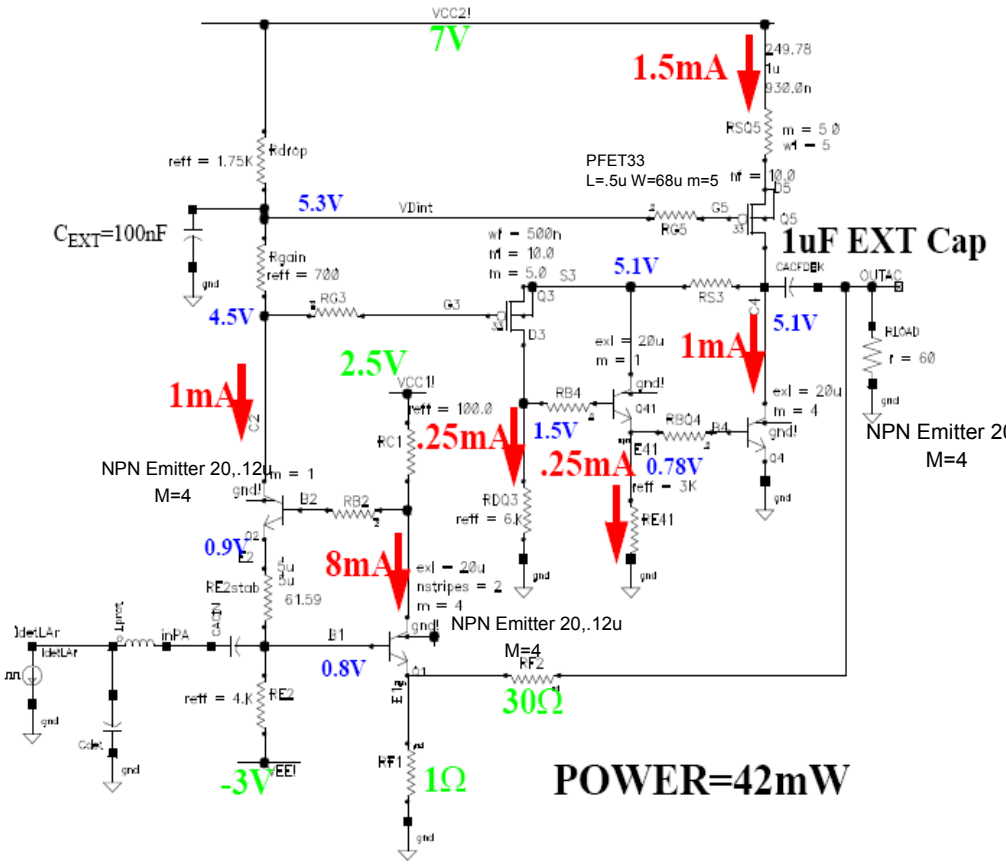
Calculated Shaper Signal Variation

Due to Spread in Passive Shaping Elements



→ May not be necessary to tune each channel to stay within a 5% Channel to Channel gain requirement for trigger sums.

SiGe LAr **Preamp** (Rin=25Ω)

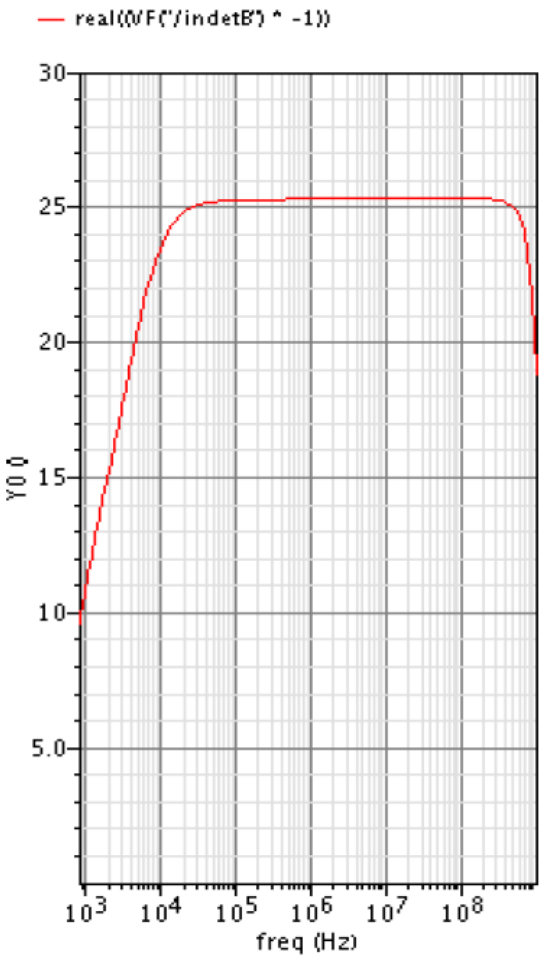


- Based on low noise line-terminating preamplifier circuit topology presently used in ATLAS LAr
- SiGe higher base doping ⟹ lower $r_{bb'}$ for low noise
- "high breakdown" (V_B=3.6 V devices allow for higher swing to accomodate full 16-bit dynamic range
- thick "analog" metal allows for low resistance connections to input, E_1
- BJTs are excellent drivers: output current ~170mA at I_{in}=5mA
- $e_{n,equiv}$=0.26nV/√Hz
- ENI=73nArms (incl. 2nd stage, C_d=1nF)
- P_{tot}=42 mW

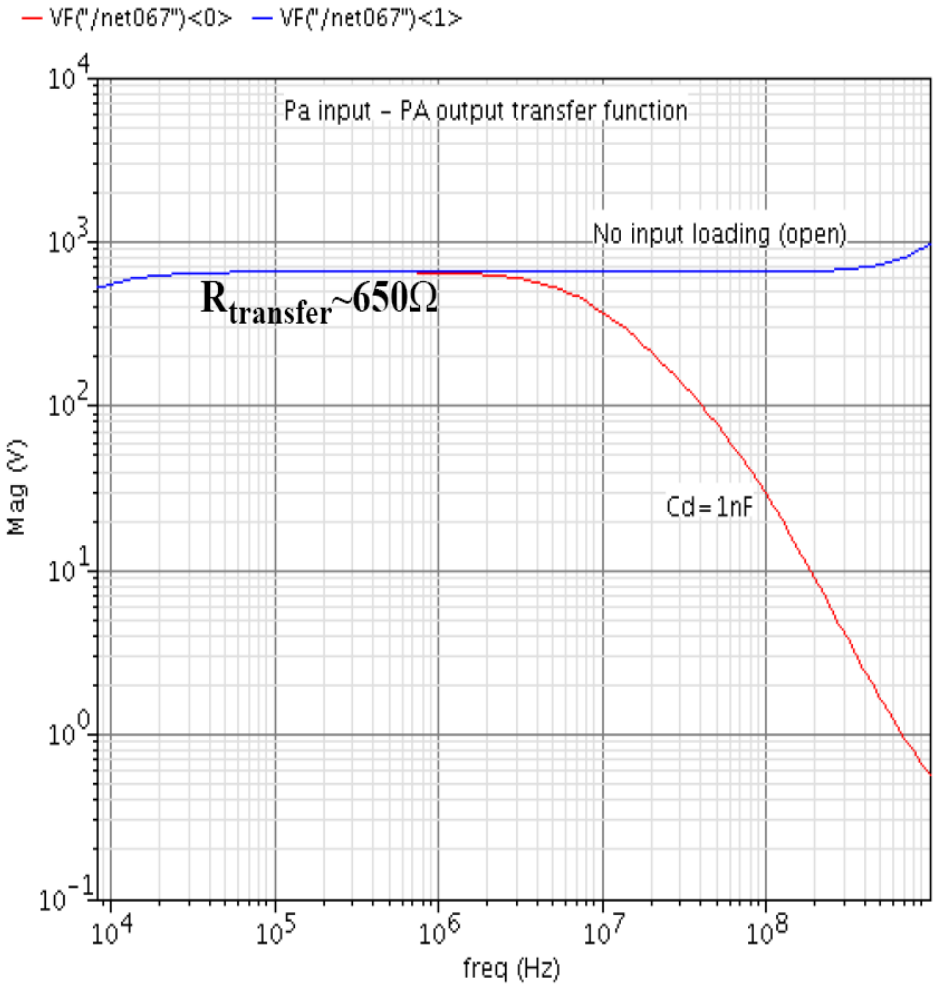
Operational Characteristics

(Simulation Results)

Real Zin



Transfer Function



Calculated Preamp and Shaper Noise Contributions

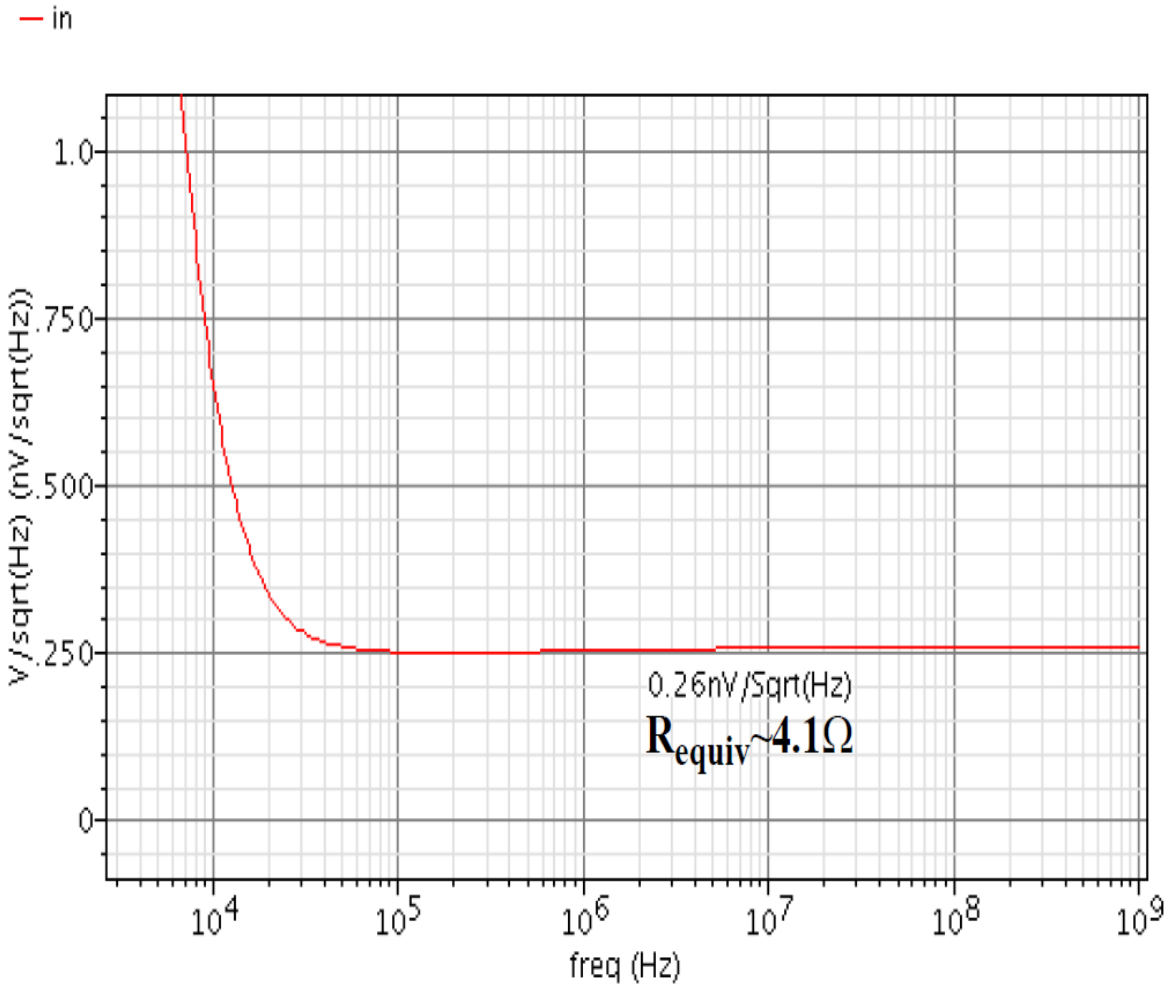
Noise Summary (>1% contributions, incl 2nd stage noise, 2nV/Sqrt(Hz))

Device	% Of Total	Inp Ref Noise Param		Noise Contribution	
Q1.q	55.10	0.000404166	total	1.08042e-05	Q1+feedback=71%
			itzf	8.03375e-06	
			rbx	5.79295e-06	
			ibe	2.87805e-06	
			rbi	2.6965e-06	
			re	1.75006e-06	2nd Stage=9%
/Rnoisesheq	8.70	0.0077712	rn	4.29214e-06	
RF1.rmb	4.65	1.32473e-05	rn	3.1375e-06	16%
RF1.rma	4.65	1.32473e-05	rn	3.13749e-06	
RF1.reb	3.47	1.1451e-05	rn	2.71207e-06	
RF1.rea	3.47	1.1451e-05	rn	2.71207e-06	
/Q3	2.90	0.00187966	total	2.4802e-06	
			id	2.33136e-06	
			fn	8.1065e-07	
			rs	2.42875e-07	
Rgain.rmb	2.86	2.63272e-05	rn	2.46295e-06	5.7%
Rgain.rma	2.86	2.63272e-05	rn	2.46295e-06	
RC1.rmb	1.75	2.06787e-06	rn	1.92389e-06	4.1%
RC1.rma	1.75	2.06787e-06	rn	1.92389e-06	
Q2.q	1.51	7.85253e-05	total	1.78959e-06	
			itzf	1.17054e-06	
			ibe	1.14894e-06	
			rbx	6.51697e-07	
			rbi	2.60069e-07	
			re	1.39711e-07	
RE2stab.rma	1.18	4.06117e-06	rn	1.58407e-06	2.4%
RE2stab.rmb	1.18	4.0455e-06	rn	1.58406e-06	
RE2.rma	0.52	2.40409e-05	rn	1.05455e-06	1%
RE2.rmb	0.52	2.40409e-05	rn	1.05455e-06	

Integrated Noise Summary (in V) Sorted By Device Composite Noise
Total Summarized Noise = 1.45553e-05
Total Input Referred Noise = 0.00914256

ENI= 14.55uVrms * 5mA/1V= 73nArms **(Preamp ENI = 66.4nA)**

Input Referred Preamp Noise Contribution (Calculated)

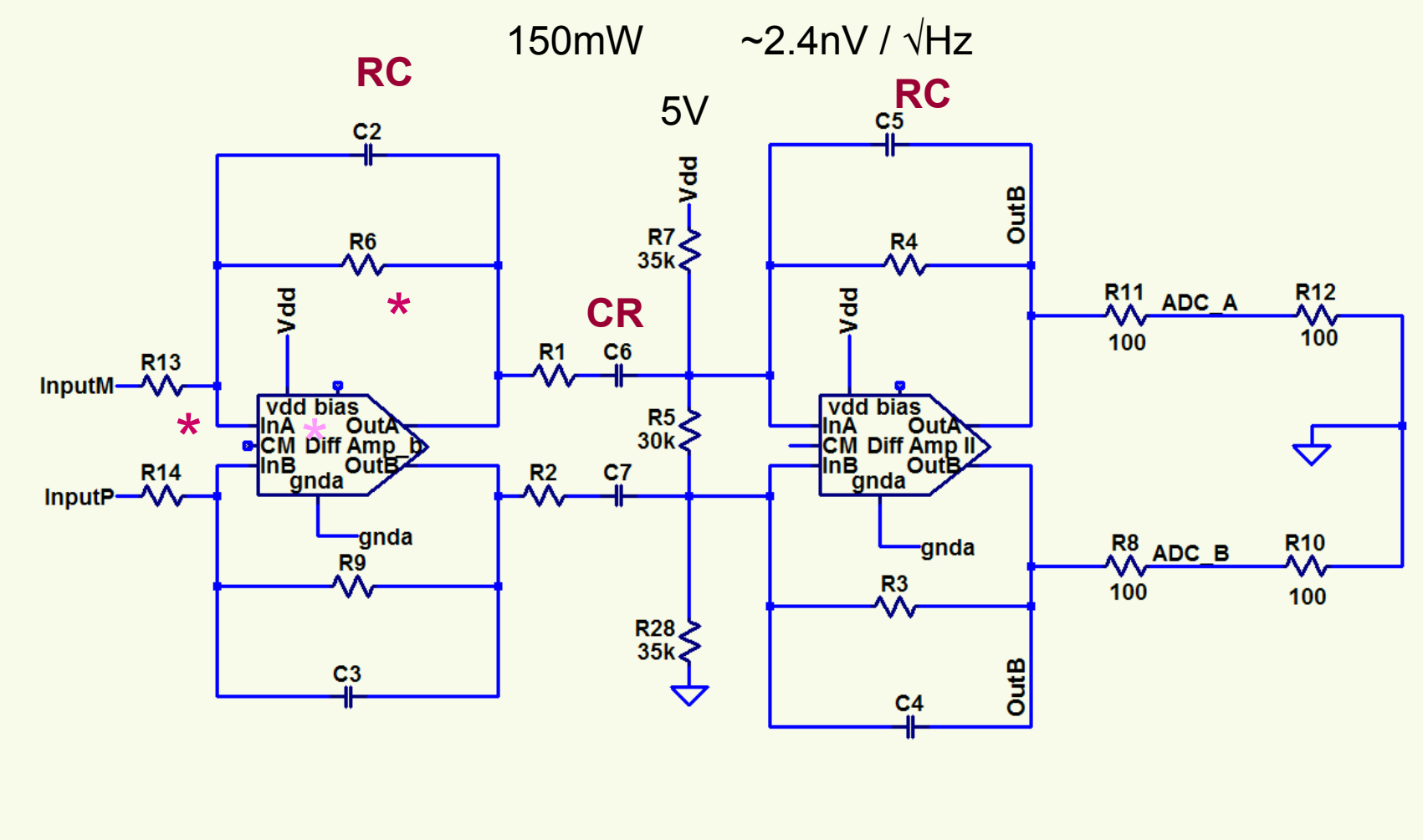


Prototype Shaper Design Goals

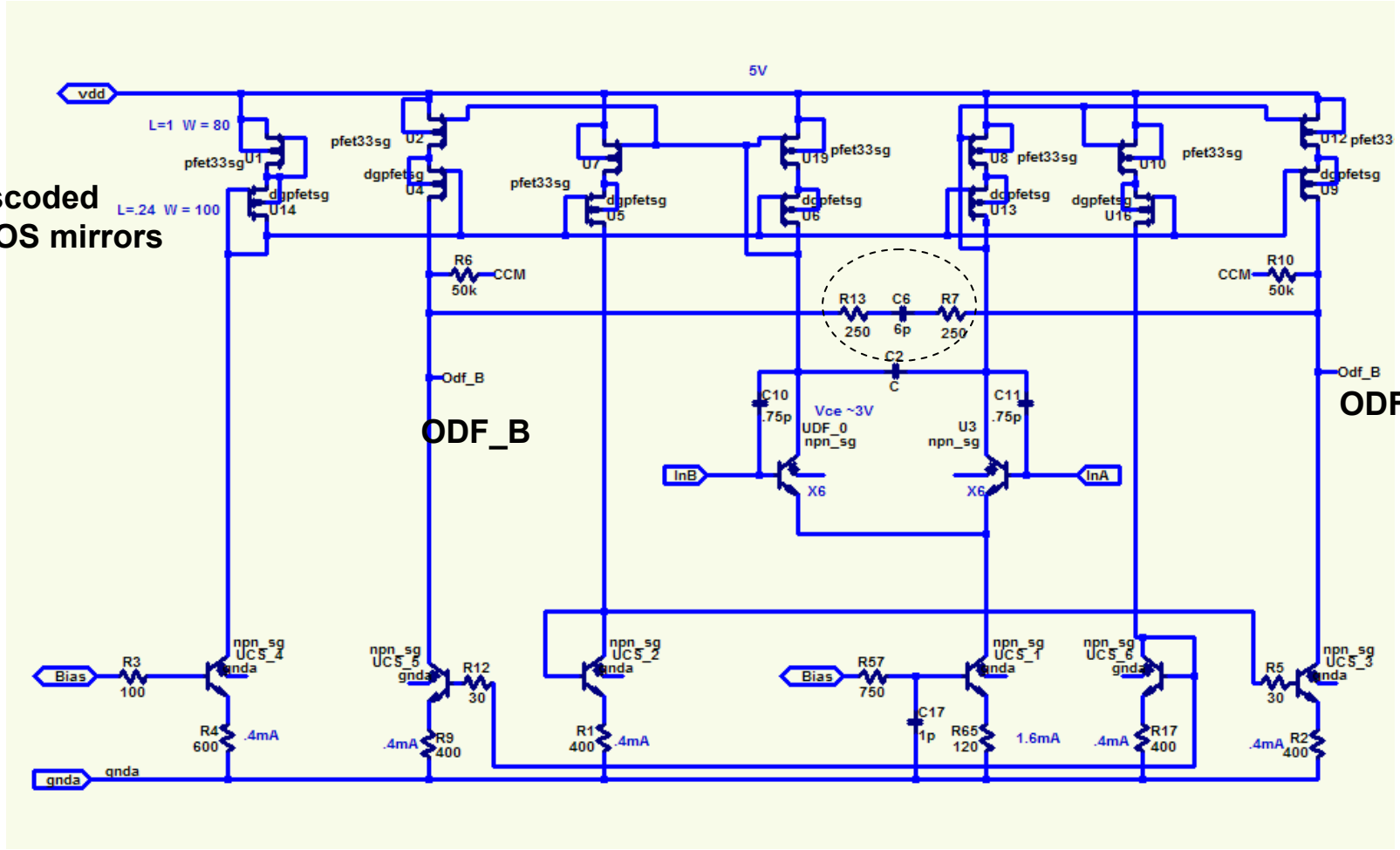
- 2.2nV / √Hz (Adds 10% to Preamp noise)*
- 15 - 16 bit Dynamic range, Less than .1% INL*
  (Necessary to use Dual or Triple ranges)
- Low Power 100 – 200 mW*
- Part to part amplitude variation < 5%
- Should be easily matched to a differential ADC

*Competing goals

Shaper Blocks



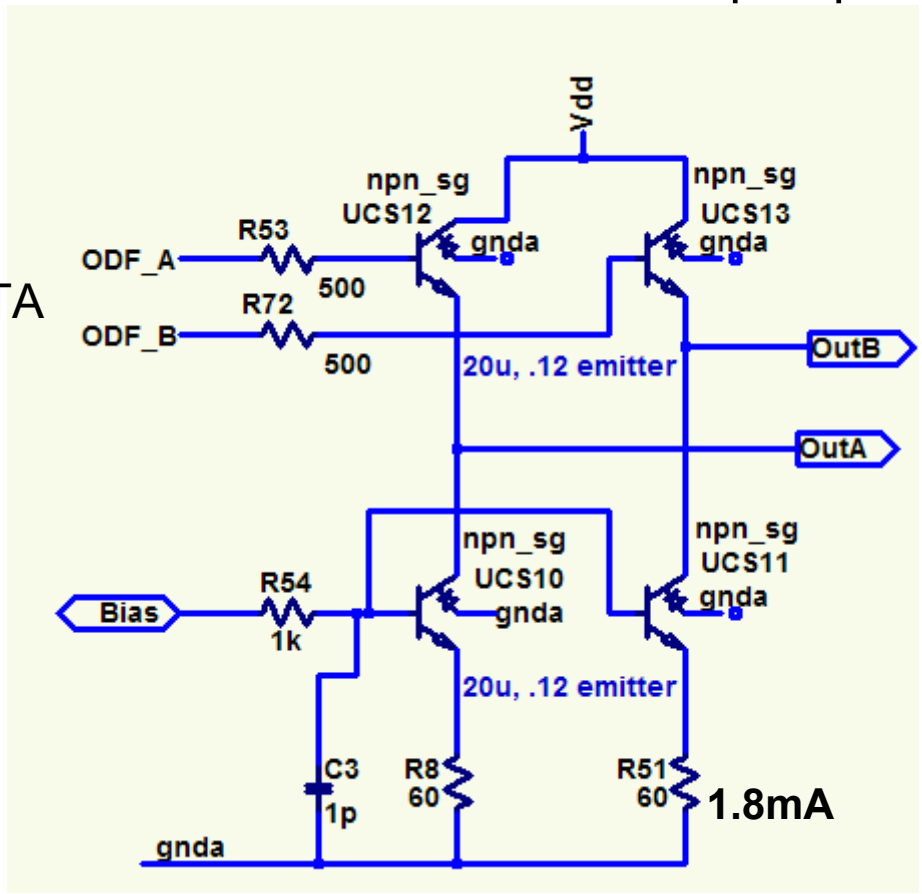
Input OTA Block



Voltage output Driver

Turns OTA back into Opamp

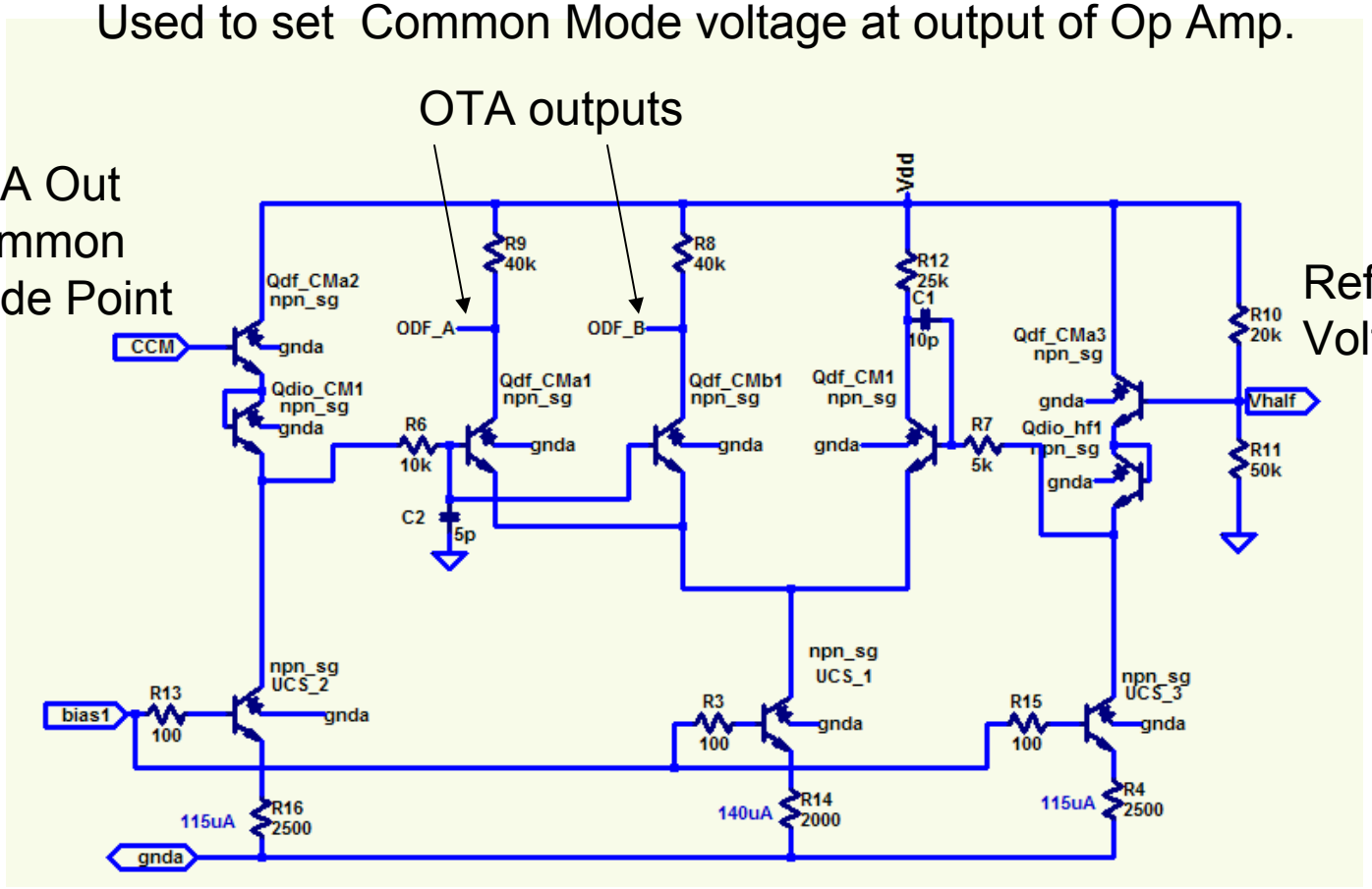
Outputs of OTA



OPAmp Output

Common Mode Amp

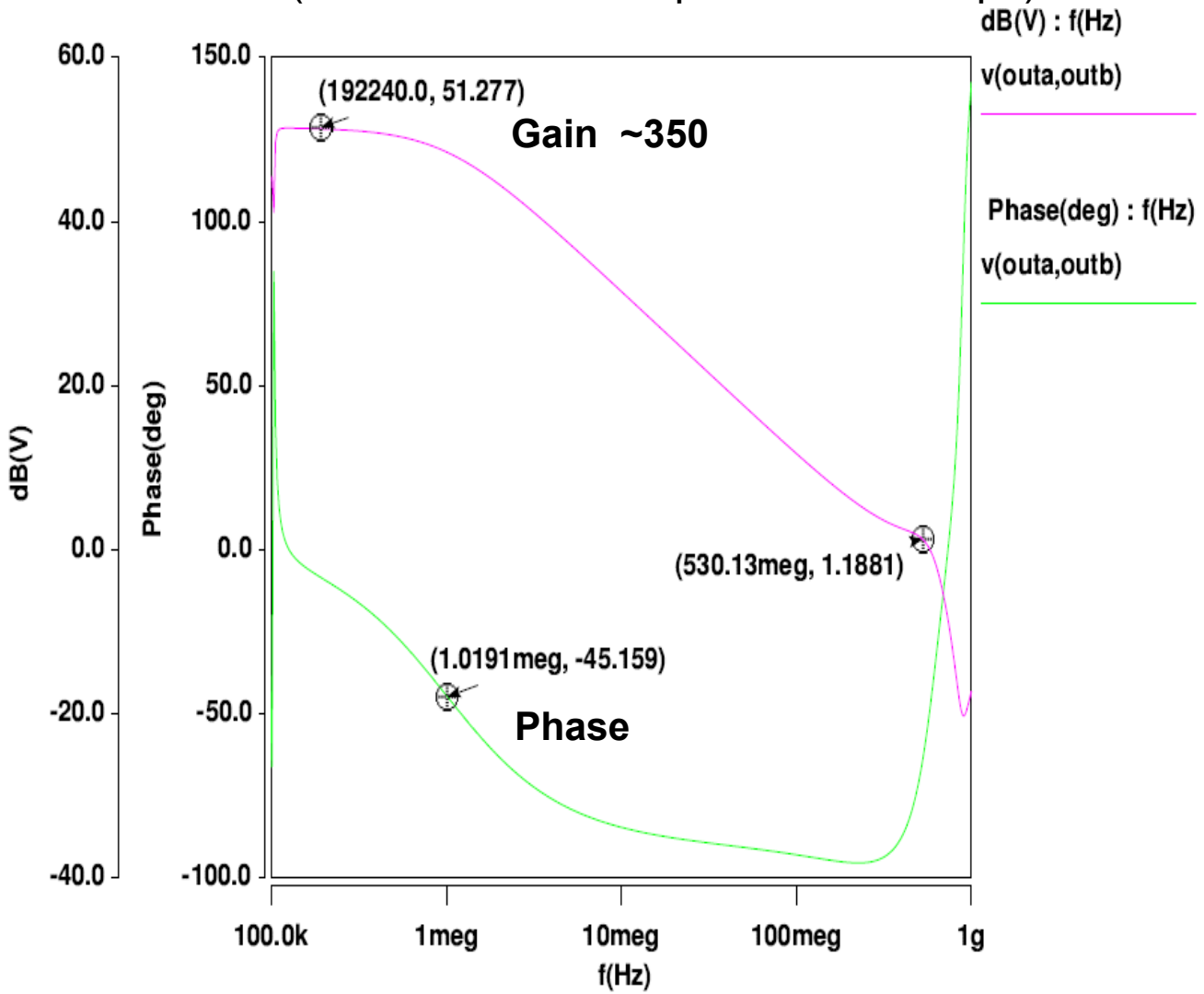
Used to set Common Mode voltage at output of Op Amp.



Open Loop Response

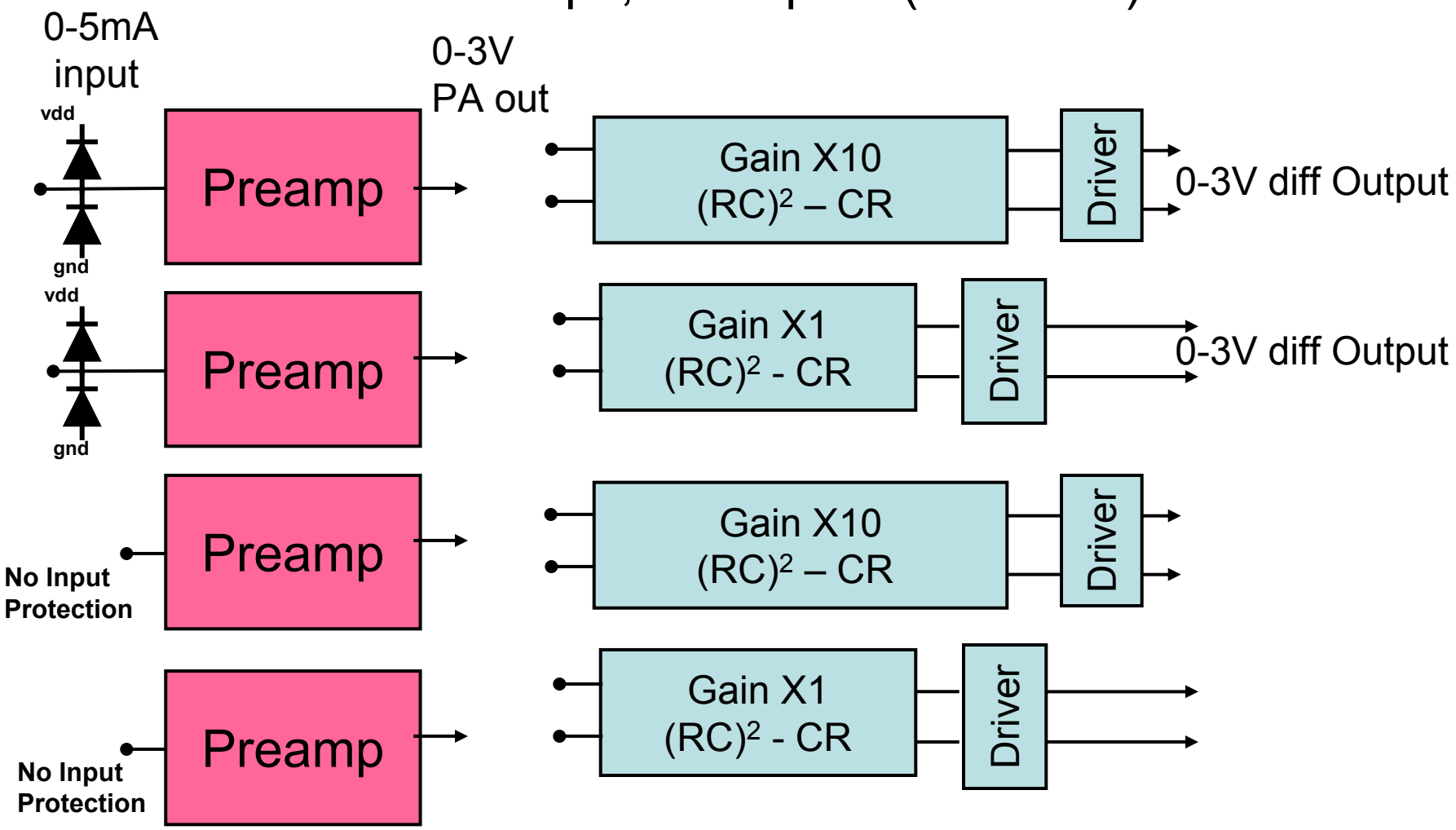
Layout Extracted AC OPAmp

(Includes external 5pF feedback caps)



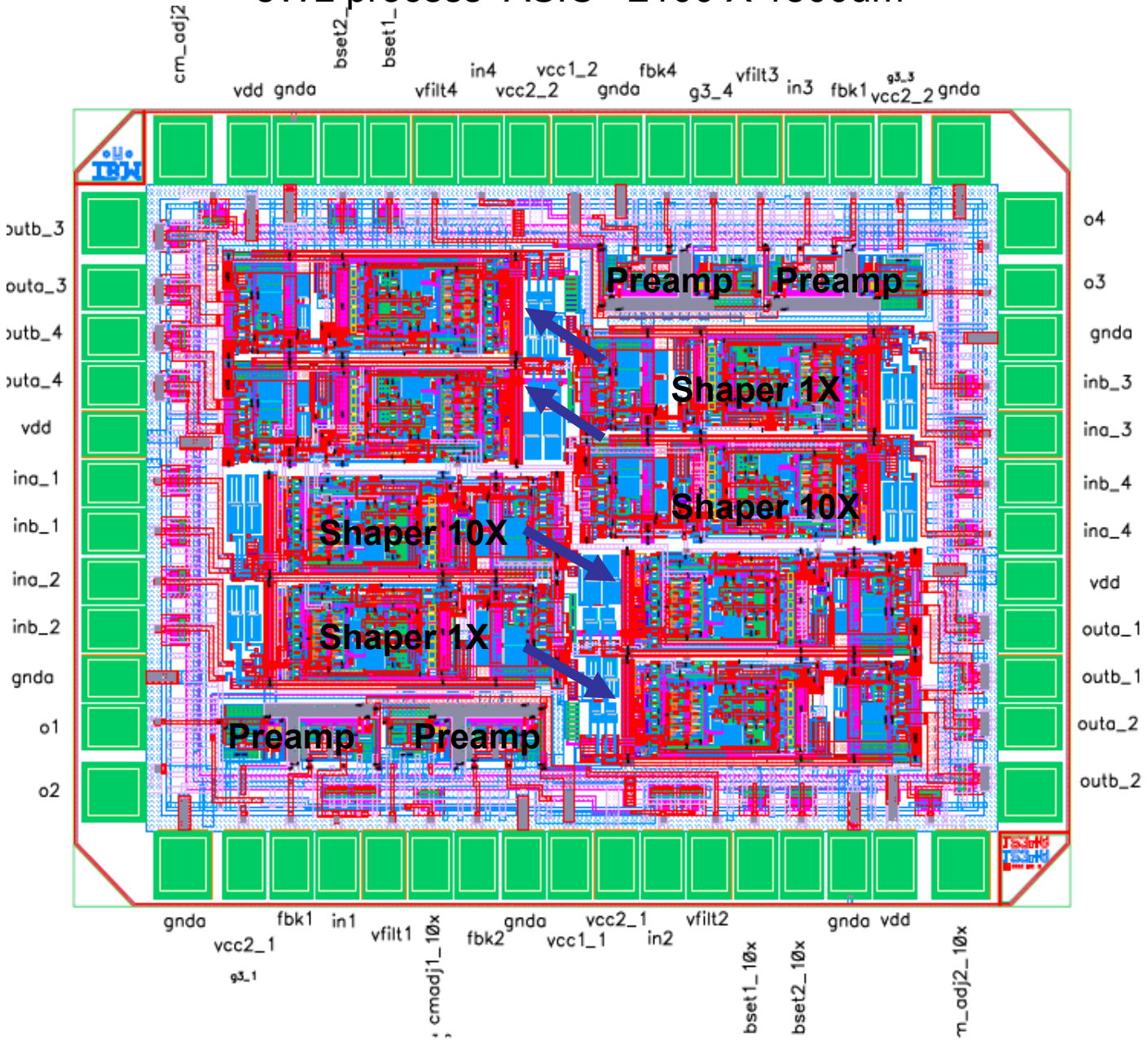
Circuit Blocks LAPAS

4 Preamps, 2 Shapers (1X &10X)

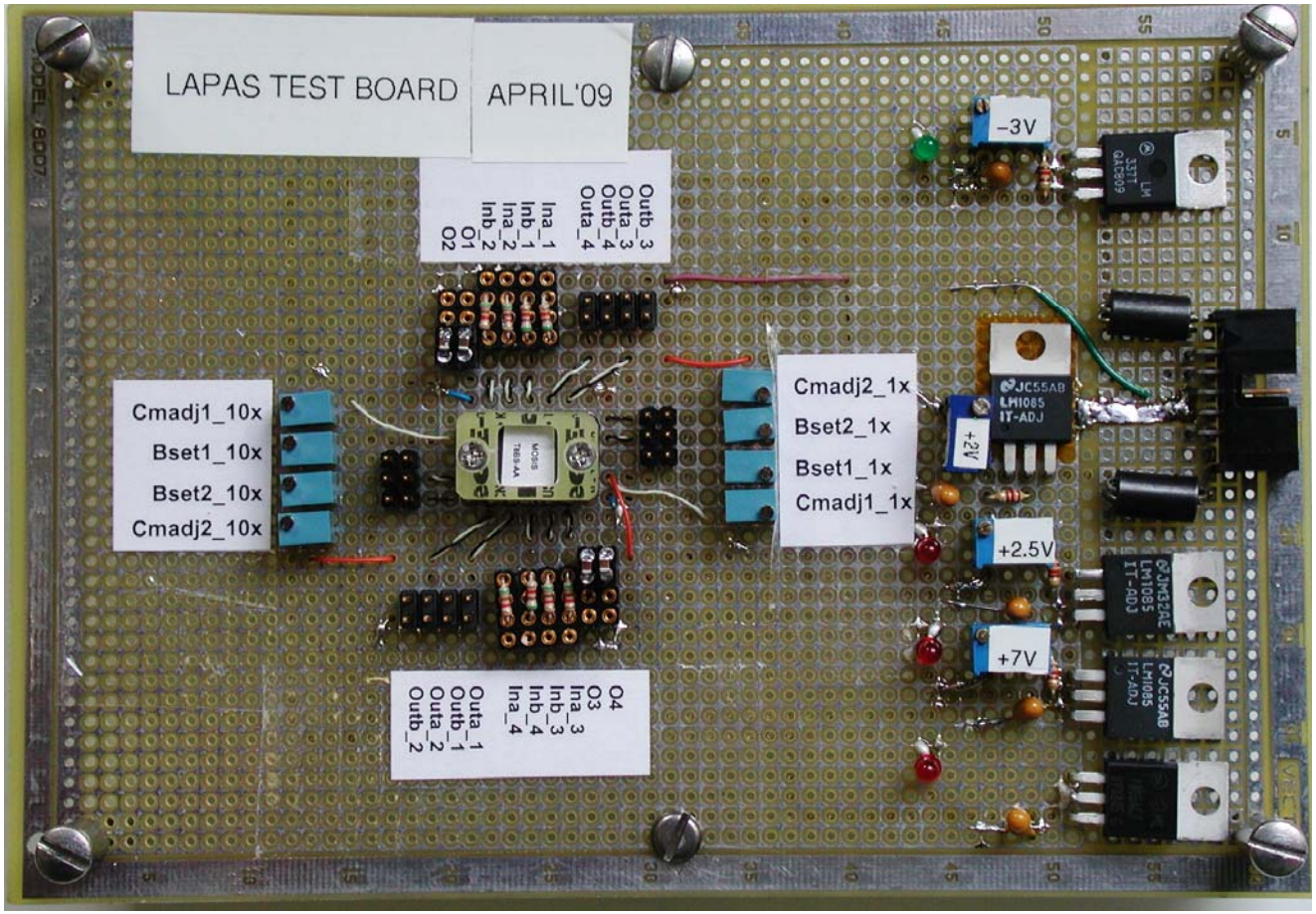


LAPAS: Liquid Argon PreAmplifier Shaper

8WL process ASIC 2100 X 1800um



Measurements with Hand Wired Board



Handiwork of Godwin Mayers, Penn

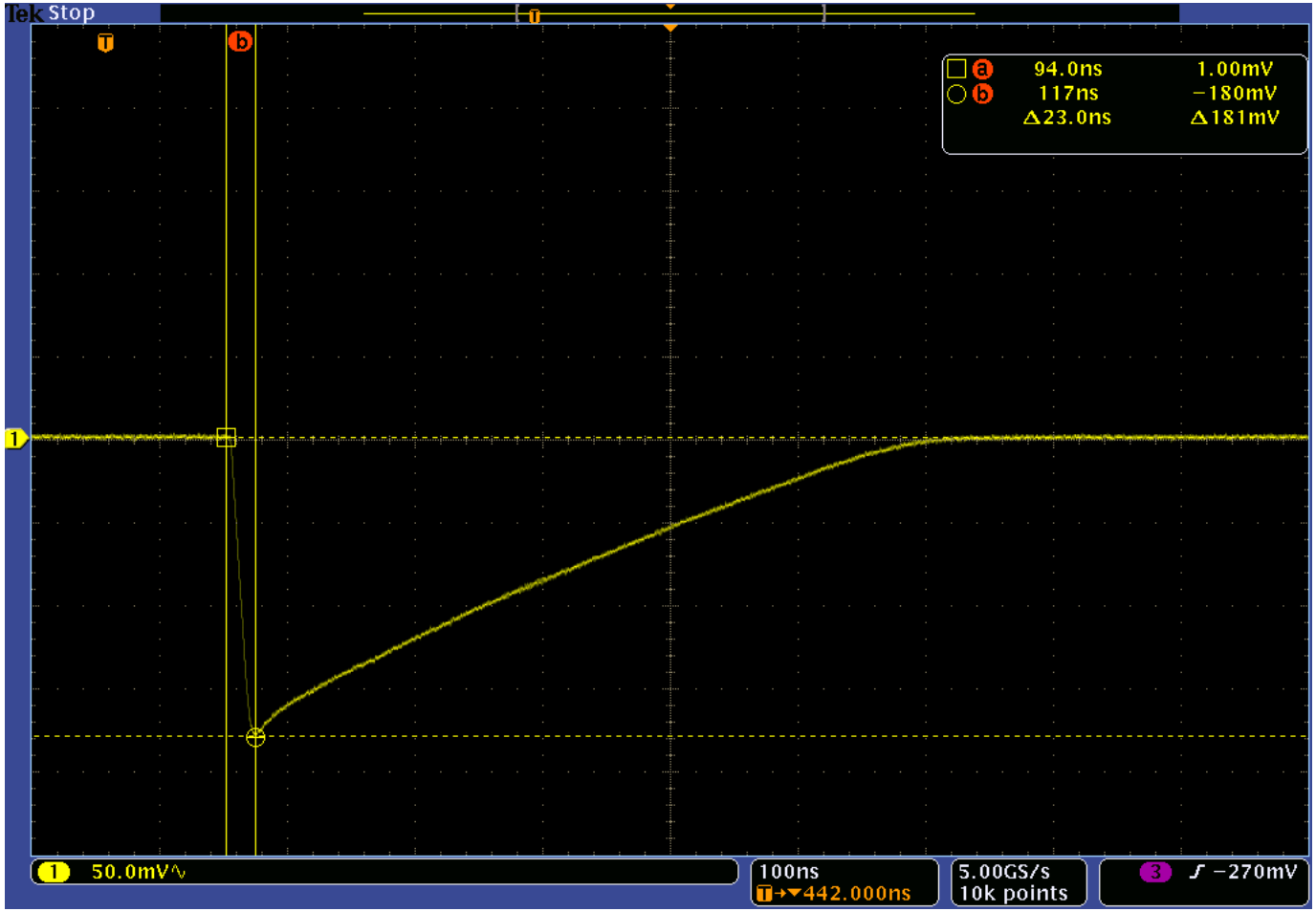
Test Signal Input Attached to Shaper

Lecroy 9210
Pulser:
12ns Rise
20ns width
400ns fall
Amplitude Setting:
1V Shaper tests

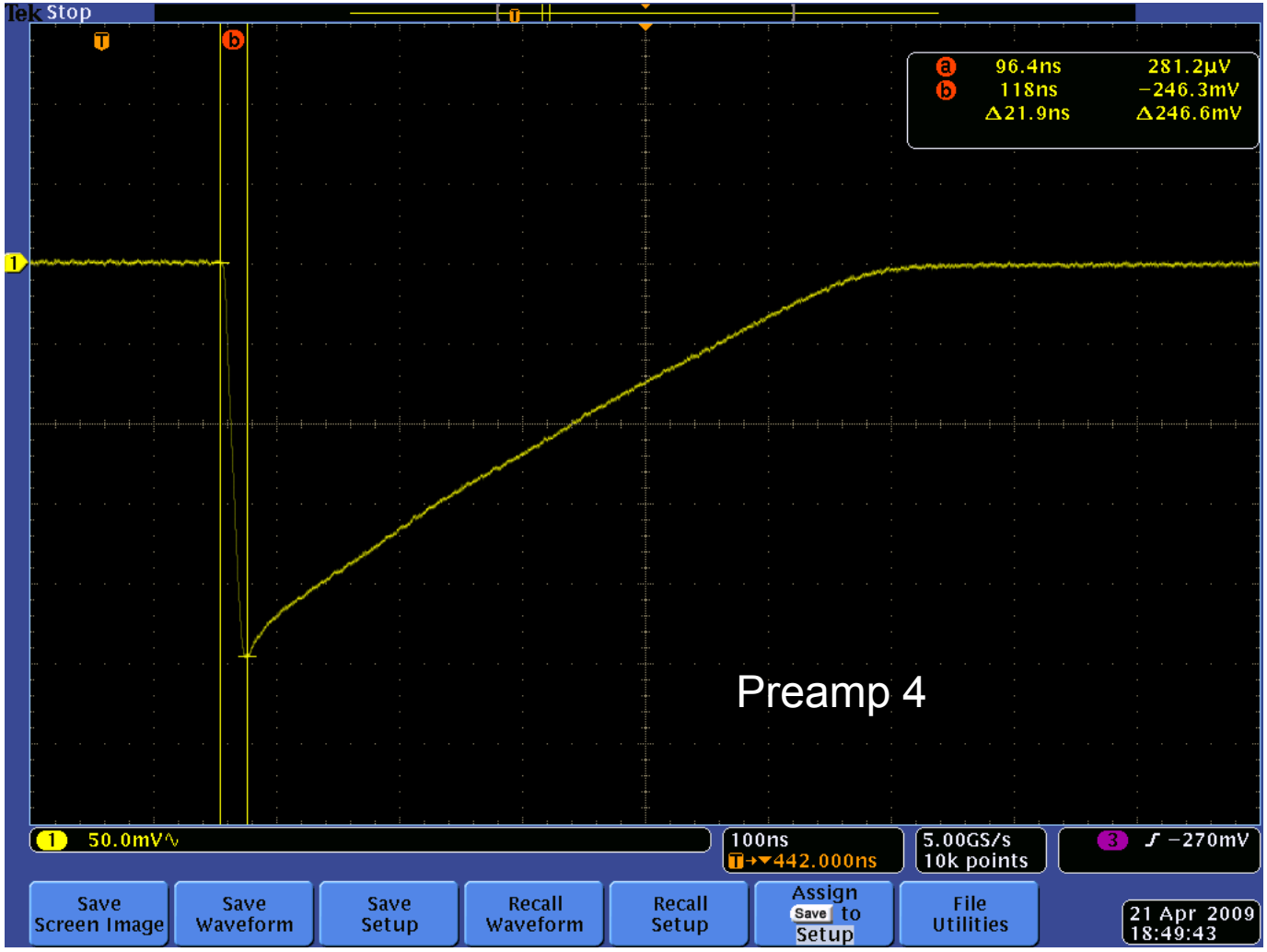
Shaper input
Shown = 5:1Atten

Preamp V → I = 5.1k

AC coupled



Preamp Output Ch 4

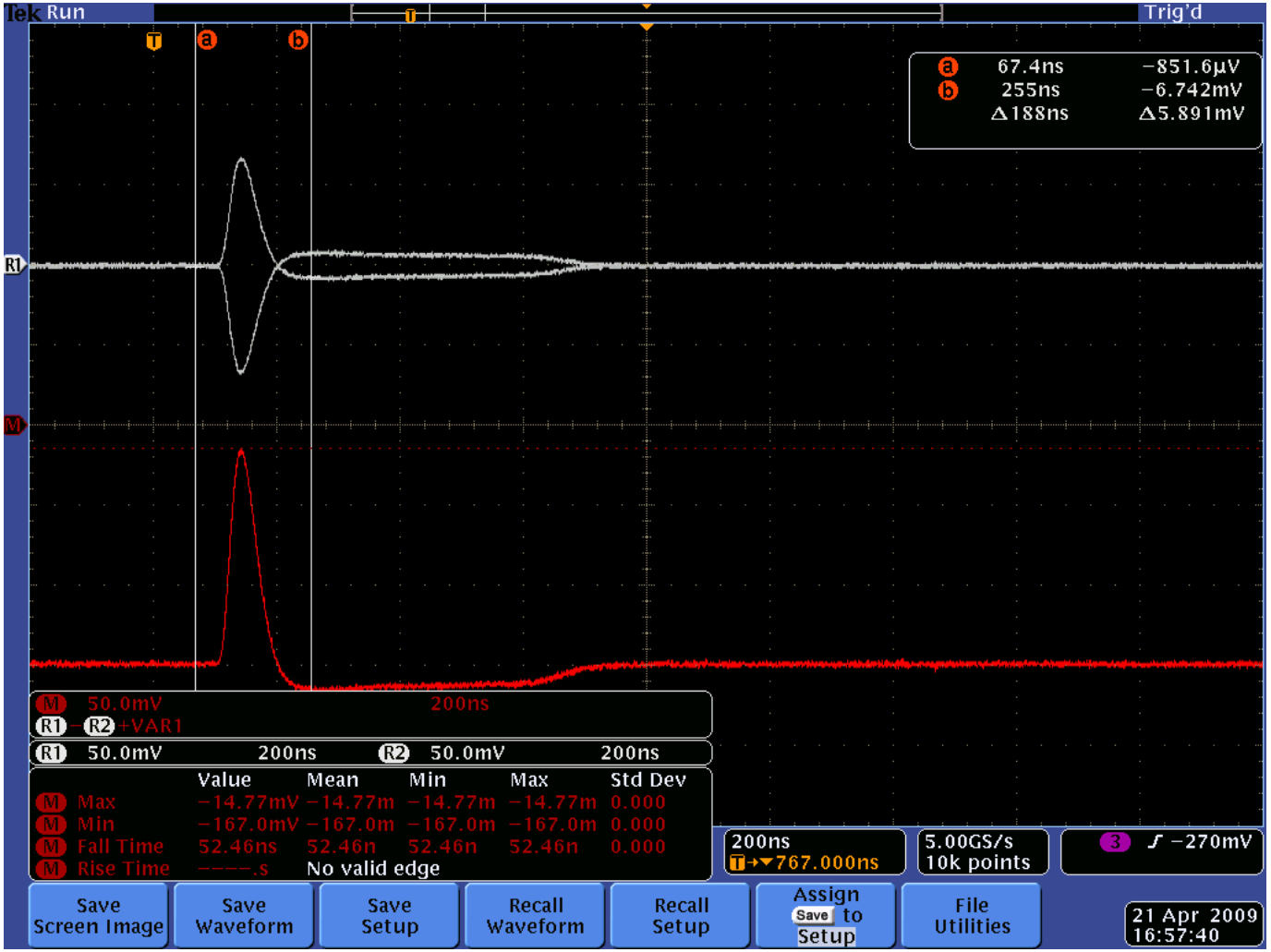


Shaper 1X output
Expected $(RC)^2$ – CR Shaping

Individual Differential Outputs A, B AC coupled

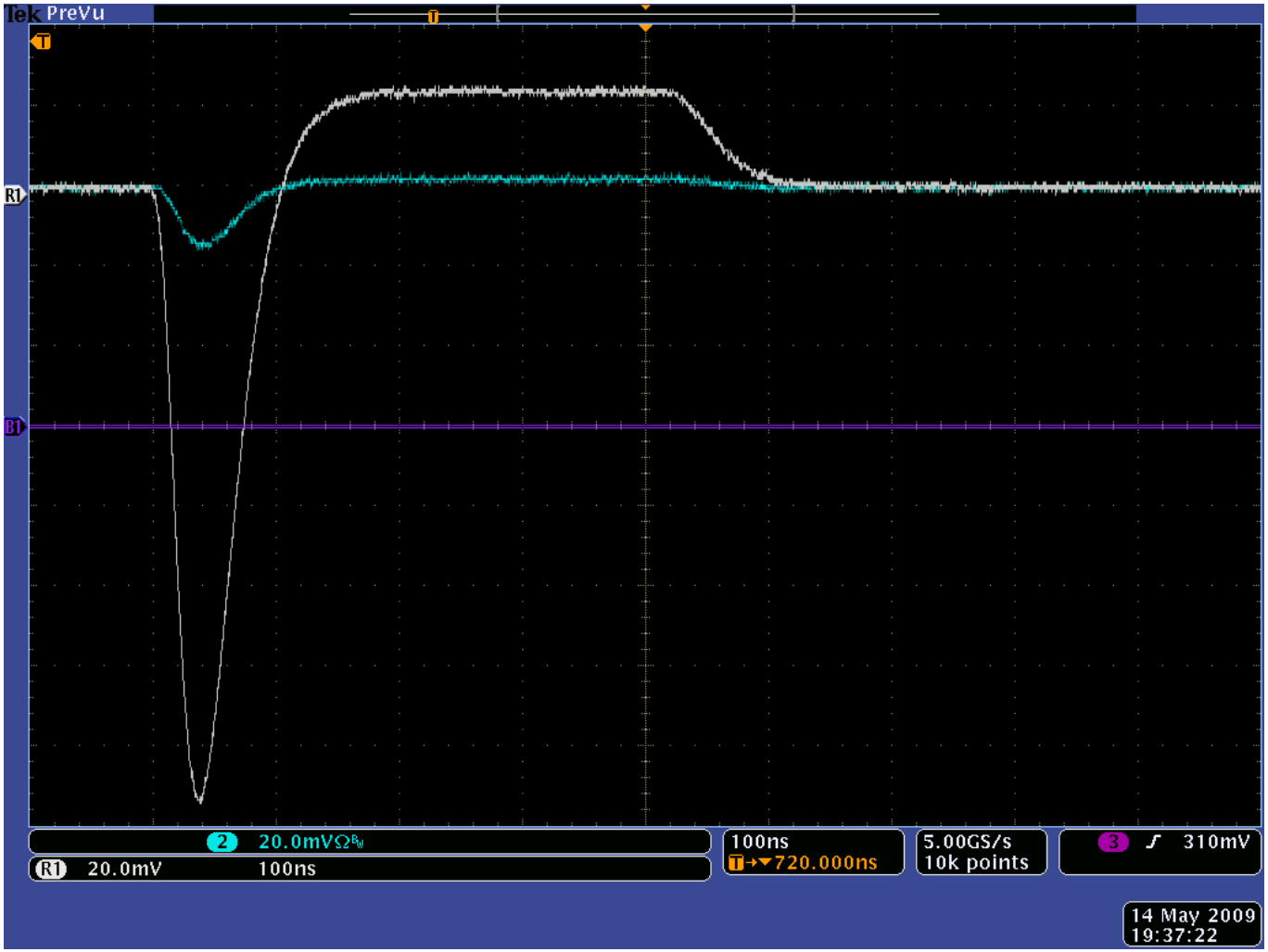
Out A – Out B

37ns Peaking time



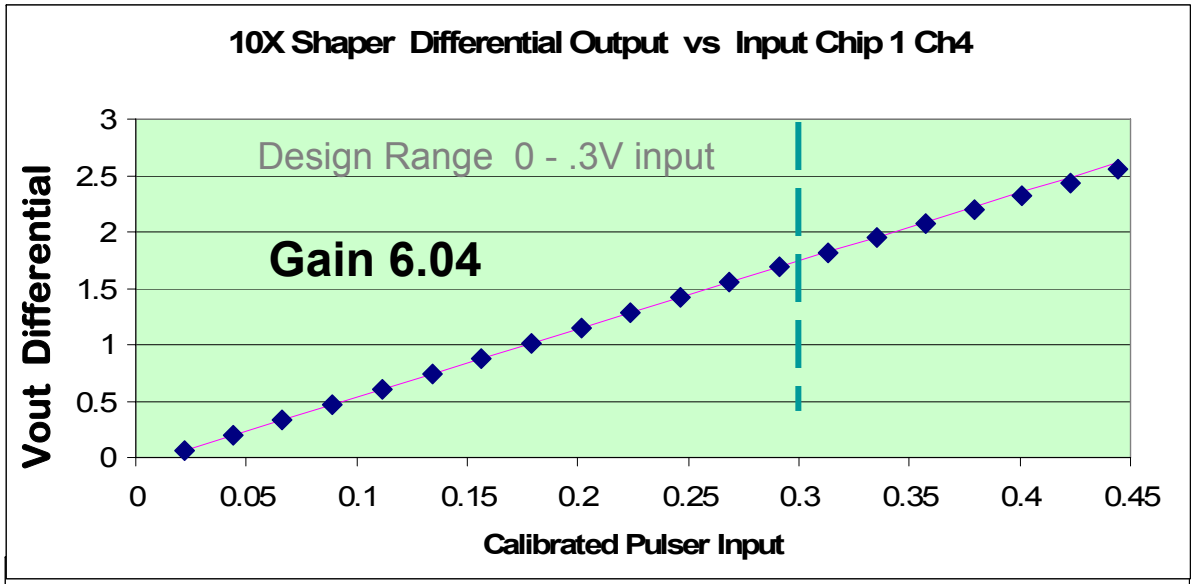
1X and 10X Shaper Output #2

14.1mV and 153mV peak 38ns Rise

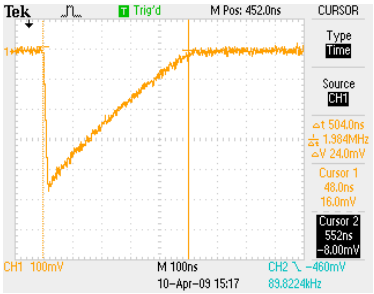


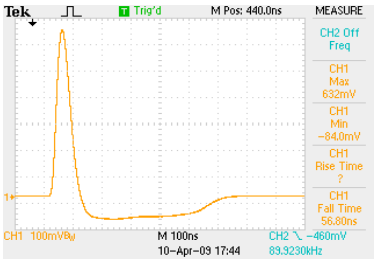
LAPAS ASIC Automated Linearity Measurement

Using AFG3252 & MSO4401

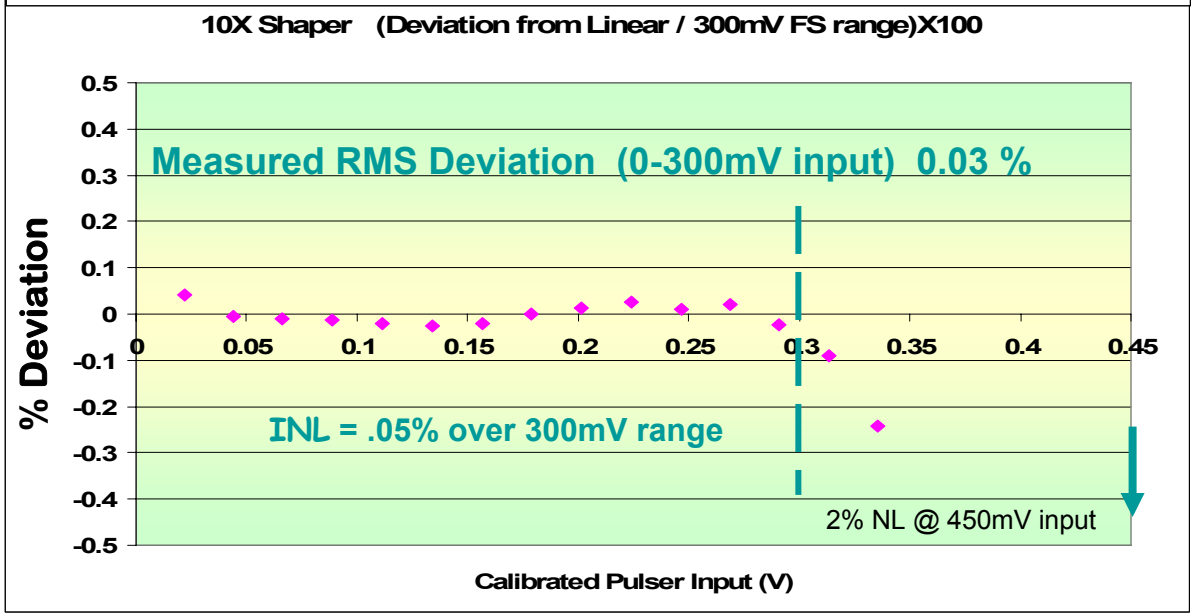


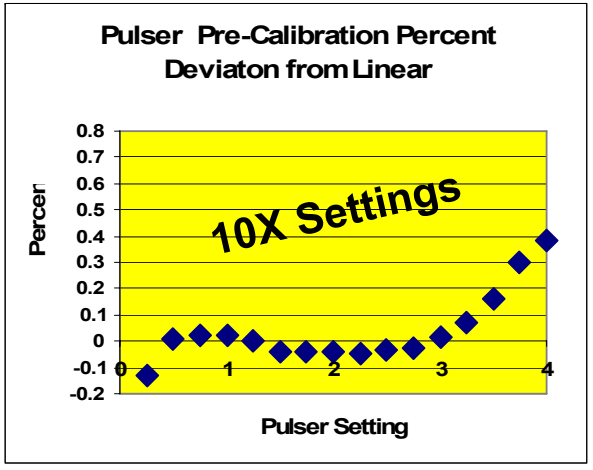
Shaper Input Signal





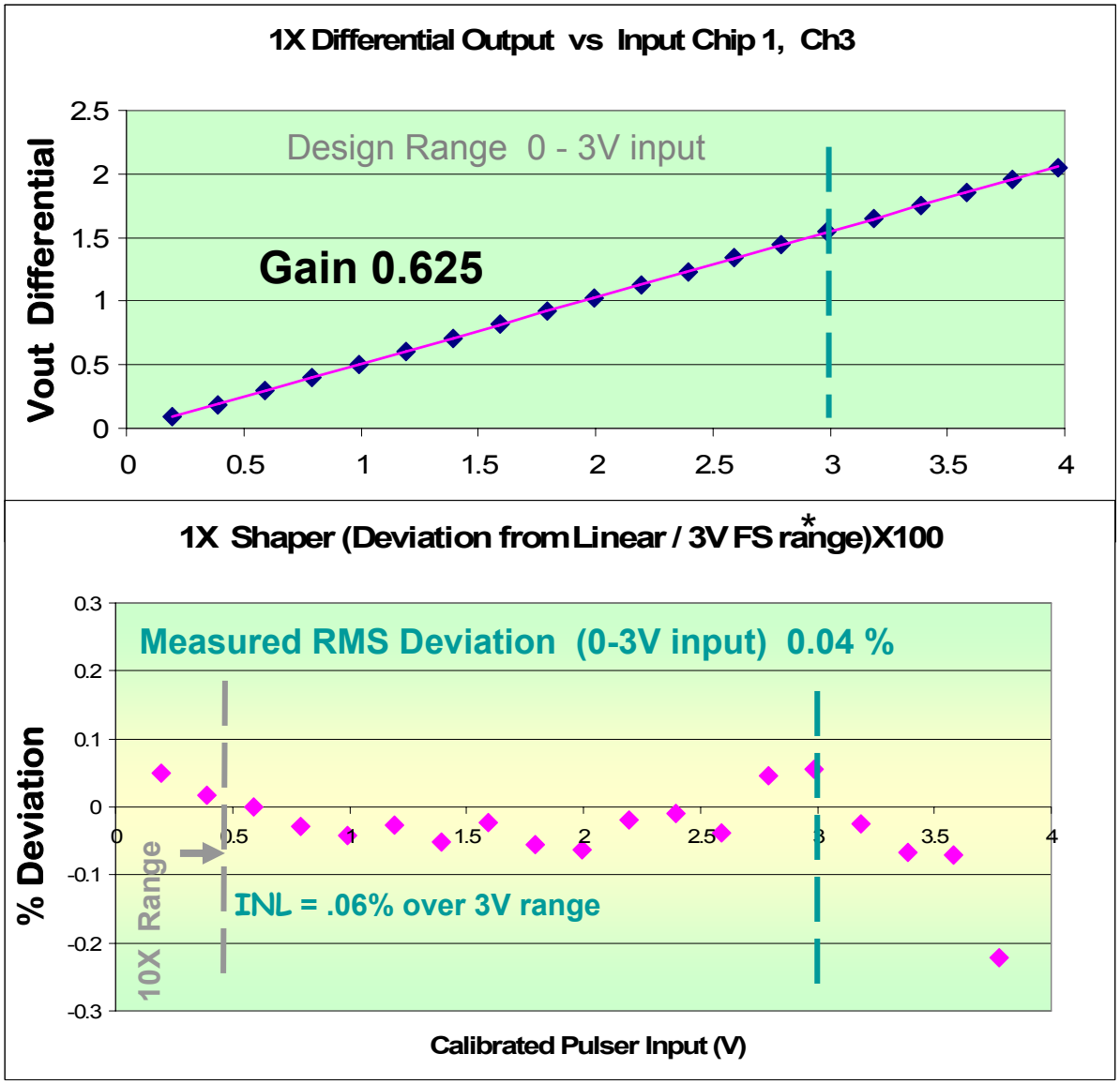
LAPAS Shaper Output



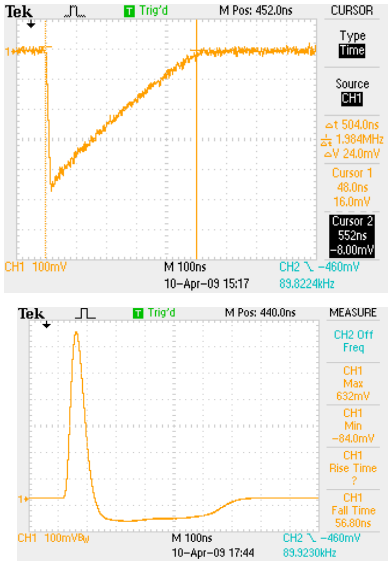


LAPAS ASIC Automated Linearity Measurement

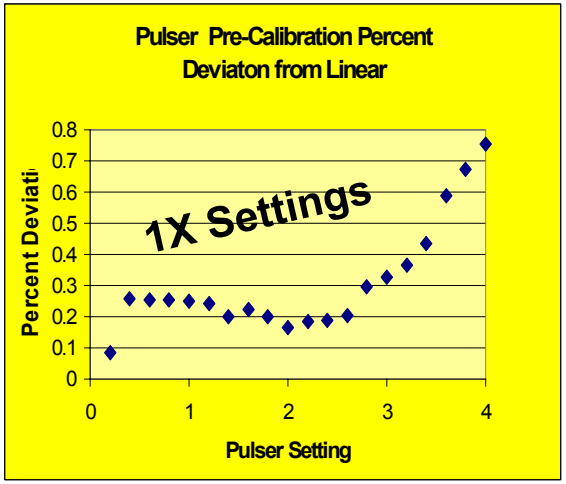
Using AFG3252 & MSO4401



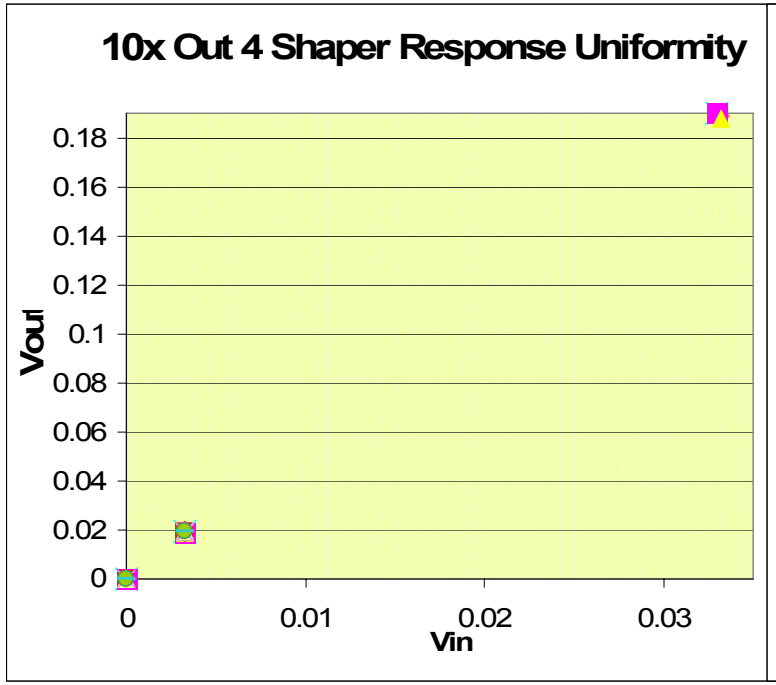
Shaper Input Signal

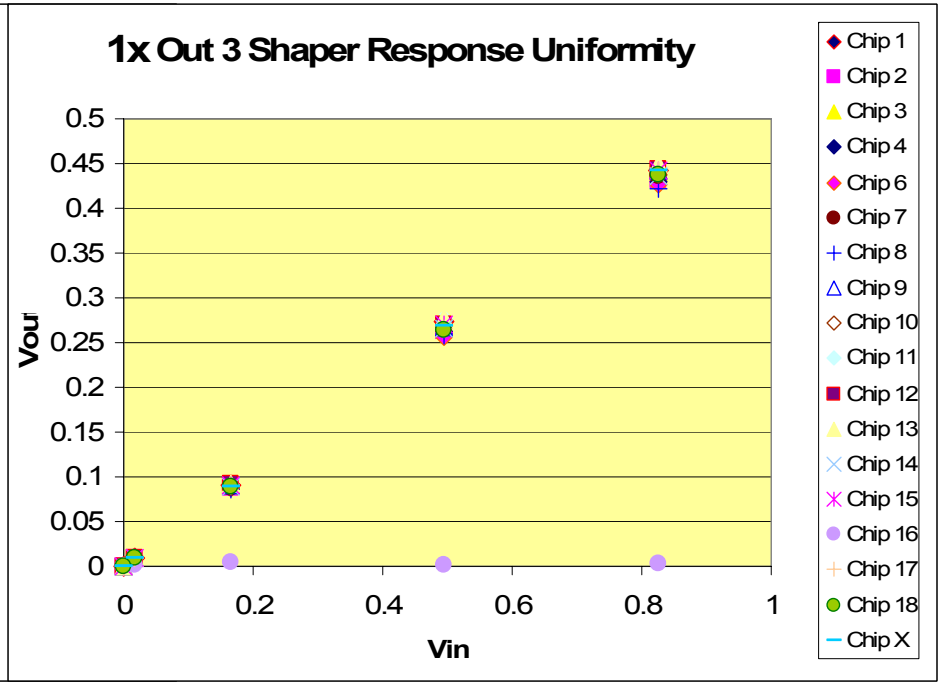


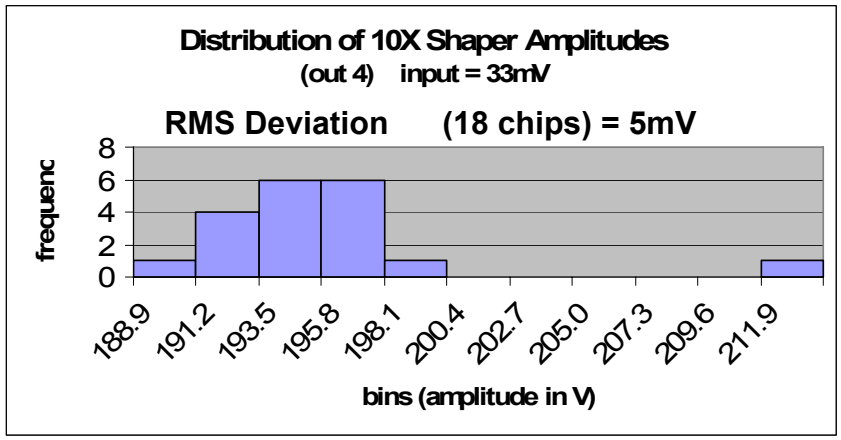
LAPAS Shaper Output

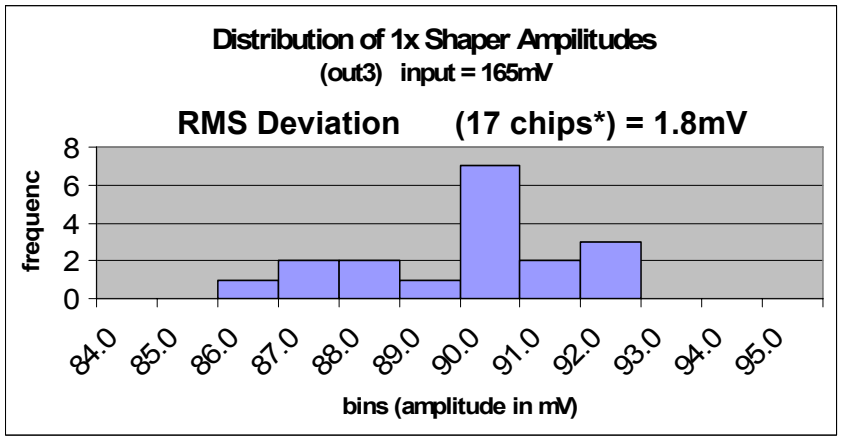


Shaper Uniformity across all tested Chips







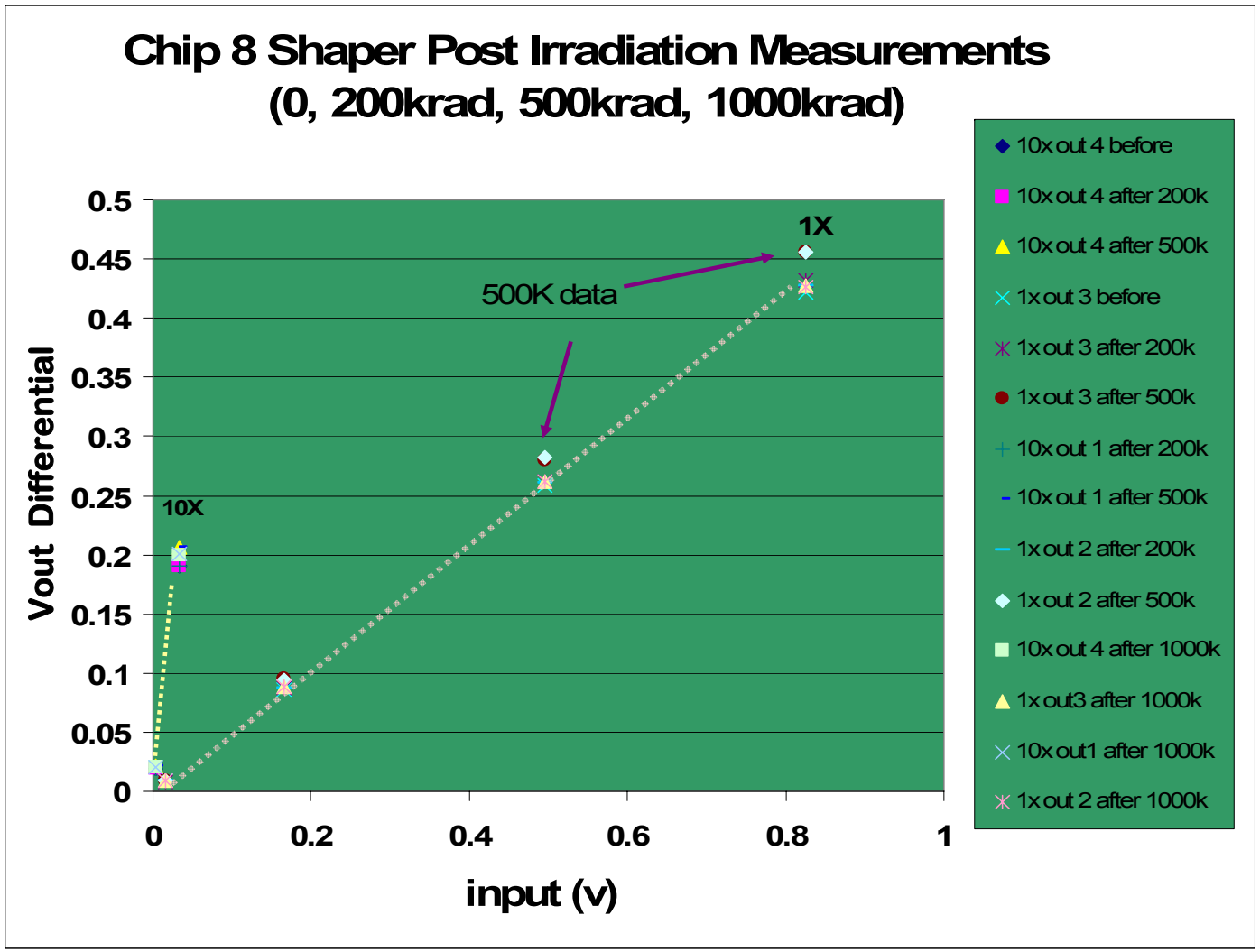


* Chip #16 removed

Gamma Irradiation

BNL source used to irradiate 3 LAPAS ASIC's to 1MRad in three steps

Possible increase in 500Krad gain not inconsistent with change in pulser shape or amplitude.



Conclusions With Hand Wired Prototype

- DC results very close to Simulations.
  - Transfer gain (Vout / Iin) Measure 5.1K Nominal Sim 5.2K
  - Peaking time 37ns as predicted.
- Preamp Transient response Good Ch 3,4 .
  → Need to understand Ch1, Ch2 oscillation.
- No Shaper Control Tuning reqd.
- Shaper Transient response, Good.
- Common Mode Auto-Tracking Excellent.
- Meas. Shaper Noise (10x) ~130uV of 3V Output range.
  ENI ~ 34nA (11% of total noise)
- Integral Non Linearity → Less than .1% over FS 1X and 10X
- Dynamic Range → As Designed.
- Ch to Ch uniformity → Better than 5% across 17 tested ASIC's.
- Shaper Power = 26.2mA*5V = 130 mW (combined 1X , 10X channel)
- No significant concerns about first Ionizing Radiation results.

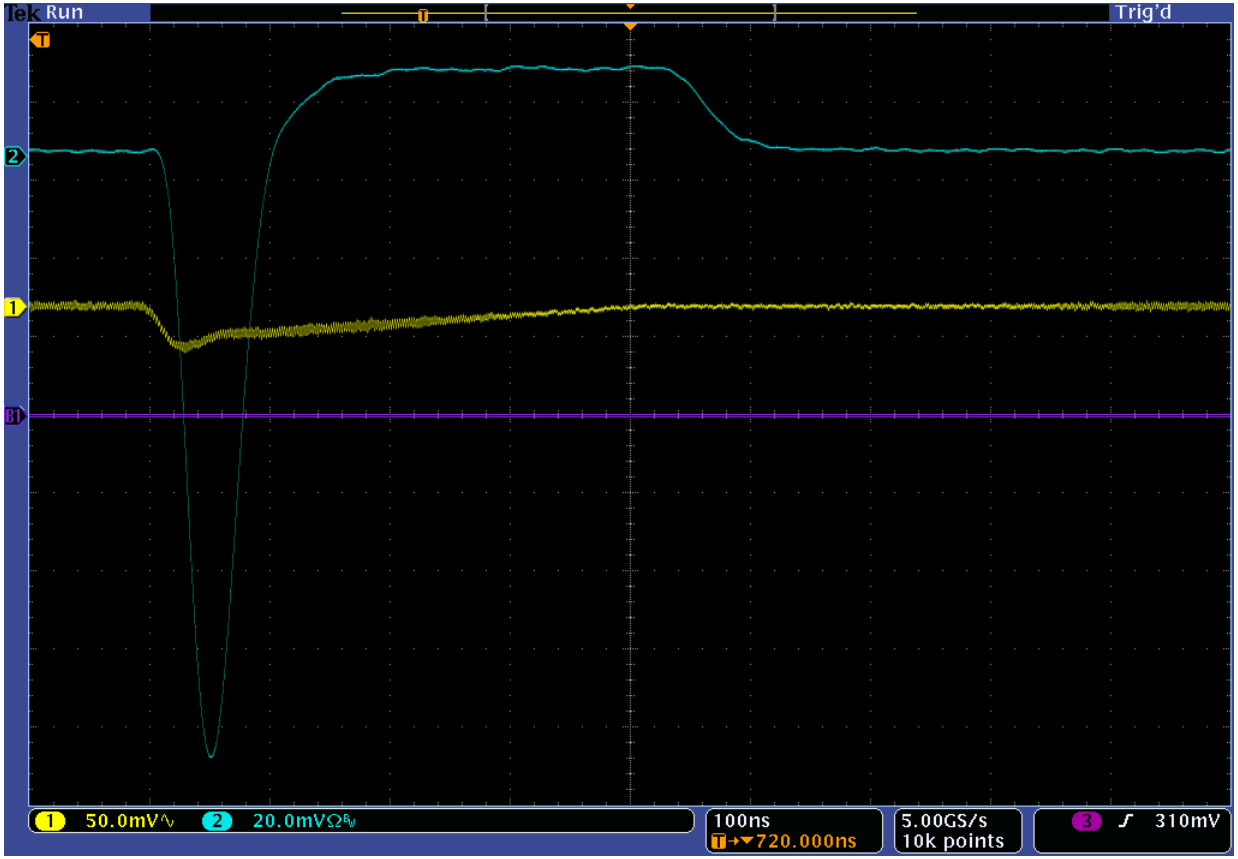
Next Steps for Prototype Evaluation

- **PC Board being Stuffed → Reduce hookup parasitics to improve testability of preamp.**
- **Test Preamp with existing LAr FEE.**
- **Preamp / Shaper tests with Prototype ADC.**
- **Finish Radiation Hardness Evaluation (protons, neutrons).**

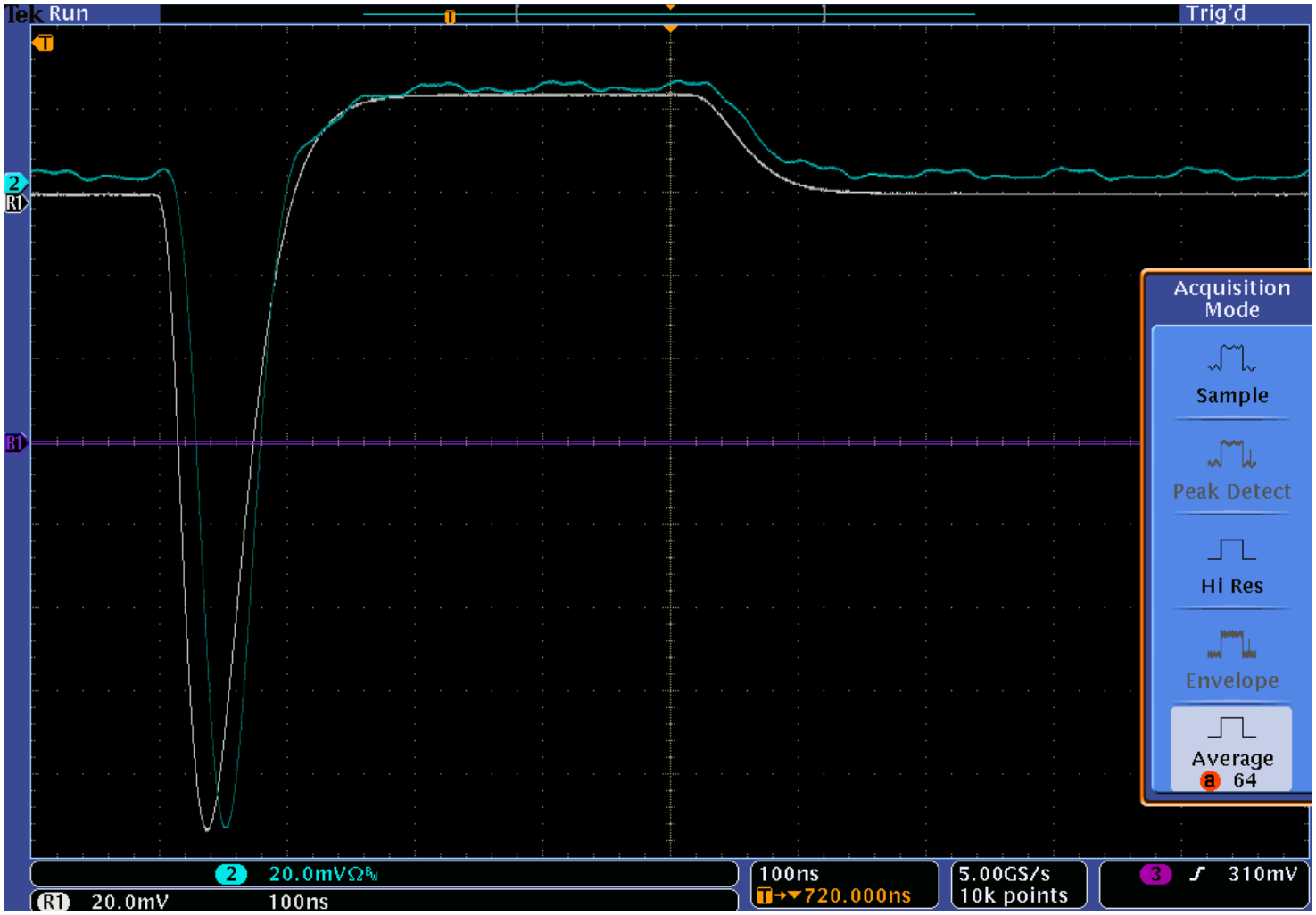
Support Slides…

Additional Measurements

1nF Detector Capacitance Preamp and 10X Shaper

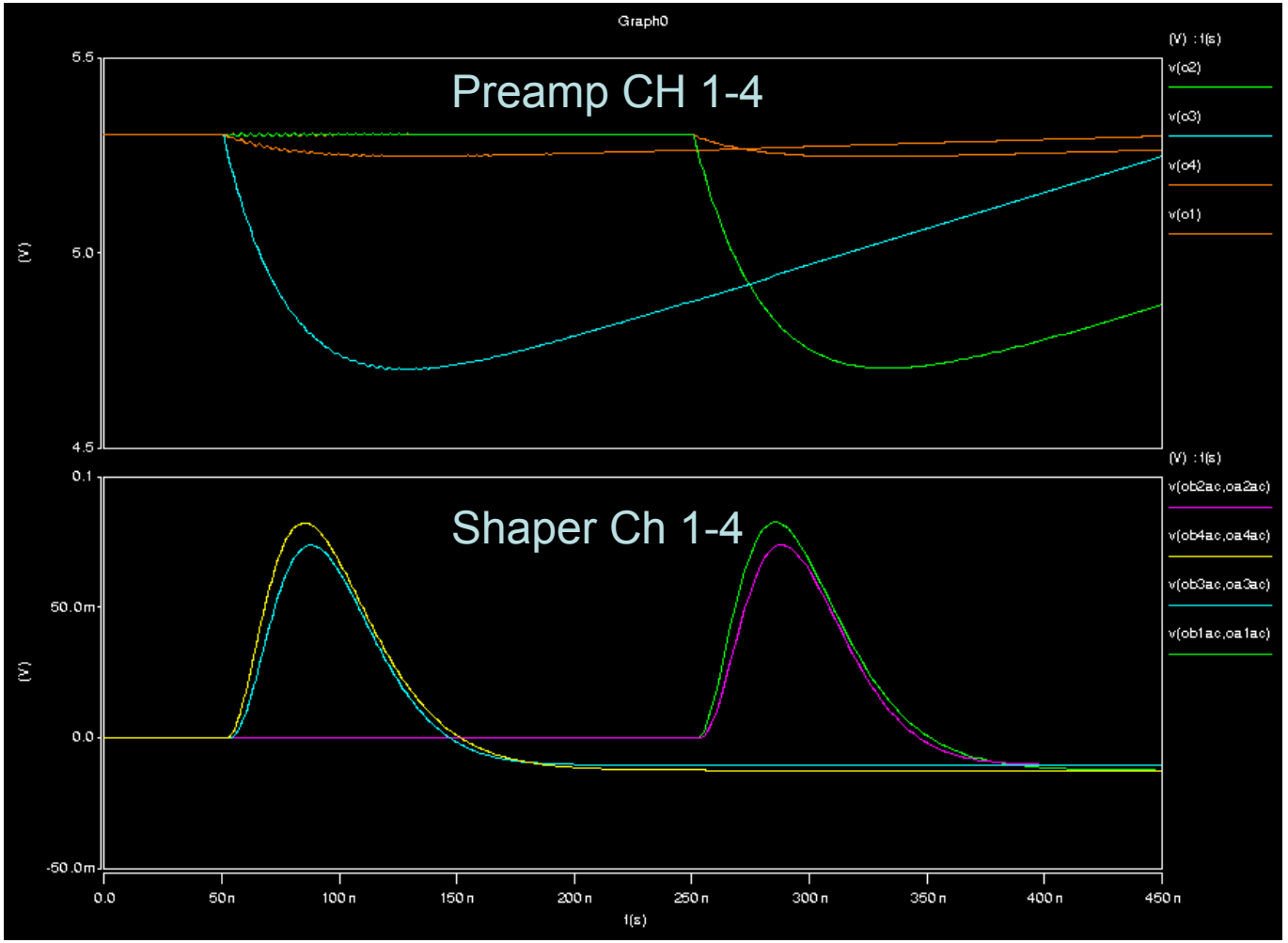


Preamp and Shaper Response
with 0 and 1nF Input Capacitance

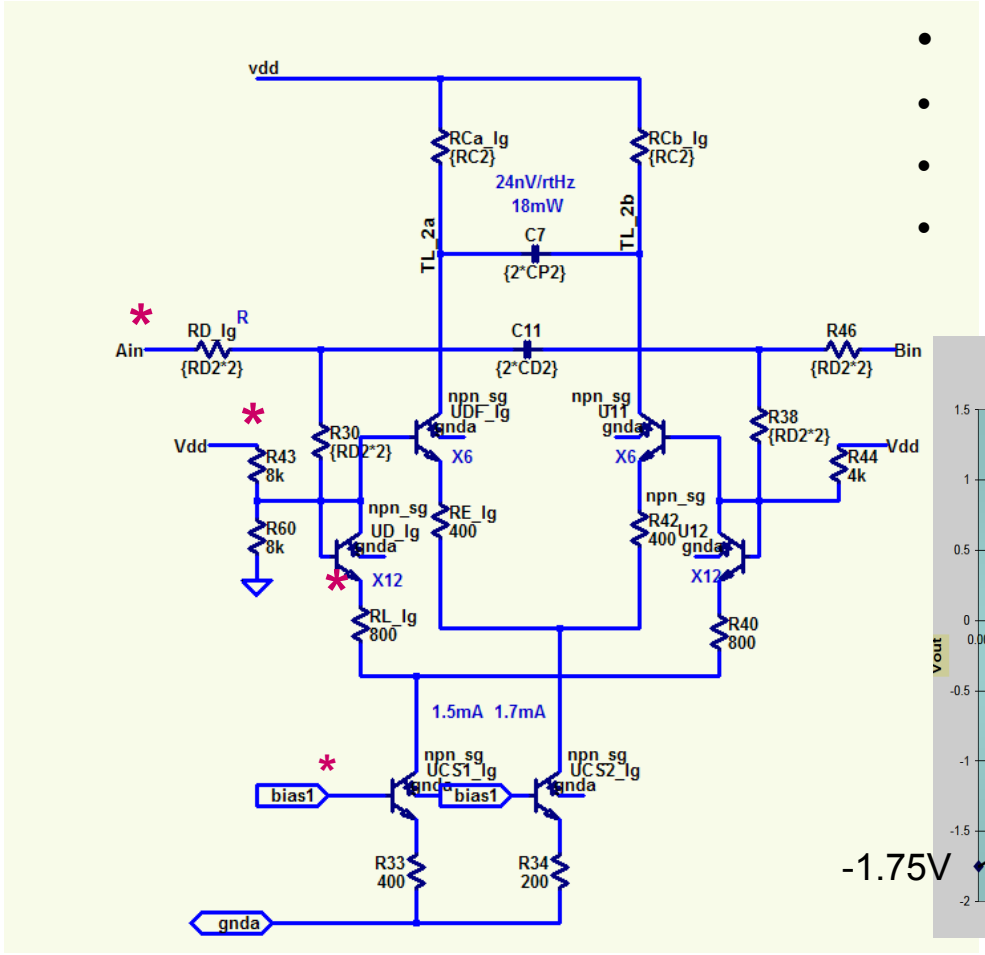


Extracted Netlist Simulation

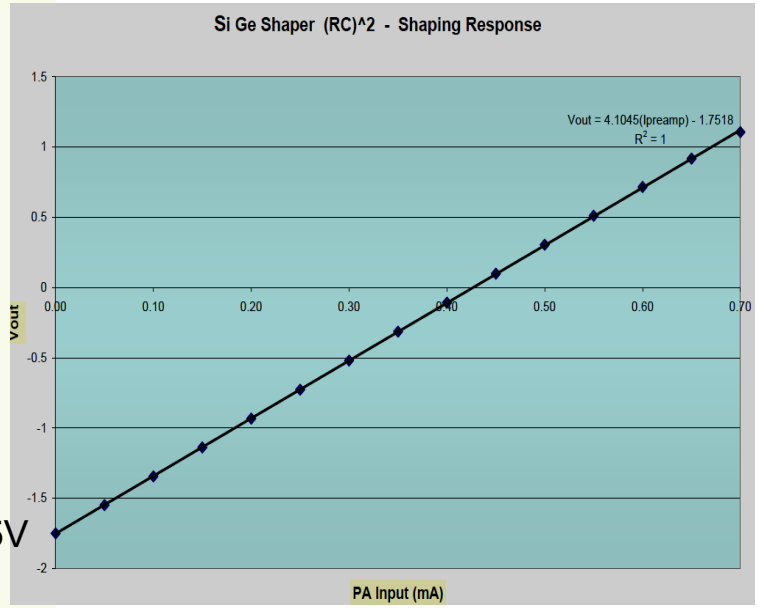
(1nf Detector Capacitance Included)



Translinear Shaper Structures



- **Low Power ~20mW**
- **Very Linear .2% over 2V output Range**
- **Low component Count**
- **Noise ~15nV/ √Hz, Too High for LAr**
- *** no simple targets to reduce noise**



1.2V

-1.75V

Process Variation MC

Extracted Netlist (no 1nF Detector Capacitance)