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Sensor development and readout prototyping for the STAR Pixel detector

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ABSTRACT: The STAR experiment at the Relativistic Heavy Ion Collider (RHIC) is designing a new vertex detector. The purpose of this upgrade detector is to provide high resolution pointing to allow for the direct topological reconstruction of heavy flavor decays such as the D^0 by finding vertices displaced from the collision vertex by greater than 60 microns. We are using Monolithic Active Pixel Sensor (MAPS) as the sensor technology and have a coupled sensor development and readout system plan that leads to a final detector with a $<$200 μs integration time, 400 M pixels and a coverage of -1$<$ η $<$1. We present our coupled sensor and readout development plan and the status of the prototyping work that has been accomplished.

KEYWORDS: Solid state detectors, Electronic detector readout concepts (solid-state)

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1 Introduction

The STAR Heavy Flavor Tracker (HFT) upgrade group is working to extend the capabilities of the STAR detector [1] in the heavy flavor domain by providing a tracking system that will allow for high resolution vertex measurements. This inner detector tracking upgrade is designed to enable the direct topological reconstruction of D and B mesons through the identification of decay vertices displaced from the primary interaction vertex by $>$60 μm [2]. This detector is named "Pixel" and is composed of two layers of high resolution MAPS. Pixel is the innermost and highest resolution detector of the vertex detector upgrades for STAR.

Achieving the required sub 40 μm extrapolated track impact parameter resolution in the Pixel detector is quite challenging in many ways. Multiple coulomb scattering constrains the detector to a design limit of $<$ 0.5% radiation length per layer in the tracking region. This small material budget needs to contain the MAPS sensors, a readout cable and a highly rigid support structure to maintain the position of the pixels, within an internal detector reference system, to a 30 μm envelope. In this stringent environment, the mechanical design requirements and sensor and readout electronics design are strongly coupled. Sensors thinned to 50 μm, air cooling, a 500 μm thick beryllium beam pipe, and aluminum rather than copper conductor readout cables become necessary aspects of the design. The expected final system design is an array of 40 sensor ladders with ten 2 cm $\times$ 2 cm sensors per ladder and parallel independent ladder readout systems. Each sensor is a 1024 $\times$ 1152 array of 18.4 μm square pixels giving the Pixel detector system a total pixel count of more than 400 M. The angular coverage of the Pixel detector ($|\eta| \leq 1$) is matched to that of the outer tracking detectors. A diagram showing the Pixel detector geometry is shown as Figure 1.

The final extrapolated track impact parameter resolution of $13 \oplus 19$ GeV/p$\cdot c$ μm is achieved by using the existing tracking detectors of the STAR experiment with the addition of a two layer silicon strip detector just outside of the Pixel detector. A cut-away representation of the set of detectors located at the innermost positions in STAR and showing their concentric cylindrical arrangement is shown in Figure 2. Tracking is performed from the outside of the STAR experiment inward to the vertex with increasingly higher resolution until the final resolution of 30 μm is achieved with the addition of the high resolution Pixel track points. We are pursuing an incremental approach

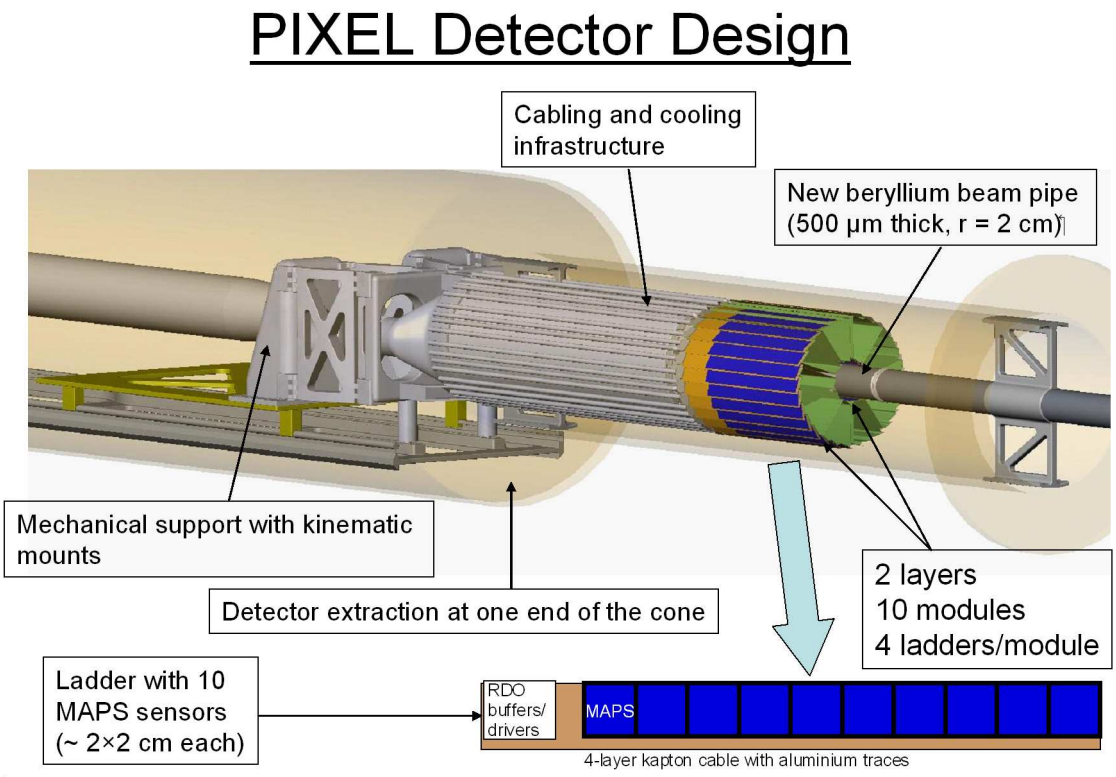

Figure 1. CAD model showing the STAR Pixel detector design. The green trapezoidal support tubes are thin carbon fiber composite. Ten MAPS sensors (shown in blue) are mounted on a readout cable and a carbon fiber carrier plate to form ladder assemblies. Ladder assemblies are placed in overlapping positions with three ladders on the outside and one ladder on the inside of each support tube. There are five support tubes in each half-detector assembly for a total of 40 ladders and 400 2 $\times$ 2 cm. sensors.

to reaching the final design by constructing prototype generations of sensors and readout electronics. The very challenging mechanical design of the detector is not included in the scope of this discussion but more information can be found in [3].

2 Coupled sensor and readout development plan

The Pixel detector group at LBNL is collaborating with the CMOS and ILC group at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg on the sensor development for the PIXEL detector. The sensor development plan for the STAR Pixel detector follows the sensor development plans of the IPHC group, who develop sensor technologies for various applications. The designs for the readout electronics are coupled to the path of the sensor technology. The sensor development path begins with simple multiplexed analog output sensors run in a rolling shutter configuration. For these early sensors, the readout system must contain ADCs for analog signal conversion and sufficient resources to perform all of the signal extraction and data reduction/zero suppression to allow for manageable data rates. The plan for sensor development is, with successive generations, to move the signal extraction and data reduction/zero suppression functions from the readout electronics onto the sensor itself. Thus, each newer generation of sensor moves functionality from the readout onto the sensor. This process is graphically shown in Figure 2.

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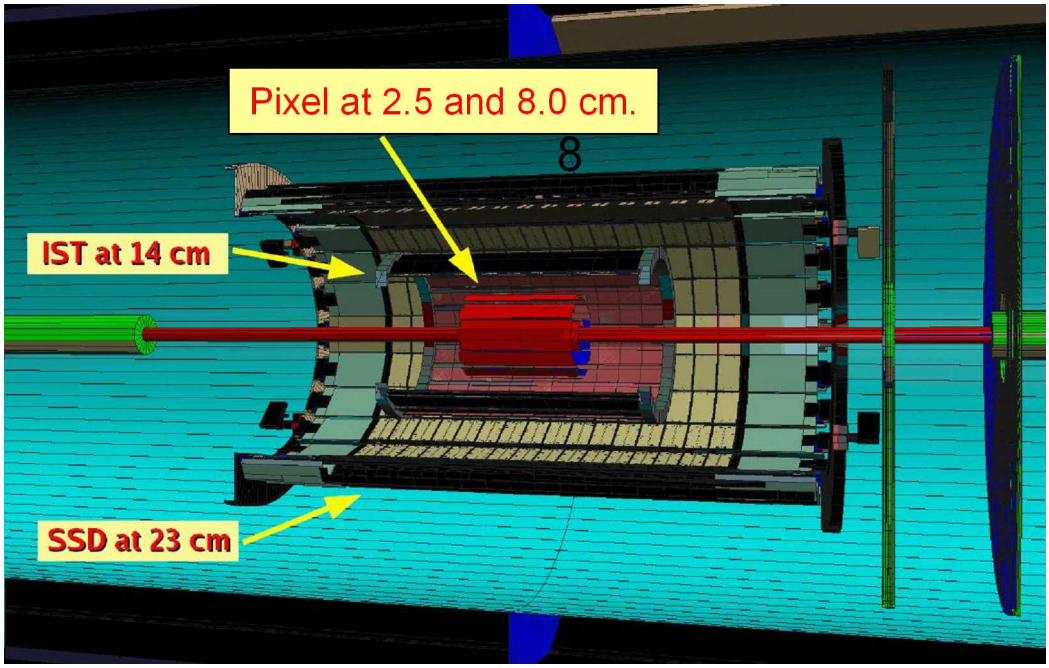

Figure 2. Cut-away drawing showing the planned detectors in the inner region of the STAR experiment. From inside outward, the Pixel detector is two layers of MAPS at radial distances of 2.5 and 8.0 cm. The Intermediate Silicon Tracker (IST) is a two sided silicon strip detector barrel at a 14 cm radius. The Silicon Strip Detector (SSD) is an existing two sided silicon strip detector located at a radius on 23 cm. These detectors are inside the central area of the 4 meter diameter TPC which is the main tracking detector for the experiment.

The sensor prototype development path for STAR begins with Mimostar series of sensor. This generation of sensors features multiplexed analog readout of parallel sub arrays processed in a rolling shutter configuration. These sensors have been produced and extensively tested.

The next generation prototype is named “Phase-1”. It is designed to contain on-chip Correlated Double Sampling (CDS) and column level discriminators providing digital outputs. This sensor will be used in a demonstrator prototype detector that will contain and test all of the mechanical and electrical final detector elements is a configuration that provides about 30% of the solid angle coverage of the final detector.

The final generation of sensor is named “Ultimate”. This sensor will be used to construct the full production Pixel detector. The Ultimate sensor contains all of the on-chip processing attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a $<$200 μs integration time and the addition of a run length encoding based data sparsification and zero suppression circuit.

2.1 Sensor design and status

The evolution of sensor development designs for the STAR Pixel detector begins with the Mimostar series of sensors and proceeds to the demonstrator prototype sensor denoted Phase-1 and culminates in the final sensor named Ultimate. The salient characteristics of each generation are shown in Figure 3.

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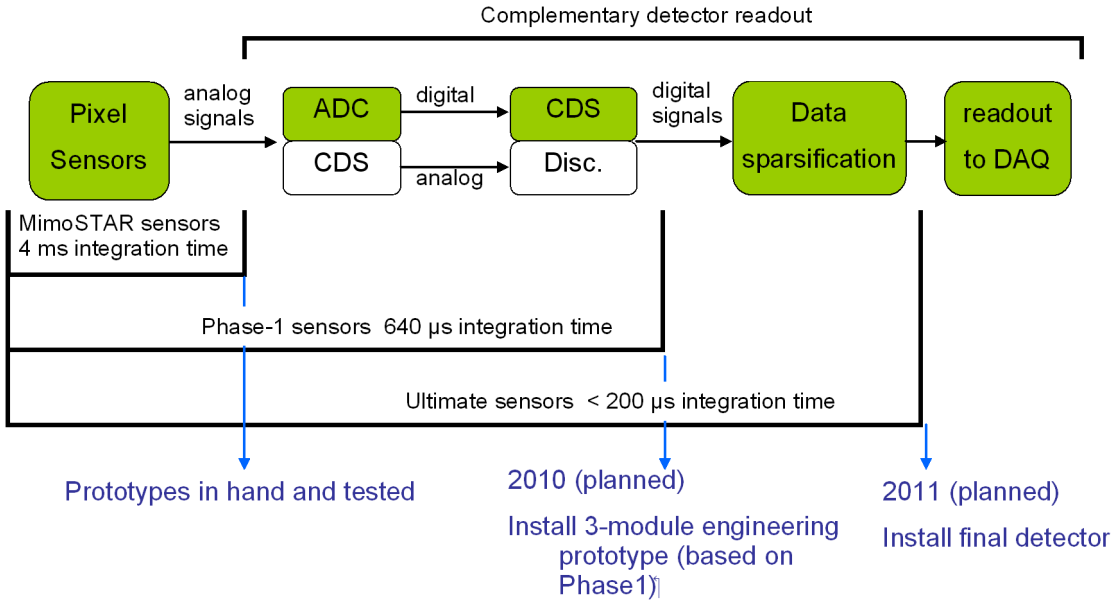

Figure 3. Sensor generation and attendant readout requirements for the STAR Pixel detector.

The first generation of sensors developed for the PIXEL detector was the Mimostar series. This generation of sensors featured 50 MHz multiplexed analog readout of parallel sub arrays processed in a rolling shutter configuration. The prototypes were based on 30 μm $\times$ 30 μm pixels with a self-biased charge collecting node (a reverse biased charge collecting, n-well/p-epi diode with the operating point defined through a forward biased p+/n-well diode). The Mimostar-2 was designed as an initial small scale prototype with a 128 $\times$ 128 array of pixels. This sensor was tested with radioactive sources and minimum ionizing particles and found to give a most probable value of signal-to-noise ratio (S/N) of approximately 16 with a charge of 220 electrons collected in the central pixel of a cluster. Tests with prototypes showed that S/N$>$12 allows for more than 99.5% detection efficiency of minimum ionizing particles with an accidental rate of less than 10^{-4}. Three of these sensors were mounted in a telescope configuration and tested in the STAR detector during the 2007 bean run at RHIC. The results were very positive with measurements of the charged particle density and limited tracking through the telescope [4].

The Mimostar-3 has the same basic attributes as the Mimostar-2 but with the pixel arrays scaled up to half-reticle size (2 cm $\times$ 1 cm). The pixel array is 640 $\times$ 320 and the pixel size is unchanged at 30 μm. The fabrication yield in the initial production run was very low with the sensor failures exhibiting large number of dead pixels in the middle of the array. This error was traced back to faulty via connections between different metal layers. The non-contacting via issue was analysed and found to be related to the pixel cell layout in the 0.35 μm Opto technology used at the foundry. The problem was corrected by modifying two production masks and the latest production run shows excellent yield.

The next generation is named “Phase-1”. This sensor will be based on the Mimosa-8 and Mimosa-16 sensors [5] and will contain on-chip correlated double sampling and column level discriminators providing digital outputs in a multiplexed rolling shutter configuration. The Phase-1

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Table 1. Parameters for successive generations of sensors in the development path for the STAR Pixel detector.

	Mimostar	**Phase -1**	**Ultimate**
Pixel Size (μm)	30 × 30	30 × 30	18.4 × 18.4
Array size	128 × 128 (Mimostar-2) 640 × 320 (Mimostar-3)	640 × 640	1024 × 1152
Active area (mm)	4 × 4 (Mimostar-2) 20 x 10 (Mimostar-3)	$\sim$ 20 × 20	$\sim$ 20 × 20
Frame integration time = readout time (ms)	4 (extrapolated to 20 mm × 20 mm. sensor)	0.640	0.100 – 0.200
Noise post-CDS @30 C (e-)	12-15	12-15	12-15
Outputs / sensor	1 analog (Mimostar-2) 2 analog (Mimostar-3)	4 LVDS	2 LVDS
Operating mode	Multiplexed rolling shutter with all pixels read out.	Column-parallel multiplexed rolling shutter with all pixels read out and integrated CDS.	Column-parallel multiplexed rolling shutter with integrated CDS and data sparsification.
Output type	50 MHz Multiplexed analog signals.	160 MHz serial data stream of digital binary pixel information based on column level discriminator threshold crossing.	160 MHz serial data stream of digital addresses of hit pixels with run length encoding and zero suppression.

will be a full sized 640 × 640 array resulting in a full 2 cm × 2 cm sensor size. In order to achieve a 640 μs integration time, the Phase-1 sensor will be equipped with four Low-Voltage Differential Signaling (LVDS) outputs running at 160 MHz. The design for this sensor is complete and has been sent to the foundry for fabrication. The first delivery of wafers of this sensor design is expected in January of 2009.

The final sensor is named "Ultimate". The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a $<$200 μs integration time and the integration of a run length encoding based data sparsification and zero suppression circuit. The pixel size has been reduced to 18.4 μm × 18.4 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. The array is correspondingly larger at 1024 × 1152 pixels. There are two LVDS data output lines from the sensor and the data rates are low thanks to the newly included data sparsification circuitry. The basic sensor design will be validated by the Phase-1. An initial prototype [6] of the data sparsification circuit has been produced and tested and

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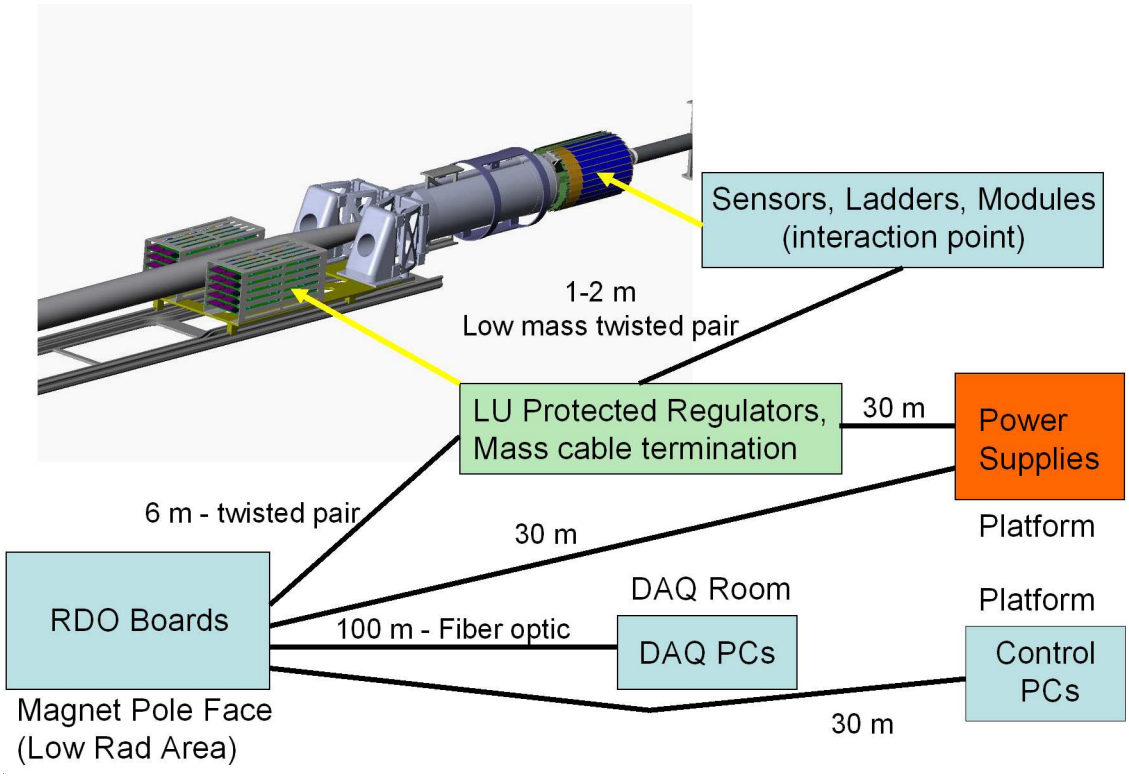

Figure 4. Physical layout of the readout system components for the Pixel detector.

will be integrated with the working Phase-1 design to give the final sensor. The first prototypes of this design are expected to be delivered in the 2010 time frame.

2.2 Readout design and status

The Pixel detector is an upgrade detector to the STAR experiment and thus must be designed to fit well into the existing infrastructure, particularly the existing trigger and Data Acquisition (DAQ) systems. In addition, the RDO system must deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC ($\sim$ 1 KHz for the STAR DAQ1K upgrade) and reduce the total data rate of the detector to a manageable level ($<$ TPC rate of a few hundred MB/sec). We will describe the readout system for the Phase-1 and Ultimate sensors. The analog Mimostar series data path has been previously described and documented in the reference [4].

The readout design is highly parallel and takes advantage of natural units in the detector design. Each independent readout chain consists of a four ladder "detector arm" unit with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of three detector arm units mounted with the final mechanical positioning structure and positioned with a 120 degree separation as the prototype demonstrator system to be installed in the 2010 timeframe followed by the full detector with all 10 detector arms in 2011. The readout system will be described for a complete system since the architecture is, by design, common to both the prototype and final Pixel system. A diagram of the physical layout can be seen in figure 4.

The basic flow of the data path starts with the APS sensors. The sensors are clocked continu-

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ously at 160 MHz and the digital data containing the pixel threshold crossing information is read out serially. The readout is continuous during the operation of the sensors on the Pixel ladder. The LVDS digital data is carried from the 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This electronics portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

Each sensor requires a JTAG connection for register based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to begin the readout. These signals, latch-up protected power and the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables (60 μm diameter wire) from the discrete electronics at the end of the ladder to a Power/Mass-termination Board (PMB). The total length of these low mass cables is approximately 1-2 meters. In addition to buffering the signals and providing transition from low mass fine wire to more robust cabling, the PMB provides regulated and latch up protected power to each ladder independently. The data is then carried to the Readout Boards (RB) located out of the high radiation area below the magnet pole-tip. There is one RB per Pixel carrier (40 sensors) giving a total of 10 in the system for the readout of $>$400M pixels. Each RB is composed of a commercially available Xilinx Virtex-5 FPGA development board mated to a custom designed motherboard. The custom motherboard provides LVDS buffering into the FPGA, the STAR trigger input, and an interface for mounting the CERN developed fiber optic Detector Data Link (DDL) [7]. The DDL provides the data link between the readout system and DAQ receiver PCs. The functional internal logic of the FPGA is shown in Table 1. Phase-1 sensor hit data streams are converted into addresses using a counter in the first stage of processing. The receipt of a trigger from the STAR trigger enables one event buffer for one full frame of readout. Hit addresses are stored in this event FIFO for event building and readout after the frame completion. Since Pixel is a relatively slow detector, its readout system needs to include capability for accepting multiple triggers during a readout frame. This is accomplished by having multiple event buffers and enabling them individually as triggers are received. The logic is nearly identical for the final sensor case. The data stream is already hit pixel addresses and is processed as described for the Phase-1 case. The zero suppression system is the main data sparsification system for the Phase-1 sensors and reduces the data rate from a raw value of 32 GB/second to a final rate of 240 MB/second at a 1 kHz trigger rate for a full detector. The flexibility of using FPGA based processing allows us to use the same hardware for both generations of sensor and make the necessary adjustments in firmware. A functional block diagram of the RDO board is shown in Table 1.

The reliability of the readout LVDS data path has been recently validated with a prototype readout system. LVDS 1-to-4 fan-out buffers were used to take the place of as yet unavailable sensors and were mounted on a mockup ladder built on FR4 PCB (0.031? thick) and sized and routed to resemble the final ladder design. The data path included up to 2.3 m fine twisted pair cable and 6 m of the robust twisted pair cable. The data transmission path was calibrated with a test signals and the latching time for each LVDS input was adjusted individually in the FPGA using the Xilinx IODELAY function [8] which allows for independent data input latching in 75 ps steps.

Three independent pseudo-random test patterns were sent continuously from the FPGA on the RB to the ladder and back to check for data corruption and possible cross-talk. The system was tested with signaling frequencies including the 160 MHz maximum data rate expected in the

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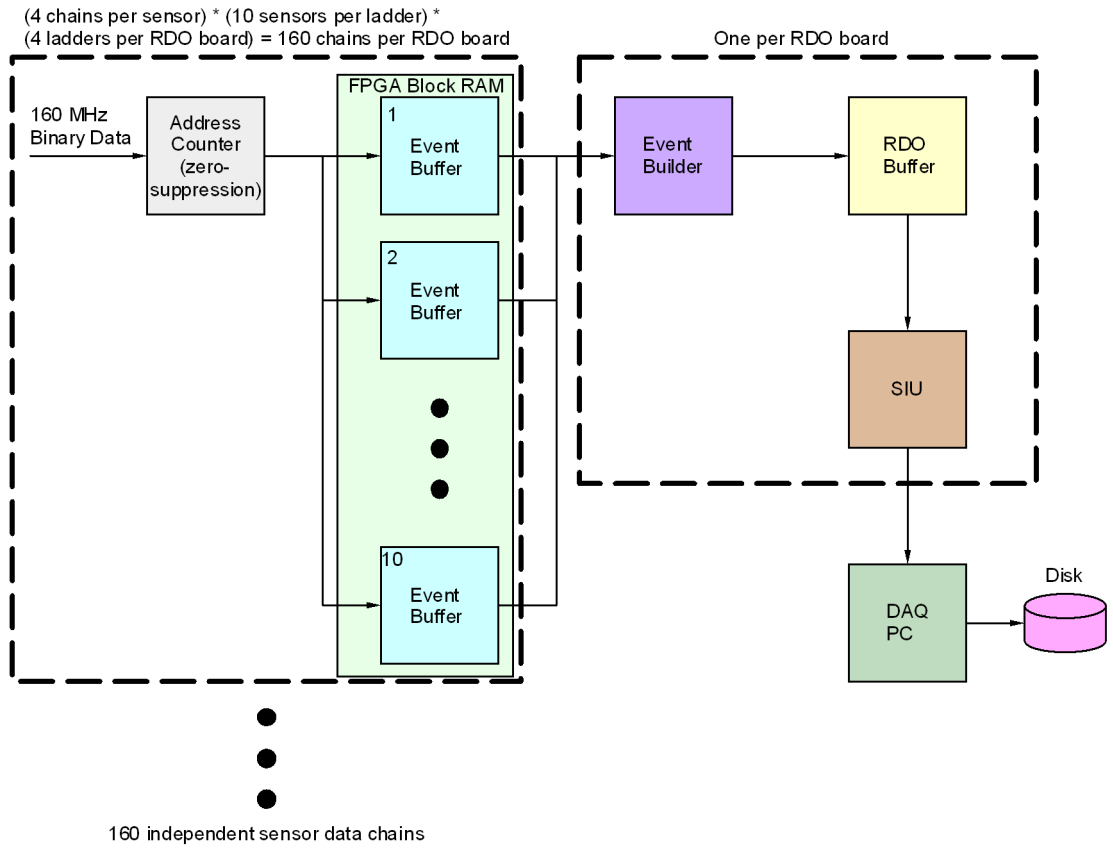

Figure 5. Functional block diagram of the Pixel readout boards showing the FPGA based address conversion and zero suppression, event buffering, event building and transfer to the STAR DAQ system using the Source Interface Unit (SIU) which is the detector end of the DDL fiber optic transfer system.

PIXEL readout system. The measured Bit Error Rate (BER) at 160 MHz was below 10^{-14}, which validates the chosen approach to the system architecture.

Based on this successful test we have constructed the first production prototype boards for the binary pixel sensor readout system. The RB is currently in test and will be used to test the Phase-1 sensors that will arrive in January 2009. The PMB prototypes and ancillary latch-up protected power board prototypes are also produced and in validation for the January system test. The design for the Al conductor flex cable is well advanced and we anticipate production of this component in mid 2009.

3 Summary and future development plans

The STAR Pixel detector group is working on developing a high resolution upgrade vertex detector for the existing STAR experiment. In collaboration with IPHC, we have a well advanced plan for sensor development starting with basic analog output sensors and evolving in a logically staged way to digital output sensors with on-chip CDS, discrimination and zero-suppression. The readout design for these sensors is strongly coupled to the sensor development path and is planned in such a way that the final readout system will, by design, be suited to both the prototype and final digital sensors.

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The analog output sensor generation has been developed, tested and characterized. The first generation digital sensor is based on currently working sensor technologies and has been designed and sent for fabrication. We expect to take delivery of the first wafers of this sensor in January of 2009. This sensor generation will be used in a prototype detector to be used in the STAR experiment in the 2010 run at RHIC. This prototype will allow for the complete testing of the mechanical, readout and STAR interface systems in addition to the sensor itself. This is planned to be followed by the final detector installation in 2011.

We have validated the design of the data path for the readout architecture with a full ladder mockup data path test. Based on this testing, we have completed the hardware design and construction prototype readout system. This prototyped system will be used for the future readout needs of the Pixel detector for the remainder of the development phase and for the final installed detector.

Acknowledgments

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[7] See, *DDL & RORC information page*, http://alice-proj-ddl.web.cern.ch/alice-proj-ddl/.

[8] See *Virtex*-5 *FPGA user guide*, http://www.xilinx.com/support/documentation/user_guides/ug190.pdf.

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