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Controller of a new pulsed source for Linac 4 (MEGADISCAP)

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Abstract

This document presents the implementation of a control system for a new multiple-stage pulsed current source converter. A new topology [1] that has been proposed to overcome some limitations inherent to capacitor discharge converter is presented in detail and explained. Its implementation is described and the design considerations adopted are accounted for. Besides, a control strategy is proposed, which has been implemented using an existing control board with some modifications on the acquisition system. A prototype whose current and voltage are scaled down with respect to those required for the converters that will be used for CERN Booster injection with LINAC 4 has been built. This reduced scale system has been simulated taking into account the control system implementation. Finally, the topology operating principle has been validated, the results obtained with the scaled down prototype have been compared with simulations and the need for more hardware resources for the control system implementation has been demonstrated.

1. Introduction

Pulsed power converters are used both to achieve high magnetic fields in extremely compact deflecting or focusing magnet loads and to perform particular short duration current or voltage pulse shapes in different devices used in particles accelerators [2].

Traditional capacitor discharge converters are composed of a capacitor bank that is first charged and then discharged in a magnet load. A resonant damped circuit is formed by the capacitor bank and the inductive load. Great improvement has been achieved in these converters:

- the use of a third harmonics circuit to increase flat-top length,
- the use of an active filter to increase flat-top precision,
- the use of a linear mode stage to modify pulse shape,
- the installation of an energy recovery circuit to reduce the power drawn from the mains,

However, these systems present the limitations inherent in their basic topology. To mention a few of them:

- these systems show lack of flexibility in the output pulse characteristics, the rise and fall times of the output pulse are imposed by the resonant circuit values. Besides, they are not capable of delivering long duration flat-top pulses.
- the power circuit of this type of converters is closely matched with the load. For many converters with different load values, the use of spare converters is not convenient.
- in many cases, capacitor discharge power converters reduce their efficiency because of the use of an energy destruction circuit that allows current amplitude variations from one pulse to another.

In many capacitor discharge power converters, thyristors were the choice for the discharge switches. This device was available with a large voltage and current range; it presented high current pulse ratings and, in case of an interdigitated gate, it was capable of producing fast turn-on commutations. However, its main drawback is the non-blocking capability that can be overcome by the use of special turn-off circuits. The development of semiconductors with a turn-off capability to cope with modern switching topologies shows that the thyristor market is becoming more and more limited and the range of devices commercially available is decreasing. In the last decade, gate turn-off components (like IGBT or IGCT) with increased current ratings have become available on the semiconductors market. In the field of pulsed power converters, these components offer new possibilities such as the use of switch mode topologies, energy recovery systems, switch-mode active filtering, etc.

This document describes the implementation of a new topology prototype (AB-PO-TN2008-05) that can be used to generate high current pulses with a high precision flat-top. These studies have been carried out in the framework of future accelerators that are foreseen to be installed at CERN (Booster injection with Linac IV, PS2, etc…). Even if this study is general, a specification is given to set the different requirements that have to be taken into account in the future. These global specifications are given in table 1.

Table 1
Pulsed power converter global specifications

Maximum pulsed output current	20 kA
Maximum load voltage	500 V
Flat-top duration	up to 10 ms
Current precision during flat-top	0.05%
Minimum rise and fall times	1 ms
Repetition rate	10 Hz

Concerning the characteristics of the load, septum magnet power converters that represent the most restrictive cases regarding the output current precision and range have been considered. For a single-turn septum magnet, the load inductance is generally of the order of a few microHenry and the magnet resistance is very small, thus:

$$L\frac{di}{dt} >> Ri$$

Considering this specific application (where the current magnitude is in the range of tens of kilo-amps and the load inductance and resistance values are low), the power supply is generally connected to its load using a matching transformer designed with a suitable

transformation ratio and installed as close as possible to the septum magnet. The matching transformer adapts the current magnitude to more practical current and voltage values for the power converter.

2. Power Converter

2.1 *Operational aspects*

In many cases (septum magnet, dipoles and quadrupoles in injection/ejection lines, etc, for accelerator operation), the essential aspects of the converter are the current stability and precision during the flat-top when the beam is circulating in the magnet load. The current rise and fall times are not critical as they do not influence the beam. However, it is important to minimize the output current R.M.S. value to decrease the losses in the magnet load and reduce its associated cooling. In fact, the main advantages of the use of pulsed power converters are to reduce the power drawn from the mains and to decrease magnet cooling requirements. Once these simple operational aspects are considered, the "ideal current waveform" to be delivered into the magnet load is trapezoidal: the maximum voltage is applied during the rise and fall times; so the output current R.M.S. value is reduced to a minimum. During the flat-top, the current is regulated with a suitable precision for the time period required by the beam duration. The corresponding current and voltage outputs of the converter are presented in figure 1.

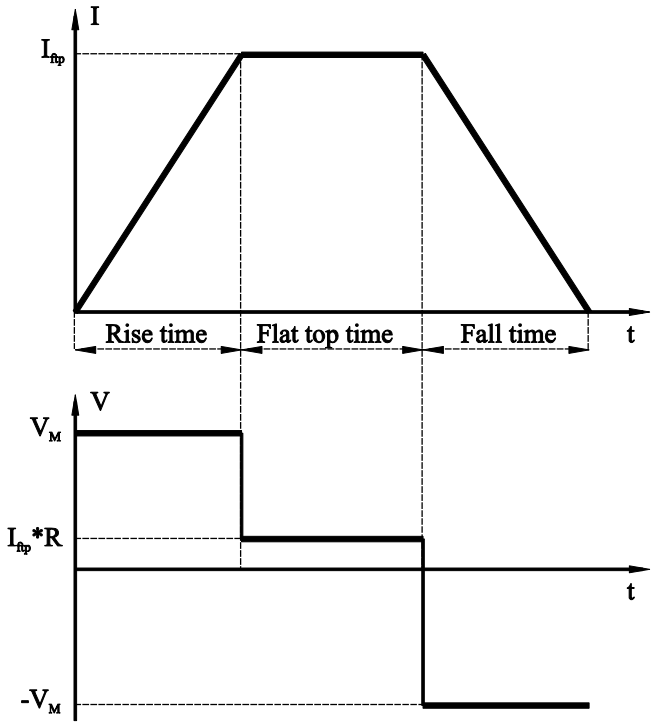


Figure 1: Load current and corresponding applied voltage.

The voltage and current waveforms shown in figure 1 correspond to an RL load, whose inductive component is higher than the resistive one. If the resistive part of the magnet load can be neglected during the rise and fall time and a DC voltage is applied on the load, the necessary voltage to reach the reference flat-top current can be calculated as follows:

$$V_M = \frac{I_{ftp} \cdot L}{t_{rise\_time}}$$

Table 2 below shows the load specifications seen from the matching transformer primary side. The application for which this power supply was designed makes use of a matching transformer ratio of 10.

Table 2

Power converter requirements used for design example

Matching transformer ratio	10
Maximum pulsed output current	2 kA
Load inductance seen at primary	1.1 mH
Load resistance seen at primary	0.150 Ω
Flat-top duration	2 ms
Current precision during the flat-top	0.05%
Repetition rate	10 Hz

From the specifications, the necessary voltage for the current to reach its flat-top value in less than 1ms can be evaluated:

$$V_M = \frac{I_{ftp} \cdot L_{load}}{t_{rise}} + I_{ftp} \cdot R_{load}$$

In this case:

$$V_M = \frac{2kA \cdot 1.1mH}{1ms} + 2kA \cdot 0.15\Omega = 2.5kV$$

As it can be seen, in order to meet the specifications, a primary voltage of 2.5kV is necessary for the load current to reach 2kA in 1ms during rise time. In the present design, the voltage of 3 kV is adopted. This value ensures a rise time of 0.8ms giving 0.2ms for the settling time.

These values indicate that semiconductors capable of operating at 2kA and 3 kV are required during the current positive ramping.

Once the current reference value is reached, a voltage equal to $I_{ftp}\ R_{load}$ must be provided to the load for the magnet current to be constant. To obtain this voltage, the converter should operate in a PWM mode with voltages above $I_{ftp}\ R_{load}$ (400V in this case) and currents of 2kA.

In this new structure, the rise time and the flat-top should be controlled separately because of the different requirements existing between them. During rise time the semiconductors must handle high voltage but no fast switching frequency is required; whereas during flat-top the semiconductors must operate at a lower voltage but with fast commutations times. For example, switches with 4.5kV and 3kA ratings could be used only to control the rise and fall times since they act as a single on-off switch.

It can also be noted that since 400V/2kA semiconductors devices available on the market do not provide the required precision by commutating at the necessary high switching frequency, an active filter that ensures the current regulation should be added to control the current during the flat-top. One difficulty to be overcome is the special control features that have to be implemented when the system switches between the different operating mode (rise time, flat-top and fall time)

2.2 *Topology*

Figure 2 shows a schematic of the proposed system made up of three stages and the load.

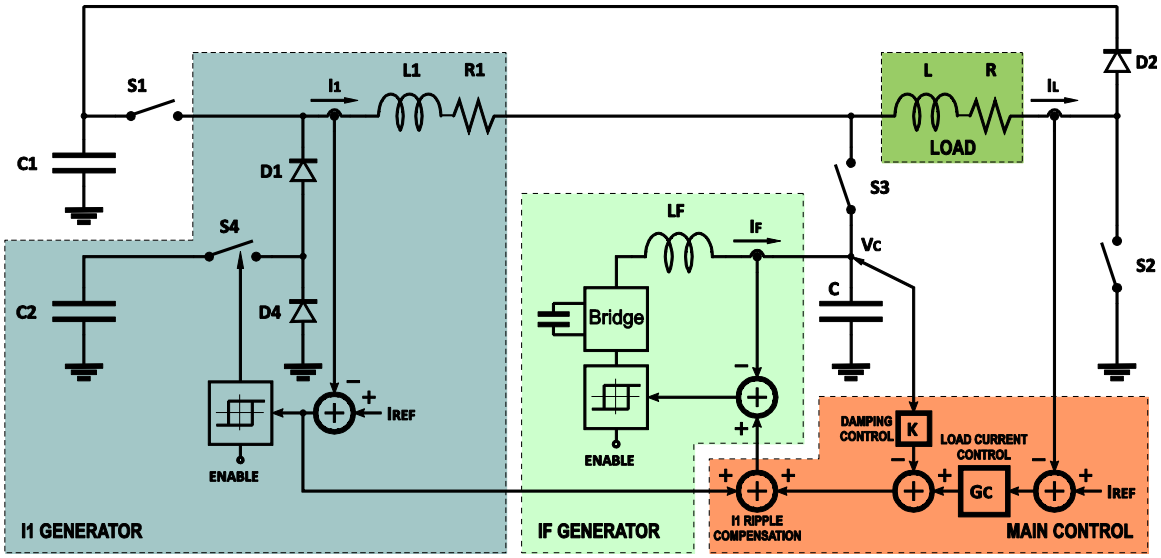


Figure 2: Proposed topology.

NOTE: In the proposed topology, S_2, common to all structures, is turned on during the rise time and flat-top, and turned off during the current fall time at the end of the pulse.

The circuit of stage 1 is composed of C_1, S_1, S_2, the auxiliary inductance L_1 and the load. When S_1 and S_2 are turn on, voltage V_{C1} is applied on L and L_1 so that current increases and the flat-top is reached at the desired time. For the rise time to be less than 1ms, V_{C1} should be greater than V_M. If the voltage drop on resistances R and R1 is negligible as regard to the high voltage on C_1, the following expression is obtained:

$$V_{C1} \geq V_M = (L + L_1) \cdot di/dt$$

Stage 2, composed of C_2, S_4, D_4, D_1, L_1, S_2, and the load make up the input I_1 generator, so-called GI_1. This generator is implemented with a one-quadrant inverter, and provides the load with the current mean value during flat-top. The maximum switching frequency of GI_1 is 10KHz. This frequency, limited by the technical limitations of S4, generates a higher current rippple in I1 than the required precision. To assure GI_1 generator control, voltage V_{C2} must be higher than the maximum value $I_{REF}(R+R_1)$ required during the flat-top. Diode D_1 is in charge of blocking the inverse voltage V_1 applied on switch S_4 when switch S_1 is turned on.

Stage 3 is composed of the GIF generator, the connection switch S_3 and the load. The GIF generator is implemented by a full bridge inverter in series with an L_F inductance, and it is controlled by a hysteresis modulator. Capacitor C is connected in parallel with the load so as to avoid undesired transients. Since diverse circuits connected to the same node behave as current generators, the use of the capacitor C is required.. The capacitor and the load form an LC filter which conveniently adjusts to eliminate I_F residual ripple.

GIF generator controls the magnet current through three feedback loops, as shown on the schematic block of the Main Controller.

The first control loop (Internal Loop) compensates I_1 current ripple. Such compensation is based on the error between the reference and I_1 current.

The second control loop (Damping Loop) is used to damp the RLC circuit response. This compensation is achieved by backfeeding V_C voltage through a constant K. K value is adjusted to obtain a critical damping.

The third control loop (External Loop) regulates the load current by means of G_C controller. This controller should compensate the second-order damped transfer, determine the system bandwidth and ensure flat-top precision.

Finally, the circuit formed by S_2, D_1, D_2, and D_4 is used for the current fall and to recover load energy. When S_2 is turned off, the load current flows through D_1, D_2, and D_4 recovering the energy stored in the magnet load to C_1. In this way, due to the high voltage in C_1, it is also possible to rapidly reduce the load current whenever a pulse ends.

2.3 *Operating principles*

Figure 3 defines the different system states during current pulse generation. Under state I (Standby), no current flows in the inductor, and the system waits for an external requirement. Under state II (Preparation), the system receives a pulse generation notice, and so pulse coefficients are updated, the hysteresis levels recalculated and the pulse external demand waited for. Under state III (Rising Slope), the system receives the pulse demand and so the pulse timer starts running and the current rises rapidly until reaching the required reference level. Under state IV (Flat-Top), the current attains the reference level and the system starts regulating. Finally, under state V (Falling Slope), the pulse time finishes and the system reduces the current level until it is extinguished.

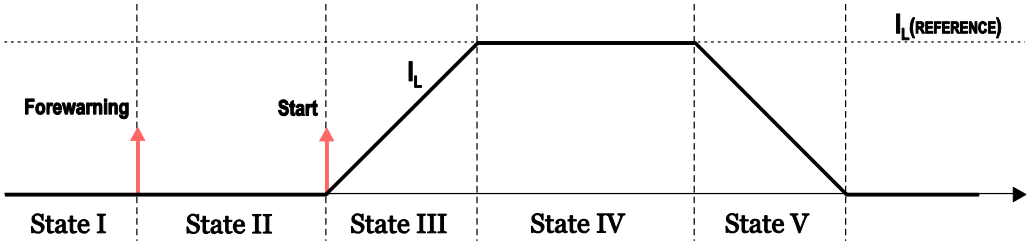


Figure 3: Temporal states within the current pulse.

An explanation of the system behavior in each stage is provided below.

- **State I: *Standby***

The system is off and in a standby mode. The switches are OFF and current does not flow.

- **State II: *Preparation***

Once the Forewarning signal is received, the system gets ready to generate a new pulse.

- **State III: *Rise Time***

During this state, S_1 and S_2 are ON while S_3 and S_4 are OFF. The enabling signal inhibits the operation of I_1 and I_F controllers. V_{C1} is the voltage applied on load L and inductance L_1. I_F generator and capacitor C are not connected to the load, and I_L current increases with a time constant given by $L+L_1$ and R. (Figure 4)

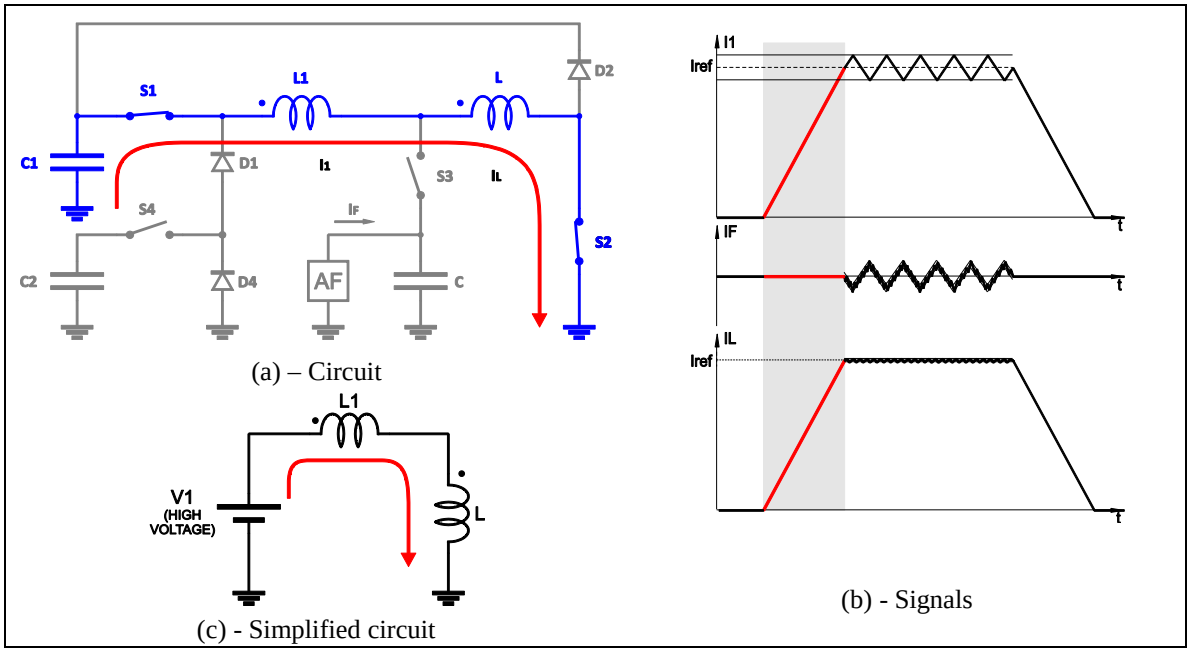


Figure 4: State III

Note: Given the fact that R+R1 is small, a linear ramping current has been considered.

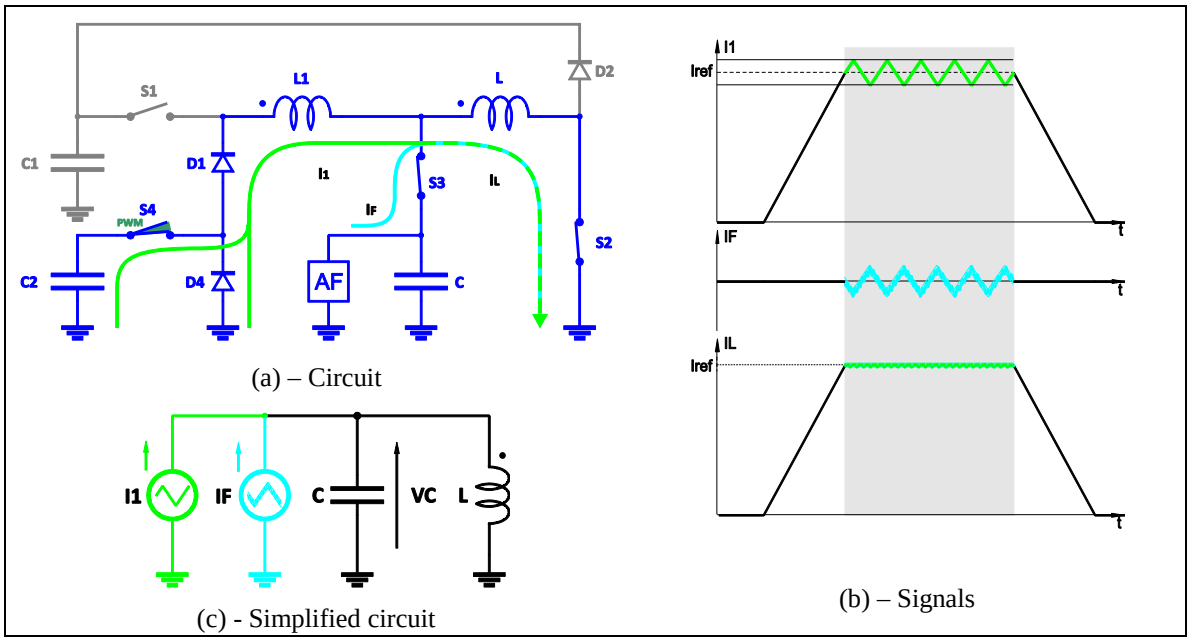


Figure 5: State IV

- **State IV:** ***Flat-top***

When the current I_L reaches the reference value, S_1 is turned off and S_3 is turned on. The opening of S_1 allows current I_1 to flow through D_1 and through the half bridge formed either by S_4 or D_4. If S_4 is closed, current I_1 flows through it and the voltage applied on L1 is V_{C2}-V_C. Otherwise, the current flows through D_4 and the resulting voltage is -V_C, where V_C is imposed by the voltage drop on the load resistance. Moreover, during this stage, capacitor C and GIF generator connect to the load by means of S_3, and the operation of I_1 and I_F controllers is enabled

(Figure 5). The action of the two current generators ensures that I_L value equals that of I_{REF} with design precision.

State V: *Fall Time*

To start magnet discharge, S_1, S_2, S_3, and S_4 switches are turned off. Current IL returns to the input capacitor C_1 through diodes D_1, D_2, and D_4. $-V_{C1}$ is the voltage applied on L and L_1 (Figure 6).

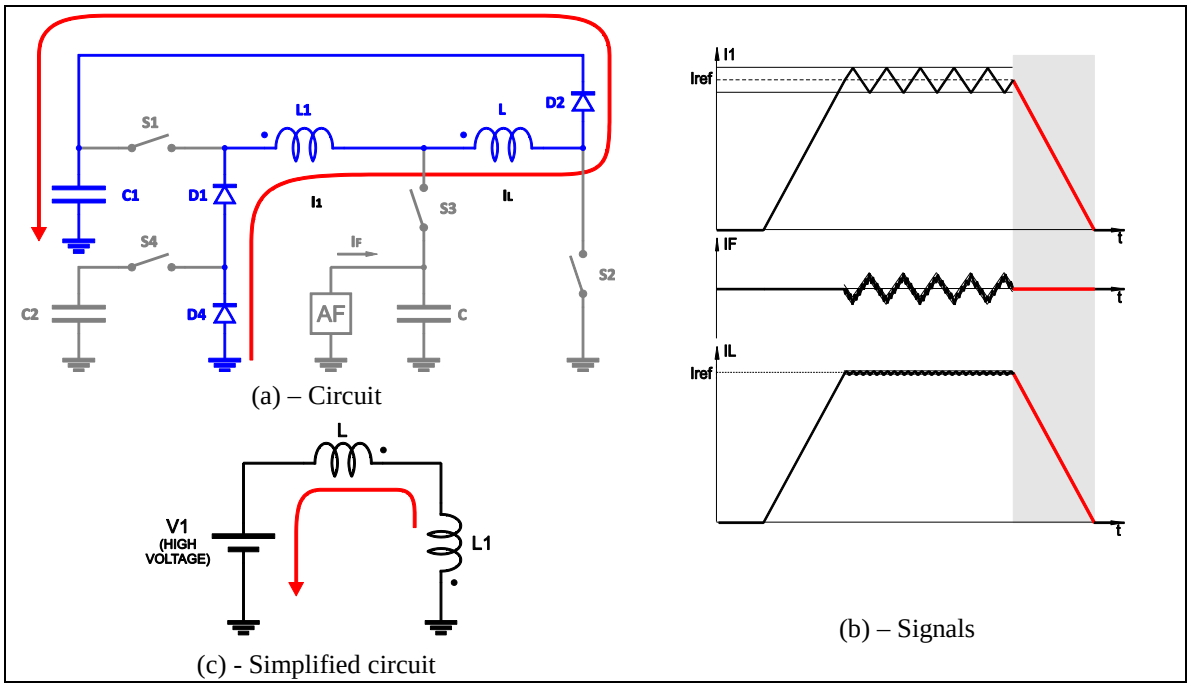


Figure 6: State V

Figure 7 summarizes the currents waveforms and the switches states throughout the different stages.

Given the fact that the circuit topology changes after each stage, special care should be taken regarding the conditions in which controller output are in each change.

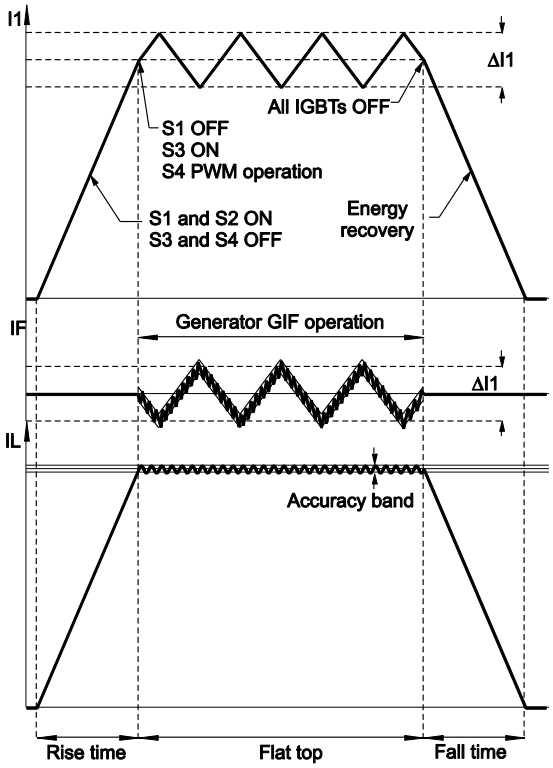


Figure 7: Current waveforms and switches states.

2.4 *Full model*

Figure 8 depicts the real system model as well as L and L_1 serial resistances and the real semiconductor switches. In the generators common coupling node, a D_3 diode is added to prevent overvoltage during the active filter disconnection. GIF generator is implemented with a full bridge (formed by IGBTs Q_1, Q_2, Q_3, and Q_4), an output inductor L_F and a floating source represented by C_3.

The clamp diode D_3 works along with the intrinsic diode in antiparallel with S_3. These diodes prevent the possible current imbalance between I_1 and I_L when the pulse finishes and the active filter is disconnected. If during disconnection current I_F is positive, it will continue flowing through S_3; otherwise, it will flow through D_3 until it becomes zero.

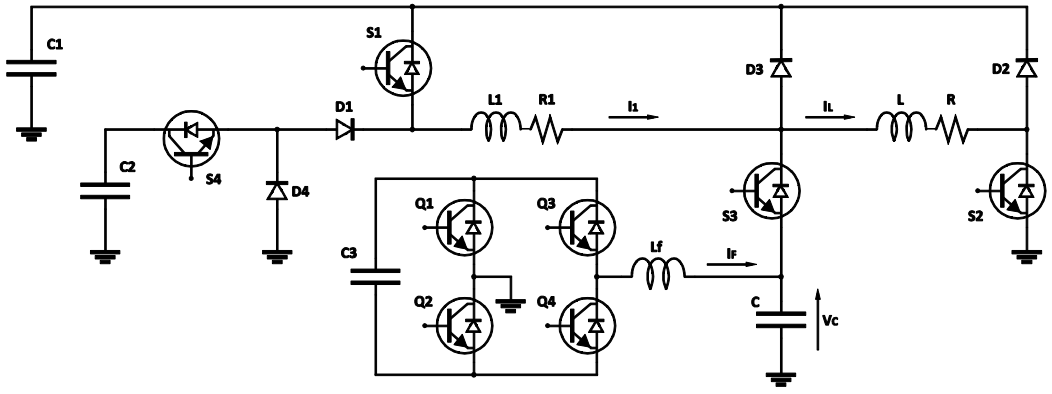


Figure 8: Complete system model.

2.5 *Power stage control*

2.5.1 I_1 Generator

The I_1 current control generator must ensure that the current ripple is within a defined range that can be compensated by the active filter. This control must also ensure stability considering the C_2 input voltage variations due to the capacitor discharge during the load current pulse generation.

In order to control current I_1, the hysteresis control seems to be the simplest and most robust technique to implement [3] [4]. Using this current mode control, the switches commutations are performed when the current error exceeds an assigned tolerance band. The current generator using hysteresis control mode is shown in figure 9.

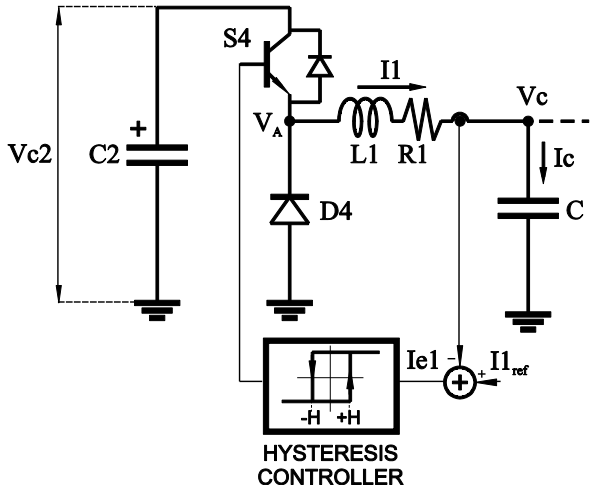


Figure 9: I_1 current generator with hysteresis control.

The block diagram corresponding to this circuit is displayed in figure 10.

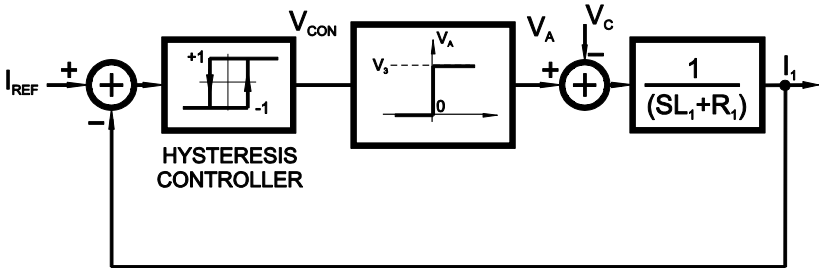


Figure 10: Block diagram of hysteresis current control.

If we consider the I_1 control system, one of the main concerns is its initial condition at the flat top beginning. One advantage of the hysteresis control technique is that it does not require the adjustment of the initial conditions when I_1 current generator is enabled. However, the disadvantage of this current control technique is not having a fixed commutation frequency. Its value depends on the voltage variations in the input, output and the variation in the reference signal.

2.5.2 I_F Active Filter

For the same reasons exposed in the design of I_1 generator, a hysteresis control is adopted to generate current IF. A schematic of the active filter with hysteresis current control is displayed in figure 11.

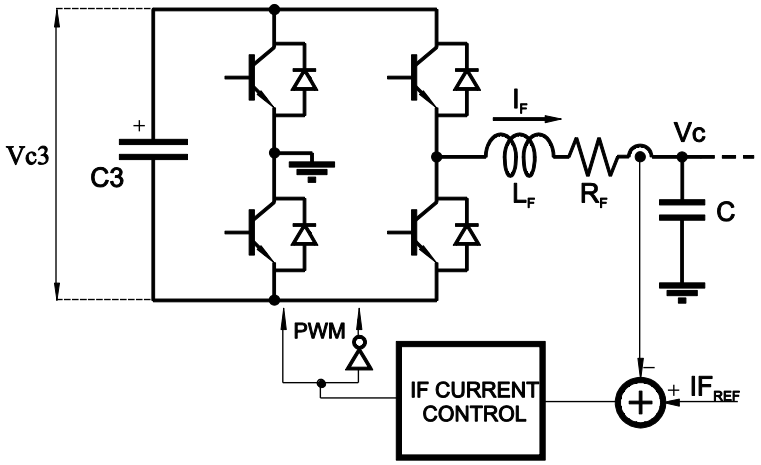


Figure 11: Schematic of active filter with hysteresis current control.

The enabling input of GIF controller, just as that of I_1 controller, is used to inhibit controllers operation during I_L current rise and fall. Figure 11 also illustrates the voltage V_C feedback necessary for damping. The block diagram corresponding to figure 11 circuit is shown in figure 12.

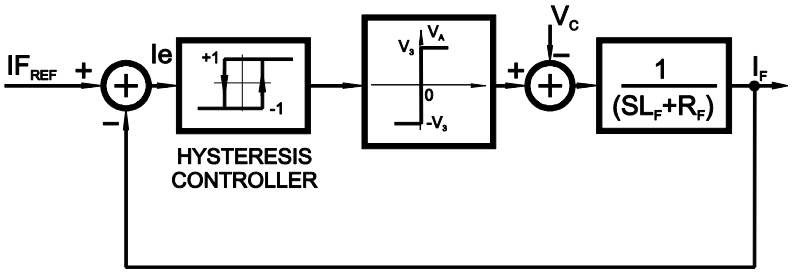


Figure 12: Block diagram of hysteresis current control.

The choice of the active filter commutation frequency is based on the bandwidth requirements, the semiconductor devices operation range and the driver's operation speed. As the active filter must compensate a current ripple of 10 kHz, its commutation frequency must be around 100 kHz.

The active filter is connected in parallel with capacitor C and because it operates during the flat-top, its output voltage is 300V. For the same reasons found in the design of the I_1 current generator, the filter input voltage must be above 300V to ensure I_F current control. A voltage of 400V is then adopted.

2.5.3 Main Controller

- ***Internal Loop***

In view of GI1 limitations, the ripple in I_1 is very high. This error should be corrected by the main control loop through GIF generator. To favor the main loop operation and, given the fact that the signal identifying the error is known, a feedforward is implemented. This signal, arising from hysteresis control, is triangular in shape and its frequency varies with a mean value of 10KHz. The Feed-Forward compensation simplifies the control loop task, which consists solely of correcting I_1 residual ripple.

- ***Medium Loop***

The connection of this capacitor with the load constitutes an RLC circuit that operates as a second-order filter, as shown in figure 13.

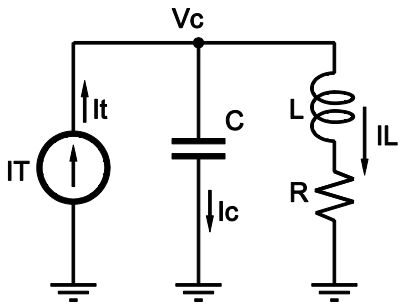


Figure 13: RLC circuit constituted by the load and the filtering capacitor C.

Due to the differences of the initial conditions between the capacitor voltage and the load current, oscillations in voltage Vc and in the load current I_L are generated. To damp the oscillatory response, a feedback of the filter variable states is performed. In this system, as detailed in AB-PO-TN2008-05, only voltage V_C can be feedbacked. Figure 14 depicts the complete control system in which the feedback loop used to modify RLC filter damping is highlighted.

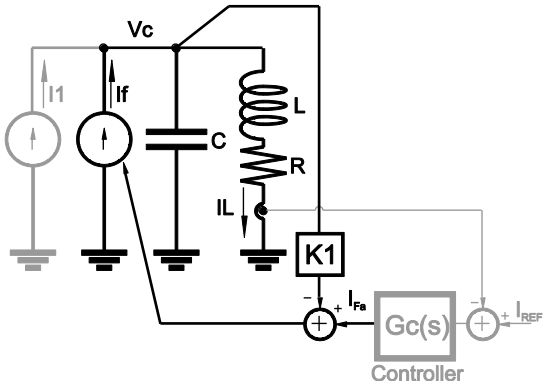


Figure 14: Damping of RLC circuit using voltage feedback.

To simplify the analysis, generator I_F is assumed ideal with a unity transfer function for all the analyses. This is based on the assumption that the generator I_F bandwidth is greater than the compensation system bandwidth. The block diagram for the control system is shown in figure 15

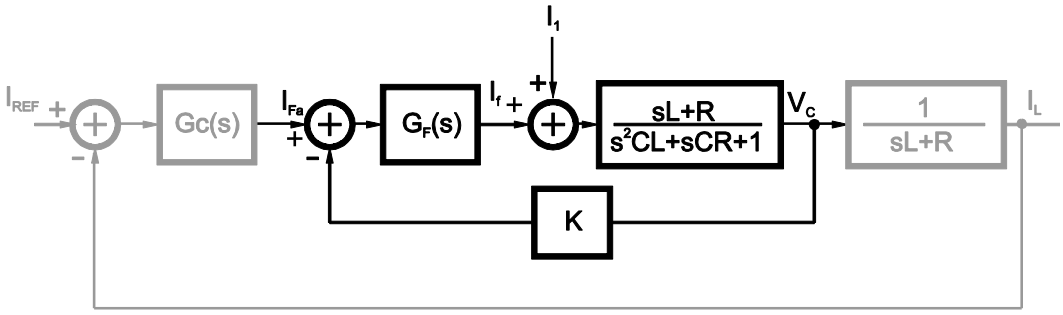


Figure 15: Block diagram of voltage feedback compensation

The way in which the feedback gain K of the damping loop is calculated is detailed below. Based on the block diagram above, it is possible to calculate the following transfer function of the damping loop.

$$G_{1C} = \frac{I_L(s)}{IFa(s)} = \frac{1}{CLS^2 + CR + KL\,S + (1+KR)}$$

By analyzing the denominator, the following expressions can be calculated to evaluate the cutoff frequency and damping factor:

$$\omega_0^{\,2} = \frac{(1+KR)}{CL}$$
$$\xi = \frac{(RC+KL)}{2CL\,\omega_0}$$

As shown in these expressions, neither the damping nor the cutoff frequency can be independently adjusted. However, given the magnitudes of the circuit variables, the term KR results lower than unity. So, it is possible to assume that the cutoff frequency does not vary with the feedback. Then, the value of K to obtain critical damping is:

$$K \approx \frac{2\sqrt{CL} - RC}{L}$$

The low-frequency gain of the damping loop is as follows:

$$\left.\frac{I_L(s)}{IFk_{REF}(s)}\right|_{S=0} = \frac{1}{(1+KR)}$$

The variation of low-frequency gain is indicative of the fact that an additional control loop is necessary to compensate the load current. This additional loop constitutes the third function of the active filter, which is analyzed in the following subsection.

- ***External Loop***

As previously seen, the compensation of the RLC filter is highly important to ensure a suitable transient response. However, it is necessary to incorporate a feedback loop to regulate the

load current and ensure it remains within the defined precision limits. The block diagram of the load current control loop is shown in figure 16.

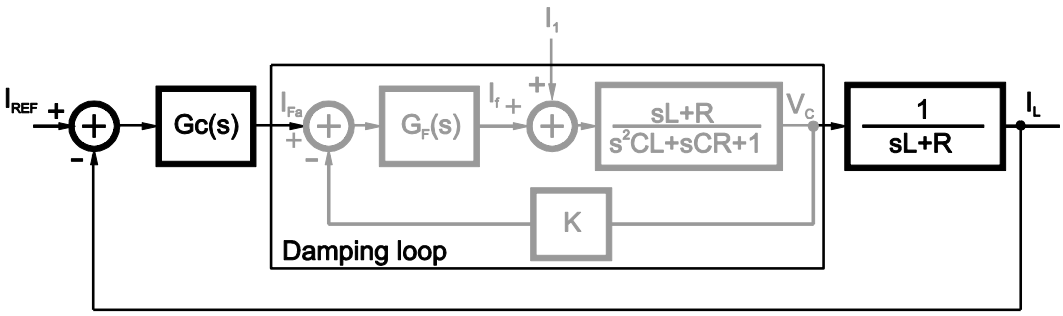


Figure 16: Block diagram of current control loop.

The design of the compensator is based on the specifications of bandwidth, phase margin, error, etc. The requirements for this control system are:

- Maximum close loop bandwidth: for a minimum transition time due to perturbations.
- Phase Margin above 60 degrees: to avoid overshoot in transient response and ensure the system stability.
- Zero steady state error for step input: to fix the load current steady state DC level at reference value.

One possibility is a controller transfer function with two zeros to cancel the real poles of the second-order system; one pole at origin to have a zero error in steady state and a high frequency pole for the system to be physically feasible. Assuming a critical damping, the suggested compensator is as follows:

$$Gci(s) = \frac{Kci \cdot \left(s + \omega_0\right)^2}{s\left(s + P_1\right)}$$

Where:

P: High frequency pole
ω_0: Zeros that correspond with the poles of the system Gc.
Kci: Compensator gain that is given by:

$$Kci = \frac{2\pi \cdot f_C \cdot P_1}{\omega_0^2}$$

fc: Cutoff frequency of the system.

Figure 17 shows the asymptotic Bode diagram of the system open loop transfer function and the controller transfer function. The values adopted for the compensator adjustment are:

- ω_C =2*π*10kHz
- P=2*π*40kHz
- ω_0 =2*π*3kHz

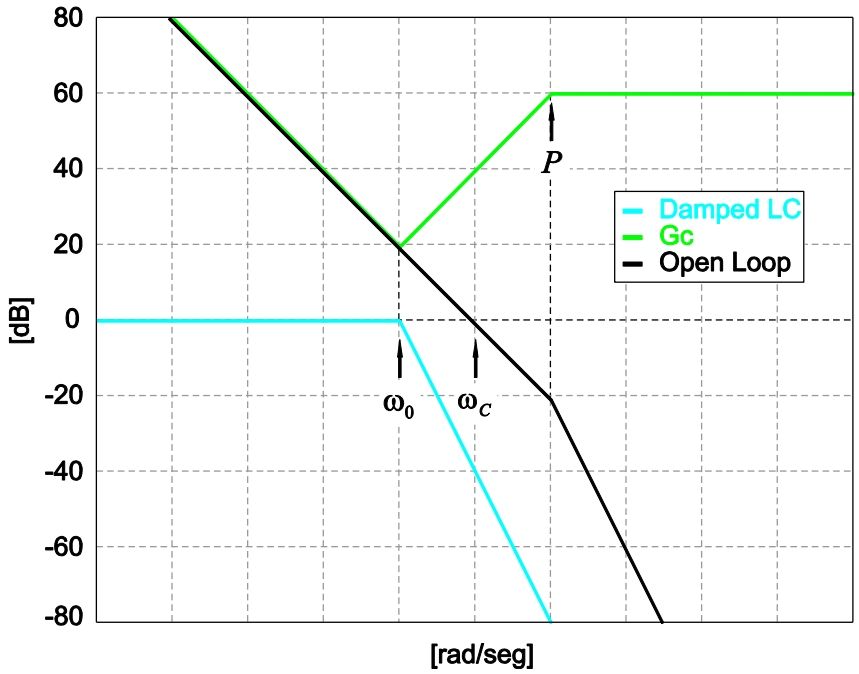


Figure 17: Bode of the current control loop.

So far, a new topology for the development of high precision pulsed current sources has been developed. A new stage of the project will now be described, in which the topology will be implemented to validate its functionality and assess its behavior. A digitally-implemented control board and a reduced-scale prototype are implemented to validate the topology and evaluate the possible changes and necessary improvements, thus reducing related risks.

In this work, the voltages and currents of the prototype are built at 1/100 scale; though loops commutation frequencies and bandwidths are maintained. The operation simulations of the prototype are performed with MATLAB. The main features of the components used are taken into account during said simulations, since the switches generally used differ significantly from the real prototype. Quantization effects and discrete control system rounding off are also taken into consideration, and so are the delays related to it. A review of the prototype implementation as well as of the related control system, also used to handle the equipment at a full scale, will be made.

Finally results will be presented and compared with those derived from the simulations. Conclusions will be drawn and the steps to be followed outlined.

3. Implementation of the control system

To consider a behavior closer to the analog model, data must be acquired at a high frequency consistent with the digital platform. To implement I_F digital hysteresis control, at least 20 samples per commutation cycle are used so as to limit the amplitude error in bands crossing detection.

As the maximum switching frequency is 100kHz, an acquisition frequency of 2Mhz is adopted. The VC damping loop is implemented in the FPGA and, being a simple operation, the maximum acquisition frequency of the channel is employed, i.e. 1MHz. The same approach is adopted for the I1 controller, as just one comparison is required; therefore, the acquisition frequency is set to 1MHz.

Regarding I_L control loop, a commitment condition between the acquisition speed and the complexity of the calculations to be performed is considered. A sampling frequency that enables

calculations with a minimum influence on the analog analysis is adopted. The resulting sampling frequency for this loop is 200kHz, twenty times above the cutoff frequency required for the system.

Since the operational requirements are covered by the EDA-01366-V3 board at CERN, the implementation is performed on such platform. The board features a Texas Instruments 100MHz DSP TMS320F2809 model, a Xilinx FPGA XCS40XL model with a 40-Mhz clock frequency, and an EDA-01729-V2 mezzanine board where the analog acquisition stage is mounted. However, the mezzanine board could not be used because its analog to digital converters did not fulfill the necessary requirements. Therefore, a new mezzanine board, composed of five 16-bit resolution ADC AD7621 converters, one of 2MHz and the remaining ones of 1MHz, and two 14- bits DAC AD5641 converters, both of 1MHz, was designed and built.

The following aspects are analysed below:

1. Description of the implemented system considering its functional blocks and features.
2. Description of the functionalities of the new acquisition mezzanine board.
3. Description of DSP operation and its interaction with the rest of the system.
4. Description of the blocks implemented in the FPGA.
5. Description of the modifications made in the control board.

3.1 *IMPLEMENTED SYSTEM*

A description of the main blocks comprising the system and their interactions is provided. These are divided into three main groups: the EDA-01366 Control Board, the Power stage and an external block called Control CPU; the latter generates the synchronism signals for the pulses generation and communicates their parameters. Figure 18 shows the block diagram.

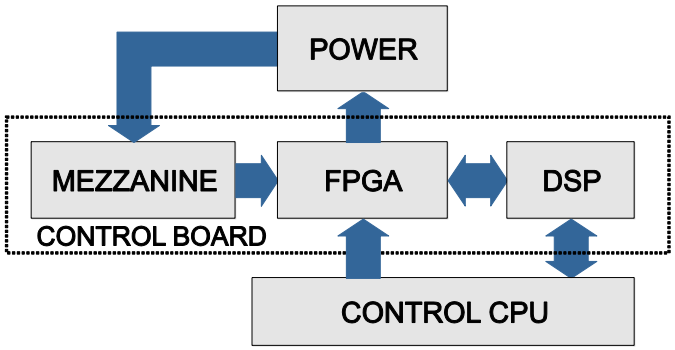


Figure 18: Block diagram of the implemented digital system.

Control CPU block: it generates synchronous pulses and transmits the pulse parameters (width, duration, etc) to the system.

Power stage: it includes the semiconductors and their drivers, the passive devices, power buses and the signal acquisition circuits. Section X details the implementation of the prototype built. As the full-scale prototype is under construction, the characteristics of its design will be reported in future works.

Control Board: it commands the switches of the Power stage in accordance with the CPU demands and the system measurements. This section is composed of FPGA, DSP and Mezzanine blocks. Communication with the CPU is achieved through a bidirectional serial channel, via DSP, and the two synchronous signals, called Forewarning and Start, via FPGA.These signals are sent from the CPU control unit to the Control Board. The Forewarning signal indicates the control that it should get ready to generate a new pulse; whereas the Start signal requests the control to generate the pulse.

Figure 19 shows the task distribution in the Control Board. The analog signals coming from the Power stage and the test output signals coming from the DACs are shown on the left; whereas the switches Control signals and the communication lines with the CPU can be seen on the right. A more detailed diagram is provided in Appendix 6.1

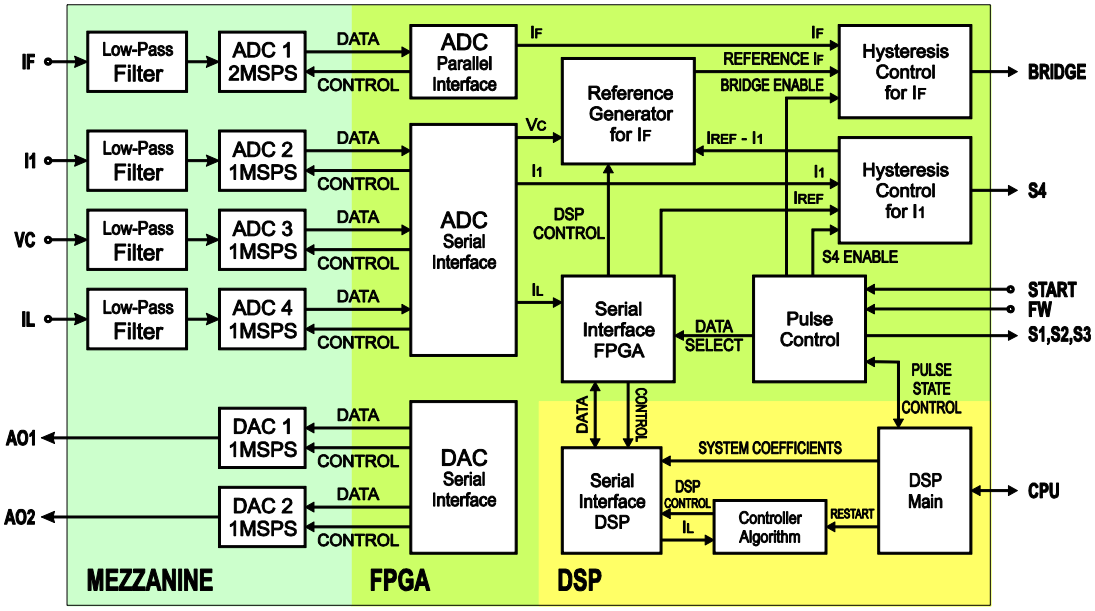


Figure 19: Functional diagram of control board.

The DSP internal blocks are: Serial Interface DSP, Controller Algorithm and DSP Main. The Serial Interface block is used to send the current pulse parameter and to carry out the digital controller communication with FPGA. The DSP Main block coordinates the DSP operation during the pulse genaration stage and performs the communication control with CPU. Its operation is further detailed in Section 3.3.

The MEZZANINE acquisition board consists of 5 ADC converters and their corresponding input filters and 2 DAC converters used as test signals to debug the system. These converters are controlled from the FPGA. Section 3.2 describes their operation in more detail.

Finally, the FPGA is composed by the following blocks: ADC and DAC Interface, IF and I1 Hysteresis Controls, Serial Interface FPGA, IF Reference Calculation and Pulse Control. The Pulse Control block receives synchronous signals, commands the switches, enables hysteresis controllers and handles communication with the DSP. A more detailed description is provided in Section 3.4.

3.2 *Analog-Digital Interface (Mezzanine Board)*

The CERN EDA-01729-V3 internal code is assigned to the new mezzanine board, whose main features are explained below, and Appendix 6.2 provides the schematic of the circuit and the PCB board.

3.2.1 Analog to Digital Converters

The new analog-digital interface consists of five AD7621[7] converters from Analog Devices. One converter is set to operate with parallel communication at 2 Msps; while the others, with a series communication at 1 Msps. The four series converters acquire data simultaneously and are commanded by FPGA with a 40 Mhz clock.

The converters inputs have third-order differential active filters to reject high-frequency noise. The filter cutoff frequency for the 2Msps channel is 4MHz and 1MHz for the remaining channels. To implement the filters, a Multiple Feedback Fully Differential ADC Driver topology [5,6] is adopted with THS4130 operational amplifiers, which can handle highly capacitive loads such as converters inputs. Butterworth filters are chosen to this end. Appendix 6.2 contains schematic diagrams of implemented filters.

The dynamic input range corresponding to the various channels are different. There are two bipolar channels, one with an input voltage range of +/- 10V (CH1) and another one of +/- 5V (CH5). The other channels are unipolar with an input voltage of 10V (CH2, CH3, CH4). The table below specifies the relationship between the actual values and their corresponding digital representation.

Table 3

Dynamic ranges

Output Digital Signal	Input Signal				
	CH1	CH2	CH3	CH4	CH5
7FFF	10.22 V	10.11 V	10.11 V	10.12 V	5.11 V
0000 / FFFF	0 V	5 V	5 V	5 V	0 V
8000	-10.22 V	-0.11 V	-0.11 V	-0.12 V	-5.11 V

The converters' data sheets describe the different data communication modes. The "Read after Conversion" communication mode[7] is used both in parallel and serial communications, where FPGA acts as the MASTER device.

3.2.2 Digital to Analog Converters

Two digital-analog AD5641 converters from Analog Devices are used to measure the FPGA internal digital signals. These converters operate simultaneously at 1Msps and use a series communication with FPGA, performed by means of a 20 Mhz signal clock.

The device datasheets provide a timing diagram of the digital communication. In this application, FPGA acts as the master device that controls communication. Section 3.4.2 below introduces the protocols used in converters-FPGA communication.

3.3 *DSP*

The flowchart of the program implemented in the DSP is shown in Figure 20. DSP operations are executed via an interruption routine every time a communication with FPGA through the SPI module is performed.

The interruption service routine comprises three basic tasks: reading data sent by FPGA, computing the control algorithm or system parameter and writing down the output data to be sent to FPGA in the next transmission. The control algorithm calculations are executed during flat top and the calculation of the system parameters once the Forewarning signal order is received. Appendix 6.3 shows the generated source code.

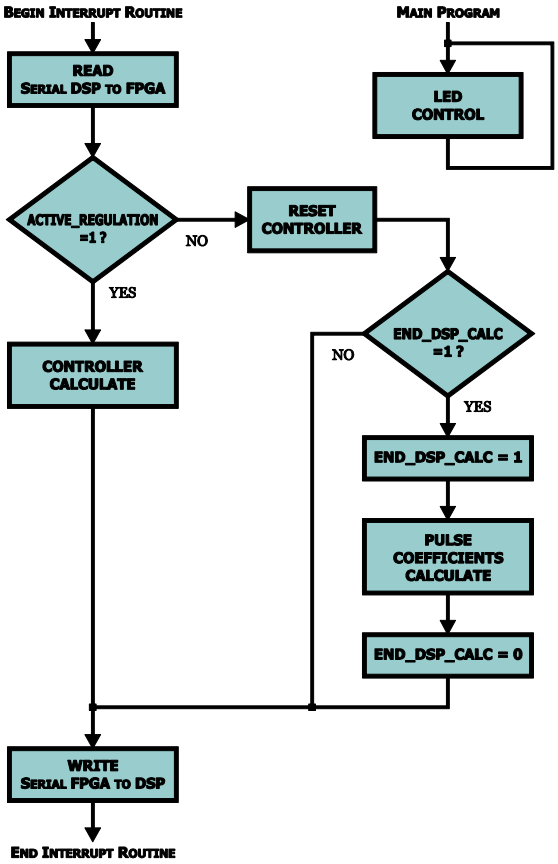


Figure 20: Interruption service routine and main program flowchart.

3.3.1 DSP-FPGA Communication

The communication with FPGA is possible through five control lines and a bidirectional serial communication channel. Figure 21 depicts the signals used in the protocol communication.

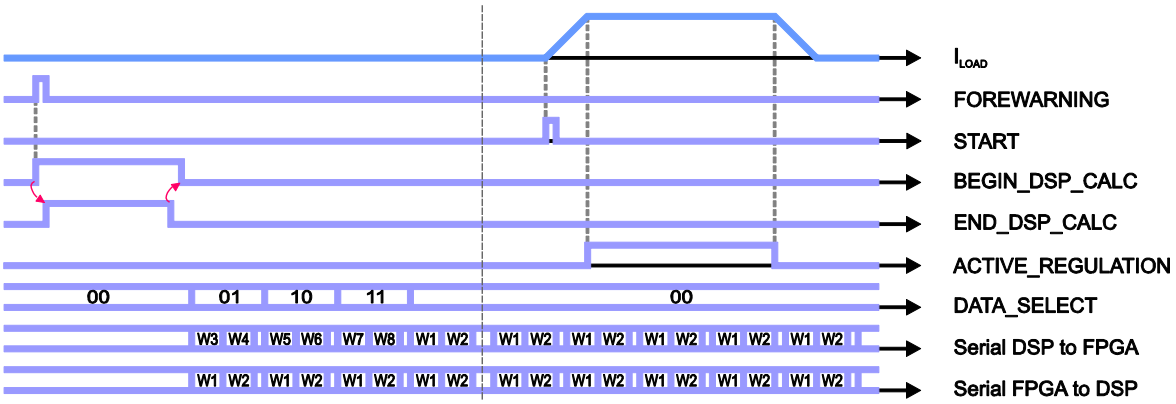


Figure 21: Timing diagram of DSP-FPGA communications.

Once the Forewarning signal is received, FPGA sends the BEGIN_DSP_CALC signal to the DSP, to begin parameters calculations. DSP responds FPGA's request with the END_DSP_CALC signal, which indicates that calculations have been concluded and are ready to be sent. Then, parameters transmission takes place through the serial channel defined in the diagram as Serial DSP to FPGA. In each transmission, two words are sent, whose order is determined by DATA_SELECT signals.

Once parameters transmission has been executed, the program waits for the START signal. During that time, irrelevant data are kept being sent to FPGA. When the START signal is activated, the pulse generation begins and the current rises to reach the flat-top reference value. Having reached the value, the FPGA activates the ACTIVE_REGULATION signal, which indicates the beginning of the control algorithm data transmission with the DSP. The transmission and calculation processes last aproximately 10 us.

The Serial DSP to FPGA and Serial FPGA to DSP communication channels work simultaneously and send two 16-bit words each at a frequency of 200 kHz by means of a 20MHz clock signal.

3.3.2 Main Program

The Main Program is a waiting loop where an interruption coming from the SPI block is expected. Such interruption indicates that the communication with FPGA has taken place. Then, depending on the signals described above in Section DSP-FPGA Communication, DSP decides on the task to be carried out. Within this loop, DSP controls a led in the control board to indicate that it is active.

3.3.3 Controller Algorithm

The analog Gc controller is transformed to its discrete equivalent using the bilinear transformation. The code used is included in Appendix 6.3.

Calculations within DSP are conducted on a fixed point arithmetics with a 32-bit word length. To do so, the difference equation coefficients of the controller and the input variables are affected by a constant, and the results obtained are subjected to the necessary corrections. The controller coefficients are fixed.

3.3.4 DSP Setting

The DSP is entirely programed in the format C language. Code Composer Studio v3.1 is employed for code writing, compilation, programming, and software debugging. To program the DSP, a JTAG model XDS510USB is employed, which is also used for debugging.

3.4 *FPGA*

FPGA is the main block of the control system. The implementation design is divided into blocks of reduced complexity, explained in the following sections.

The programming environment is explained below. Appendix 6.4 shows the program generated in each block and provides the corresponding source code.

3.4.1 Pulse Control

This block controls the states during the current pulse generation. Its functions are listed below:

- Control of the connection among converter stages (I1 Generator, Active Filter, etc.), by means of S1_control, S2_control and S3_control signals.
- Activation of I1 and If current controls by means of S4_enable y bridge_enable signals.
- Activation of the Gc controller by means of the ACTIVE_REGULATION signal
- Control of data transference between DSP and FPGA, by means of the DATA_SELECT signal
- Demand of the hysteresis band calculation before the pulse beginning by means of the BEGING_DSP_CALC and END_DSP_CALC signals.

Figure 22 shows the different tasks execution sequence in a timing diagram.

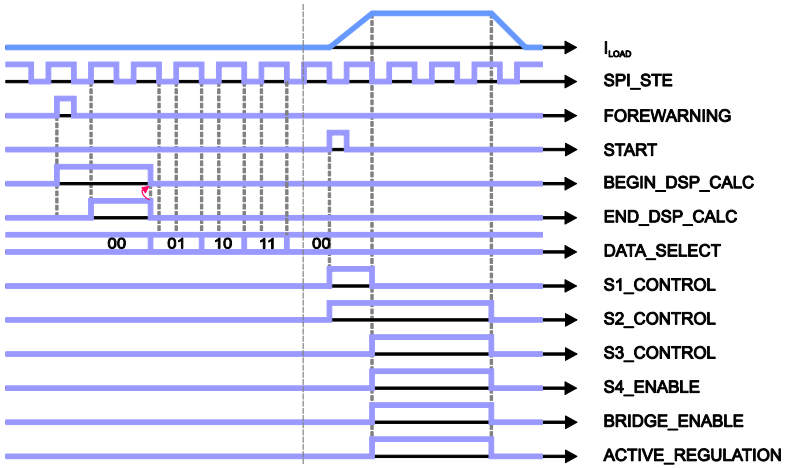


Figure 22: Timing diagram of FPGA Pulse-Control block.

A more detailed description is provided in the flowchart shown in Appendix 6.4.

3.4.2 ADCs and DACs Control

ADC Parallel block

The operation sequence in this block is as follows:

- Acquisition start: it originates when this block receives a low level in the START_ACQUISITION signal.
- Conversion: 450ns are expected in this stage to ensure valid conversion data.
- Data transfer: this function is enabled by CHIP_SELECT signal. Data are sent in two stages: first the upper part and then the lower part of the 16-bit digital signal. The selection between these two parts is by means of the BYTE_SWAP signal.
- End of data transfer: once the transfer ends, the FPGA sets the CHIP_SELECT signal, leaving the system ready for a new acquisition.

Figure 23 shows a timing diagram of the ADC Parallel block.

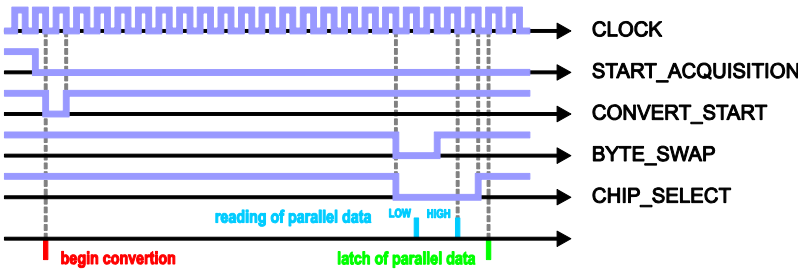


Figure 23: Timing diagram of FPGA ADC Parallel block.

ADC Serial block

This block performs the same operations sequence that the Parallel ADC block. However, in this case the transmission is performed in serial mode through the SERIAL_DATA line, one bit at a time in a given order, beginning with the most significant bit, and changing in each cycle of the SERIAL_CLOCK signal. The converter updates the serial data in each positive edge of the SERIAL_CLOCK signal. Conventionally, this data would be read in the FPGA in the following negative edge. However, due to the high transmission frequency and to the board delays, it is considered more appropriate to carry out such reading in the next positive edge, as shown in the Figure 24.

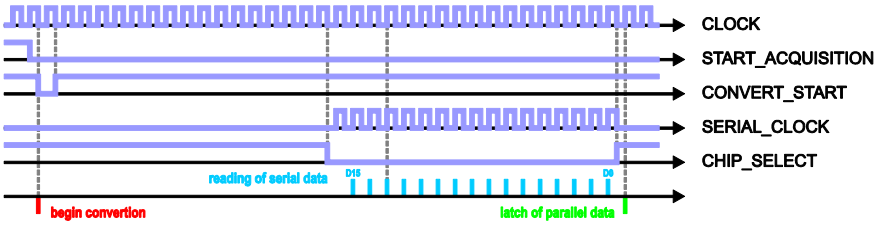


Figure 24: Timing diagram of FPGA ADC-Serial block.

DAC Serial block

A timing diagram depicting DAC Serial block is shown in Figure 25. Once the order has been received through the START_TRANSMITION line, data are sent in serial mode to the converter synchroneously with the CLOCK signal. The data transfer consists of two zero bits in the upper part added to the 14 bits of the converted data. These two zeros are part of the communication protocol and they are used to set the way the converter operates (datasheet of AD5641).

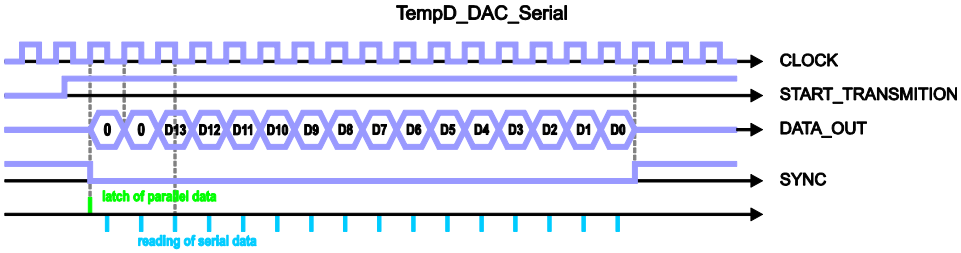


Figure 25: Timing diagram of FPGA DAC-Serial block.

3.4.3 DSP Communication

To communicate with DSP, the FPGA uses three blocks. The first one called SPI DSP Control performs the serial communication, in which two 16-bit words are sent and received in each communication. The remaining two blocks (SPI DSP Receptor and SPI DSP Sender) transfer data between the first block and the FPGA internal registers. The selection of internal registers depends on the state of the DATA_SELECT signal. Table 4 lists the transmitted and received signals.

Table 4

Signals transmitted between DSP and FPGA

DATA_SELECT	DSP to FPGA	FPGA to DSP
000	Regulation_Result	Acquisition_Il
001	Damping_Coeff	Acquisition_Vc
010	I_Reference	Acquisition_Il
011	Time_Pulse	Acquisition_Vc
100	Hys_Band_If_Max	Acquisition_Il
101	Hys_Band_If_Min	Acquisition_Vc
110	Hys_Band_I_1_Max	Acquisition_Il
111	Hys_Band_I_1_Min	Acquisition_Vc

Figure 26 shows the timing diagram of SPI DSP Control block. A 20MHz serial communication clock (SPI ClOCK) is used.

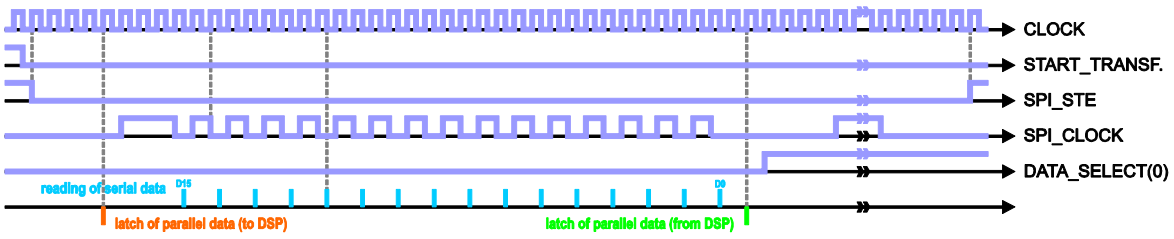


Figure 26: Timing diagram of SPI-DSP-CONTROL block.

The operations sequence for the bidirectional data transfer is as follows:

- Request transfer it is generated by a low level in START_TRANSF signal.
- Start transfer: the SPI_STE signal level is lowered
- Data transfer: two serial words are sent and received simultaneously. The transmission order is controlled by the DATA_SELECT signal.

3.4.4 Reference Generator for IF

This block calculates the reference of the active filter by means of following equation:

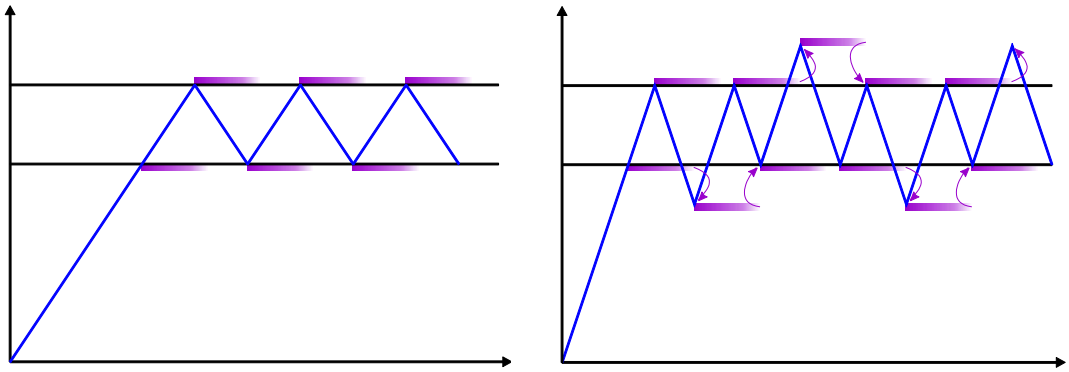
$$REFERENCE\ \_I_F = DSP\_CONTROL - (V_C \cdot DAMPING\_COEF) + (I\_REF - I_1)$$

where: the first term corresponds to the main control loop, the second to the damping, and the third one to the cancellation of I_1 ripple.

3.4.5 Hysteresis Control

A hysteresis control, whose particularity is that of limiting switching frequency, is performed for this application. If the switching frequency is within the normal operation parameters, it behaves as a simple hysteresis control. If, due to a possible change in the parameters, the frequency intends to exceed the limit, the implemented control inhibits the commutation.

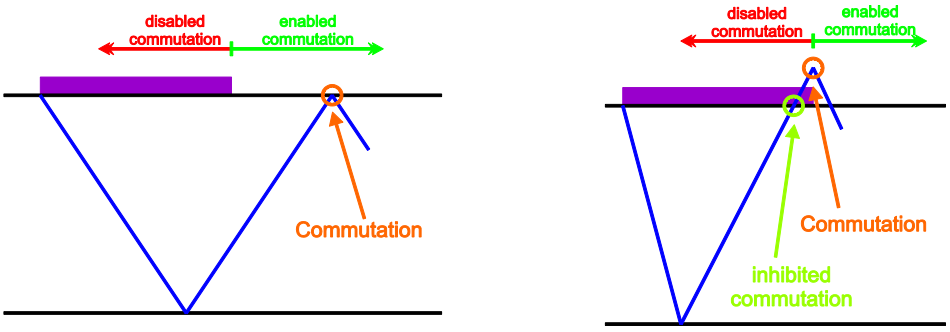
The switching frequency limitation is simple. Every time the current reaches a hysteresis band, a timer loaded with a value corresponding to the minimum switching period begins to run. During the timer operation, the commutations generated by the arrival of the current to the same band that has started the timer is inhibited. i.e., the commutation takes place after the timer expires.The normal and limited operation modes are shown in figure 27a and 27b, respectively.



(a) Normal Work (b) Limited Work

Figure 27: Waveforms resulting from hysteresis control.

Figure 28 details frequency limitation behavior in the upper hysteresis band under normal operation (a) and under limited operation (b). The same principle applies for the lower band.



(a) Normal Work (b) Limited Work

Figure 28: Behavior of the hysteresis control.

Figure 28a shows the timer operation. This timer is activated when the signal reaches the upper hysteresis band. Then, since the timer expires before the current reaches the same hysteresis band commutation takes place on a normal mode.

Figure 28b shows the case when the current reaches the upper band during timer operation. As a result, the current commutation is inhibited until the timer expiration. A control diagram is provided in the Appendix 6.4

3.4.6 FPGA programming software

FPGA programming is carried out using the hardware description language VHDL. To compile the code, Synplify Pro v9.4 software is used. This software generates a netlist which is implemented with Project Navigator v4.2.03i software. Impact v6 software is used to program the FPGA.

3.5 *BOARD MODIFICATIONS*

To implement the digital control, modifications were introduced in the EDA-01366 Control Board. As the switches control signals should be performed from the FPGA, the control signals from the DSP have to be replaced by the FPGA ones. To do so, the FPGA and DSP control output signals were interconnected; at the same time, the DSP lines were set as input to avoid any potential connection conflict.

Figure 29 shows the relationship between the switch control signals of FPGA and board external terminals.

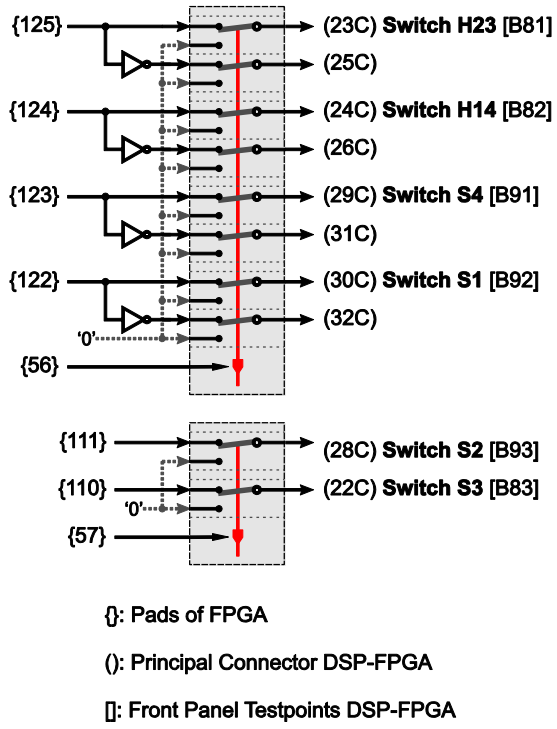


Figure 29: FPGA- switches commands connections.

4. Prototype

To validate the proposed topology, the current and voltage values of the prototype have been scaled to laboratory levels; though the dynamics and the switching frequency of the full scale converter have been maintained.

The characteristics of the components used are scaled and mounted on two boards in the laboratory work bench. Therefore, the technical characteristics of the full scale model are not present, for instance, the turn- ON and OFF times of the high voltage switches are lower than the full scale ones.

Table 5 indicates the values of the implemented prototype.

Table 5

Specifications of the prototype built

Load Current	15A
VC1	20V
VC2	10V
VC3	10V
GI_1 switching frequency	10 KHz
GIF switching frequency	100 KHz

4.1 *Simulations*

Taking into consideration the differences between this prototype and the full-scale converter, a complete system simulation is performed using a model that represents the detailed behavior of the low scale prototype. The effects of the discrete control system are also included together with the characteristics of the control board. Figure 30 shows the main signals in the system.

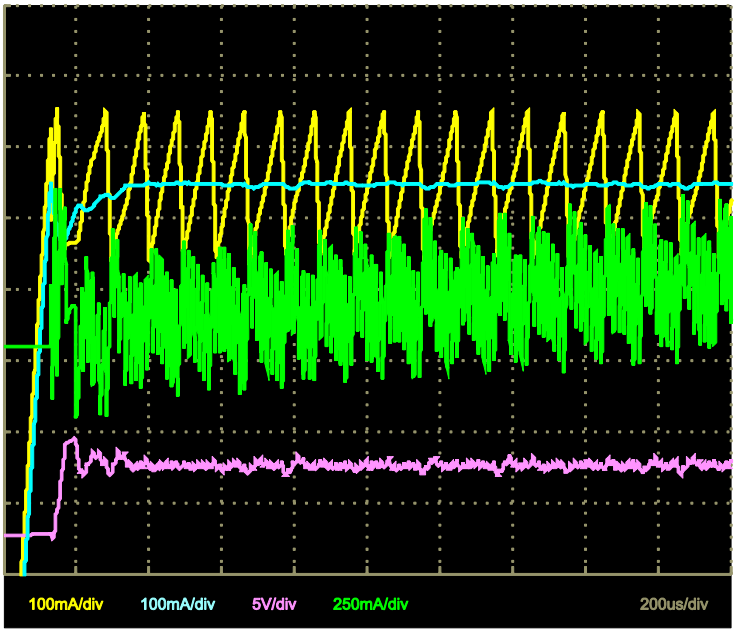


Figure 30: Prototype simulation. (The yellow curve represents current I_1, the blue one, the load current, the green one, the active filter current, and the violet, the voltage on capacitor C)

Figure 30 shows important transient oscillations at the beginning of the flat-top, in the capacitor voltage and in the I_L current. This behavior is the consequence of a reduction in the phase margin resulting from a communication delay between DSP and FPGA. To validate this assertion, I_F and I_1 switching frequencies, together with the cutoff frequency of the passive filter

and the system bandwidth, are reduced to a half; while the acquisition speed is maintained. Thus, the processing time of the digital control is also reduced to a half in relation to the time associated with the system.

Figure 31 shows the improved behaviour.

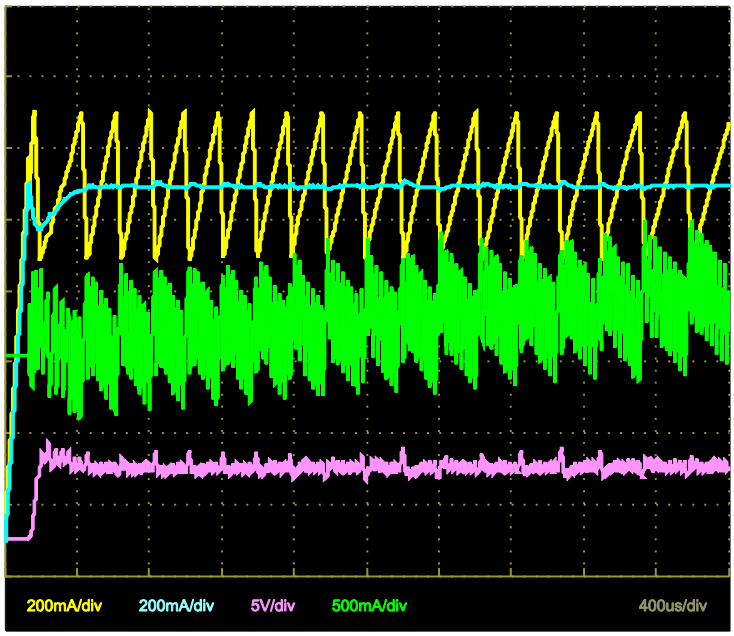


Figure 31: Simulation of the prototype with reduced speed.

Figure 31 shows that the I_1 rising slope is much smaller than the falling slope. This is mainly explained by the high voltage drop in the switches when they are turned on in relation to the input voltage source. This is not evident in the full-scale prototype due to its construction characteristics. The difference between the I_1 ripple slopes constitutes a high demand for the active filter, which in turn affects the ripple compensation. This figure also shows that the main perturbations in the load current are attributed to this phenomenon. A complete current pulse is shown in Figure 32.

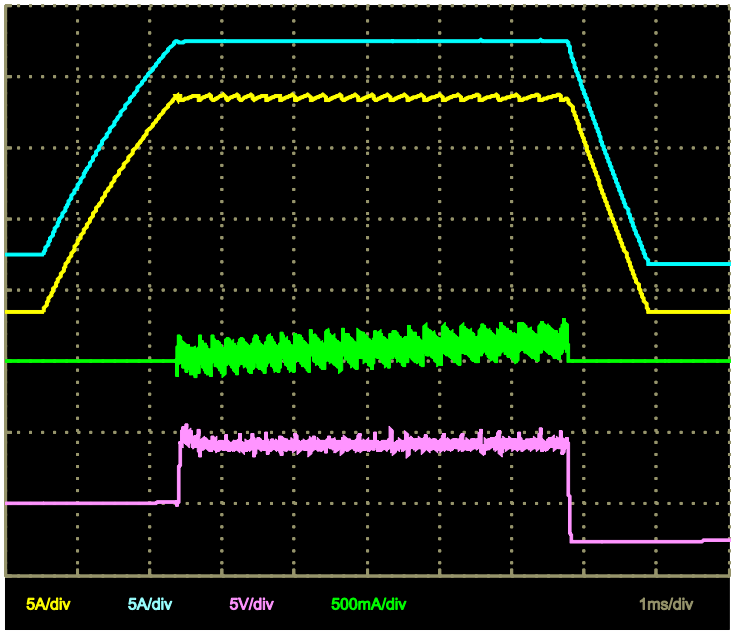


Figure 32: Simulation of a complete pulse.

4.2 *Prototype construction*

Two boards constitute the prototype, the Main board and the Active Filter Board.

The main board consists of:

- High voltage stage: C_1, S_1, D_1, S_2 and D_2,
- I_1 generator: C_2, S_4, D_4 and S_{I1} current sensor,
- Capacitor, C,
- Switch S_3,
- Drivers of S_1, S_2, S_3 and S_4,
- Signal conditioning circuit.

The active filter board comprises:

- The full bridge IGBT stack,
- The floating source C_3,
- Output inductor L_F,
- Full Bridge drivers with the switches dead-times.

Appendix 6.5 includes the schematic of the boards built and the corresponding PCB.

4.3 *Prototype images*

This section includes some images of the prototype. Figure 33 illustrates the complete work bench with the two prototype boards, the control board, the L_1 and L inductors and the current sensors. The power sources and the oscilloscope can also be seen.

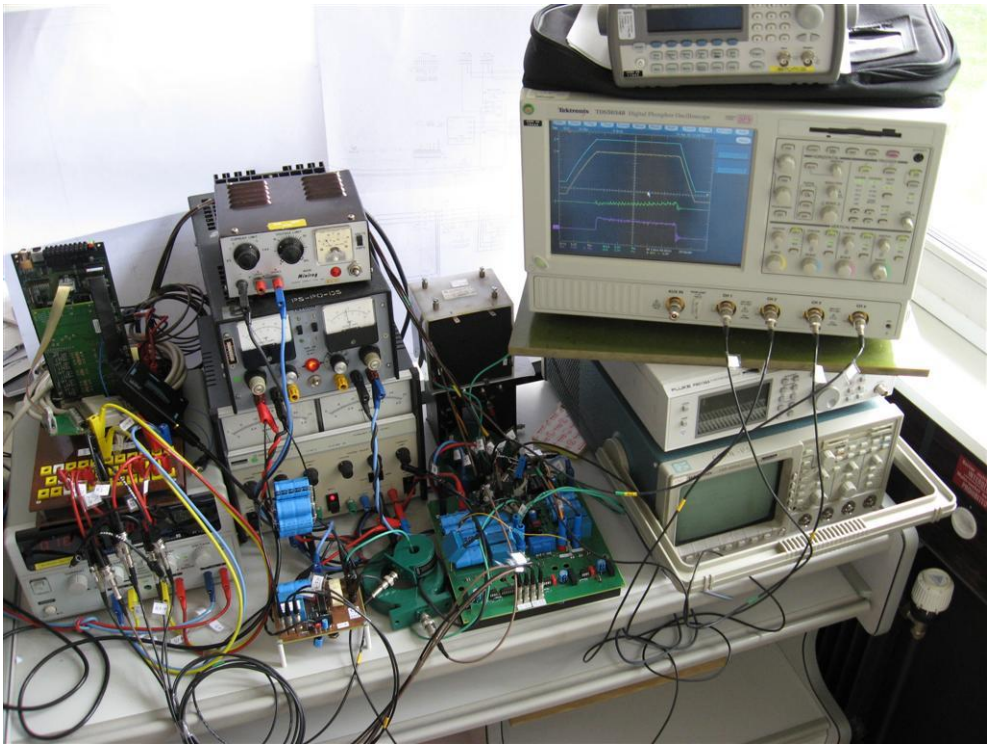


Figure 33: Measurement bench.

Figure 34 illustrates the main board, and figure 35 the active filter board.

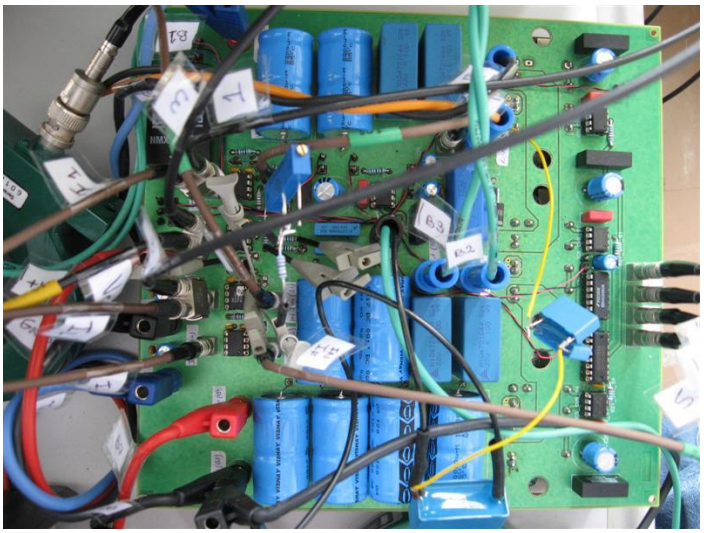


Figure 34: Main power board.

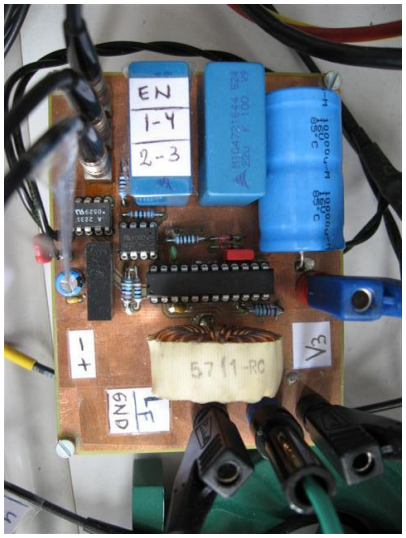


Figure 35: Active filter board.

Figure 36 shows the control board mounted on an adapter board.

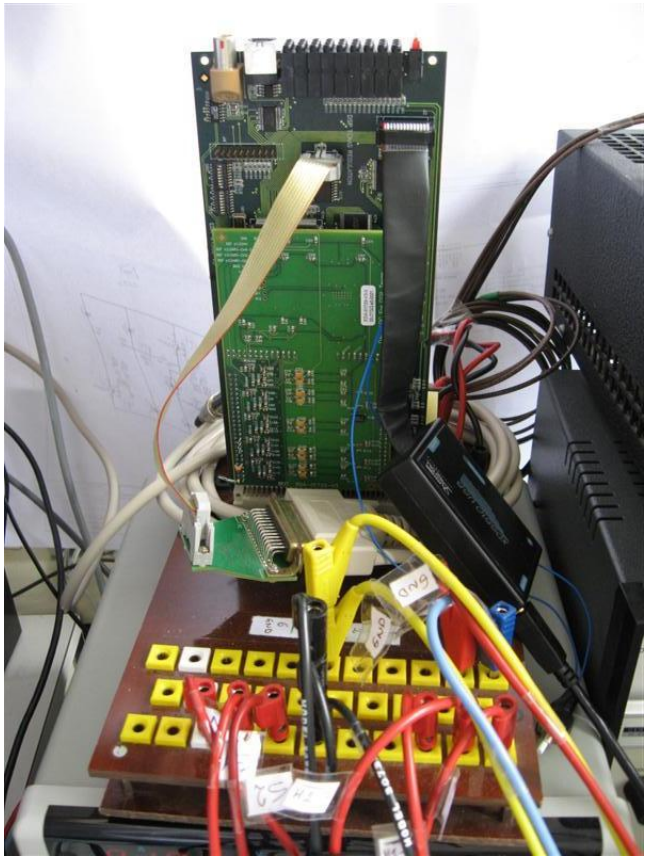


Figure 36: Control board and its mezzanine used for A/D and D/A conversion.

4.4 *Experimental results*

Figure 37 shows the measurements taken on the reduced scale prototype. In this case, a zoom on the flat-top is made. For comparison purposes, scales were the same as those used in the simulations.

A similarity in the behaviour can be seen when comparing measurements (Fig 37) with simulation results (Fig 31).

Figure 38 shows a complete current pulse generation. This can be compared with figure 32, which illustrates the simulation of such same event.

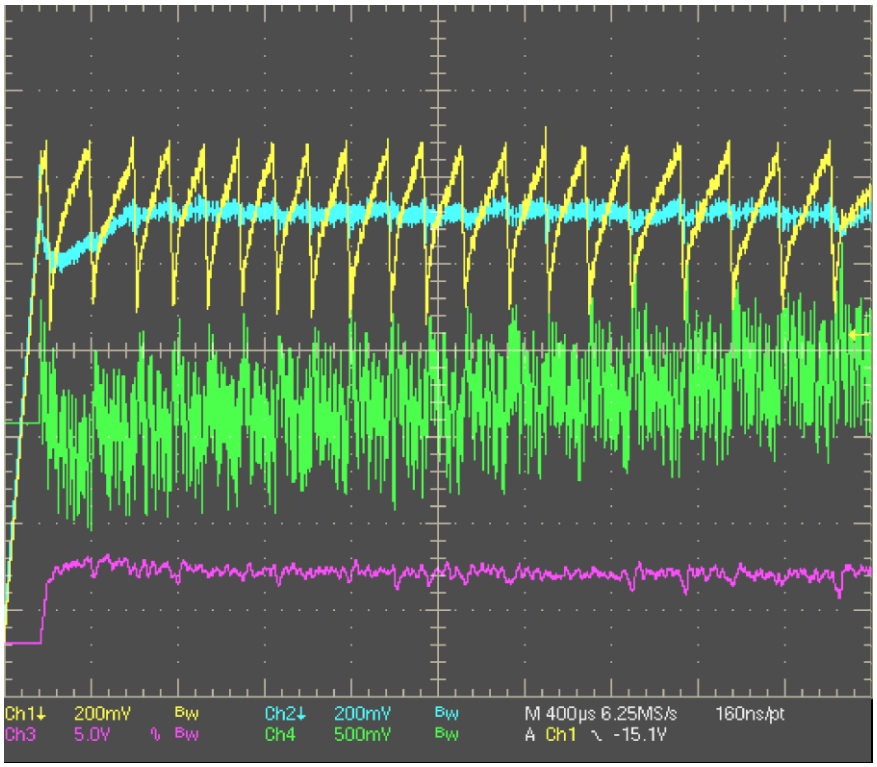


Figure 37: Measurement on the prototype (the yellow curve represents current I_1, the blue one the load current, the green one the current delivered by GIF generator, and the violet, the voltage on capacitor C)

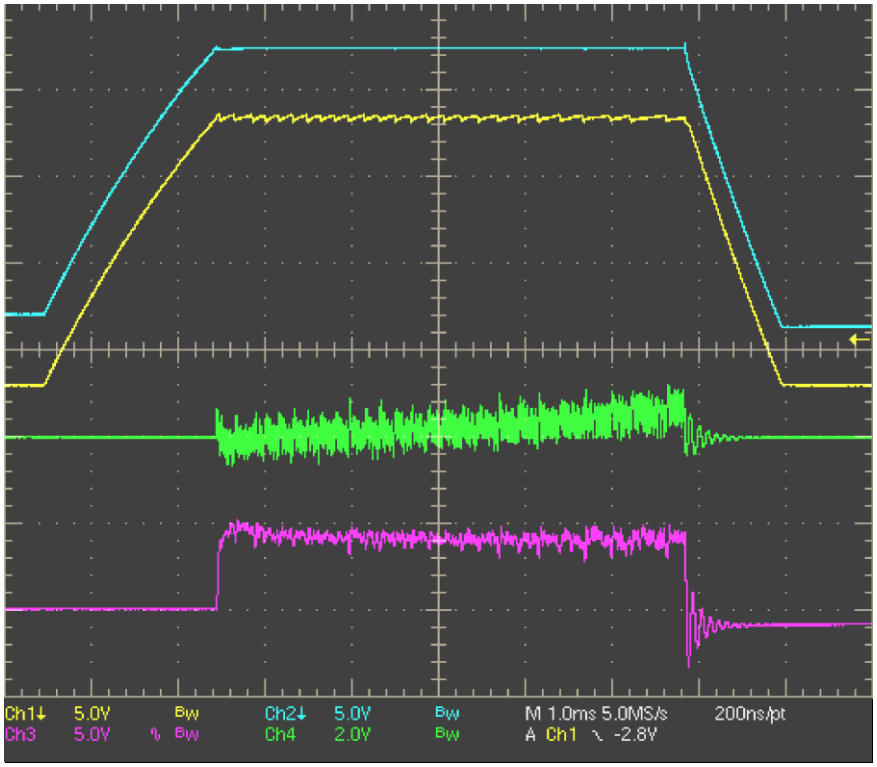


Figure 38: Measurement of a complete pulse.

The figure above shows that the active filter current increases along the pulse to compensate an error in the load current measurement. This error results of the use of a PEARSON-type sensor. This sensor is a current transformer that can measure only AC currents and leads to errors in DC value measurements. As a consequence, the real load current will increase during the flat-top.

Since the sensor does not meet the precision requirements, the control is not able to satisfy the specifications. Thus, this problem will must solved when building the full-scale prototype.

5. Conclusions

In this project a control board existing at CERN was used to develop the control system for the proposed topology. A new, faster analog-to-digital signal converter board was designed. A scale prototype was built to validate the new topology behavior. Simulations of the new system carried out involved the conversion and calculation delays presented in the experimental control board.

The reduced scale prototype that has been built has allowed to validate the proposed topology. It will also be a great help for the testing of the the full-scale prototype.

This work has has also demonstrated the need to rely on a faster control platform in order to decrease delay times affecting the stability and precision required. This is corroborated by the correspondence existing between the simulations and the experimental results, as the system operates correctly with reduced bandwith and commutating speeds. The present system has been using the existing CERN control board to its limits and the need to redesign the control board using more powerful hadware (DSP, FPGA, parallel ADC, …) has been shown.

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6. APPENDICES

6.1 *FULL SCHEME OF THE IMPLEMENTED SYSTEM*

6.2 *MEZZANINE BOARD*

6.3 *DSP SOURCE CODE*

6.4 *FPGA SOURCE CODE AND SCHEMES*

6.5 *PROTOTYPE BOARDS*