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Building and commissioning of the CMS pixel barrel detector

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ABSTRACT: The CMS pixel barrel detector is a complex system that consists of 768 segmented silicon sensor modules. The total number of readout channels in the system is about 48 million. An overview on the module assembly and qualification procedures as well as testing results will be presented. The assembly of the detector control and readout electronics on the supply tube, the integration of the final system and the installation into CMS will be explained. The strategy and results from the early commissioning of the complete system that includes the performance of the hardware and the data acquisition and control software will be reviewed.

KEYWORDS: Solid state detectors; Large detector systems for particle and astroparticle physics; Hybrid detectors

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1 Introduction

The CMS barrel pixel detector is composed of three cylindrical layers. The length of the detector is 53 cm, the layers have mean radii of 4.4, 7.3 and 10.2 cm. The detector has been built at the Paul Scherrer Institute (PSI) in about two years, finishing at the beginning of 2008. It took more than 10 years to develop the final design of the readout chip (ROC) and the module, the cooling system and the mechanical structure.

The barrel pixel detector is built of 768 segmented silicon sensor modules. The size of a module is $66.6{\times}26\,\mathrm{mm}^2$, the weight is up to 3.5 g depending on the final length of the signal and power cables. There are two types of modules: full modules composed of 16 ROCs and half modules built of 8 ROCs. In total the barrel pixel detector contains 672 full and 96 half modules. Each ROC is segmented into 4160 pixel readout channels. The pixel size is $100\,\mu$m in $r-\phi$ and

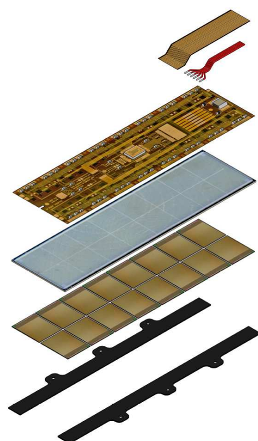

Figure 1. The components of a barrel pixel detector module (from top to bottom): the Kapton signal cable, the power cable, the HDI, the silicon sensor, the 16 ROCs and the base strips.

150 μm in z. The total number of readout channels is about 48 million (47923200). Detailed descriptions of the CMS barrel pixel detector can be found in [1, 2].

All components of the modules were assembled and tested at PSI. The testing procedures, the production rate and the yield at each step of the module production are presented in section 2. Each module has been checked for functionality and extensive performance tests and calibrations have been made. The module testing procedures, the qualification criteria and the results will be discussed in section 3. Furthermore, the technique for mounting the modules on the support structure, the assembly of the detector control and readout electronics on the supply tube, the integration of the final system and the installation into CMS will be explained in section 4. In addition the strategy and results from the early commissioning of the complete system will be reviewed in section 4. This includes the experiences gained in the operation of the pixel detector at PSI and after the installation at CERN, as well as the performance of the hardware and the data acquisition and control software.

2 Module assembly

The sensitive element of a module is a silicon sensor [3] with a dimension of $66.6\times18.6\,\mathrm{mm}^2$ and a thickness of about 285 μm. A minimum ionizing particle crossing the sensor at an angle of 90° deposits energy corresponding to about 22000 electrons on average. An array of 16 or 8 readout chips [4] is bump bonded to the Si sensor. The ROC dimension is $8\times8\,\mathrm{mm}^2$. On the other side of the Si sensor a high density interconnect (HDI) flex printed circuit is glued and wire bonded to the ROCs. A token bit manager chip (TBM) [5], that controls the readout of the ROCs, is mounted on top of the HDI. To fix a module to the mechanical support structure two base strips made of Si_3N_4 are glued to the ROC side of a bare module. A power cable that brings analog, digital and high voltage to the module is soldered to the HDI. A Kapton signal cable, through which the ROCs are controlled and readout is wired to the TBM. The components of a barrel pixel detector module are shown in figure 1.

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All components have been carefully tested before being used in the module assembly. Below, the main module construction steps and test procedures are briefly described.

2.1 Readout chip testing

All ROCs have been tested on the wafer level with the help of an automated probe system. The goal of the tests is to identify ROCs that are fully functional having less than 0.1% defective pixels. The test procedure performed on each ROC includes the following steps:

- verify that each pixel readout channel responds to the internal calibrate signal and provides the correct address in the readout,
- perform a comparator threshold scan for every pixel readout channel and verify that the mean value, RMS and global spread satisfy the qualification criteria,
- test the functioning of the 26 DAC registers that are used to program the ROC,
- check the functioning of the 4 threshold level trim bits and the masking mechanism,
- verify that data and time stamp buffers work properly,
- check the ROC power consumption.

ROCs are programmed using the I2C protocol. To test each ROC about 400k I2C commands have to be executed which takes about 20 sec. Therefore, four wafers ($\sim$1000 ROCs) could be tested per day. Accepted ROCs are not allowed to have more than 4 defective pixels. Trim bits, mask, address and functionality tests are binary tests: if any pixel fails the test, the ROC is discarded. The average yield of ROCs qualified for module production is 74%.

2.2 Si sensors

The Si sensors have to satisfy the following requirements. All wafers, each containing three sensors, should come from the same ingot. This restricts the spread of the depletion voltage that should be in the range $V_{depl} \simeq 55 - 65$ V. The leakage current at a bias voltage of 150 V is required to be less than 2 μA. The slope of the I-V curve defined as the ratio of the current at 150 V and 100 V, I(150 V)/I(100 V), should be less than 2.

During the module production a small number of Si sensors was damaged. The loss was about 10% in bump deposition and wafer cutting. Another 5% of the sensors have been damaged during the bare module assembly.

2.3 ROC-Si sensor bump bonding

An elaborate indium bump bonding procedure has been developed at PSI [6]. In a first step, photolithographic and under-bump-metal (UBM) treatments of ROC and sensor wafers are done. UBM is needed to make a robust connection between indium bumps and Al pads on wafers. It is composed of thin layers of Ti, Ni and Au. Then, indium is evaporated on both wafers. The next step is the lift-off of the photo-resist. Sensor wafers are re-flowed in an oven to make spherical bumps. Finally, ROCs and Si sensors are cut out and the ROCs are placed and pressed to the sensors. Afterward, the bare modules are re-flowed again. The in-house fabricated bump bonding machine

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provides a precision of $1-2\,\mu$m in placing ROCs on the sensors. Thanks to the fully automated procedure, up to 6 bare modules were produced per day. All ROCs were tested before the bonding. The testing procedure is similar to the one done on-wafer and has a yield above 97%. The bare modules also have passed a test that included an I-V curve and ROC functionality tests. In case of low quality bump bonding, it is possible to rework a ROC with a 80% success rate. The overall yield of the bare module test is about 85%. Failures are split into several categories:

- Modules draw a high leakage current due to various damages of the sensors (40%).
- A sizable fraction of indium bumps is missing due to failures during the processing of the sensor wafers (18%).
- Both above failures at the same time (8%).
- Sensor problems: scratches, failures with indium evaporation (no bumps formed), etc. (28%).
- Various failures during electrical tests that stay after the rework of the ROCs (6%).

2.4 Building modules

The HDIs equipped with the passive elements (capacitors and resistors) are tested by the vendor. The TBM chip and the signal cable are first glued and then wire bonded, the power cable is soldered to the HDI. Up to 15 HDIs have been assembled per day. The HDI has been tested for the TBM chip functionality and shorts or broken traces in the power and token passage lines. After a procedure of assembling and storing of HDIs had been established, the failure rate was reduced to less than 2% [7].

Two base strips are glued to one side of the bare module, the HDI is glued to the other side. In a final step, the ROCs are wire bonded to the HDI. Up to 6 modules per day have been produced. Failures were mainly related to human mistakes and happened rarely, only 6 out of almost 1000 modules have been lost that way.

3 Module test procedures and results

The goal of the module tests at PSI was to verify that all pixels function correctly, that each ROC can be programmed properly, and that all calibrations of a module produce reasonable results. The task was a challenge due to the large number of channels ($5-6\times10^7$ pixels) and the multidimensional parameter space: each ROC has 26 DAC registers to be set out of which 8 have to be tuned for each ROC individually.

Another complication results from the unknown temperature at which the pixel detector finally will be operated and the missing knowledge of the module behavior after thermal cycling. Therefore, the full test procedure described below has been performed twice at -10°C (before and after 10 thermal cycles) and then, repeated at +17°C. The complete test procedure and the analysis of test results were fully automated: human interventions were reduced to placing modules in the cooling box, starting a program that supervises all procedures and browsing results that appear on an automatically generated web page.

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The PSI test setup is composed of a programmable cooling box in which four modules can be tested at a time, four custom test boards connected to a PC via the USB interface and a high voltage supply. The test board includes a field-programmable gate array (FPGA) which controls the tests as well as two ADCs.

3.1 Module test procedure

The test and qualification process is divided into three main steps. First, all ROCs have to be set into an operational state by adjusting the proper DACs: the analog current is set to the nominal value of 24 mA, the header levels (ultra-black) of the output from all ROCs are set to a common value, the signal threshold and the timing of the internal calibrate signal are tuned to a stable state. In the second step, the functioning of the pixel readout circuits and their electrical connections to the sensor pixels are checked. The following procedures are performed:

- Check that each pixel responds to the calibrate signal.
- Test the functionality of the four threshold trim bits.
- Determine the bump-bonding quality.
- Verify that each pixel readout circuit responds with the correct pixel address.

The main characteristics of a module have been determined by performing the following tests.

- Determine the noise for each pixel.
- Set the threshold of each pixel to obtain a uniform response over the whole module (trimming).
- Establish the dependency of the pulse height on the injected charge.
- Verify the absence of sensor breakdown and high leakage current (I-V curve).
- Calibrate the temperature sensor of each ROC.

The internal calibrate signal (V_{cal} DAC) is used for many tests and calibrations. It is important to know the conversion factor between the V_{cal} unit and the corresponding number of electrons. The calibration has been done using an X-ray setup built at PSI.

The full description of the module qualification procedures and the results can be found in [8, 9]. In the following, selected examples of tests and calibrations are briefly described.

3.1.1 Noise measurement

Noisy pixels may flood the ROC with a high rate of fake hits and cause significant dead time and data losses. Therefore, either the threshold of these pixels has to be increased or the pixels have to be masked. The noise of a pixel is determined by measuring the so called S-curve, i.e. the efficiency of the pixel as a function of the amplitude of the calibrate signal. Assuming Gaussian noise, the S-curve has the shape of an error function and its width is a direct measure of the noise. Figure 2 illustrates the noise distribution of all, edge and corner pixels of modules used in the pixel detector construction. The noise of the edge and the corner pixels is higher because they have two or four times larger area with respect to the inner pixels.

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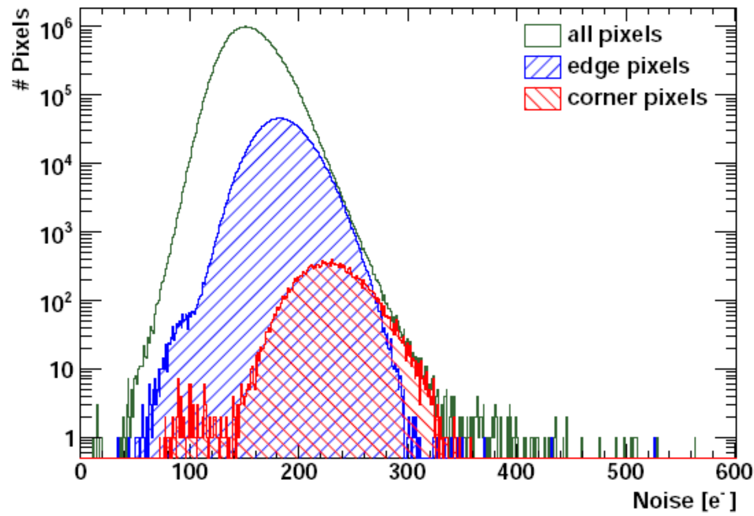

Figure 2. Noise levels determined from the width of the S-curves for all, edge and corner pixels.

3.1.2 Trimming

The aim of the trim algorithm is to unify the thresholds of all pixels on a ROC to the lowest possible value. To reach this goal, the following parameters are adjusted. A common threshold for all pixels in a ROC is set using the V_{cThr} DAC. To account for the pixel to pixel variations four trim bits are set in each pixel unit cell. The strength of the correction is determined by the trim voltage (V_{trim} DAC), which is set per ROC. The only relevant input parameter to the algorithm is the absolute threshold at which the response has to be unified. In practice this threshold is fixed by choosing a value of the V_{cal} DAC. The pixel threshold distributions for a single ROC are shown in figure 3 before and after trimming.

The trimming is an iterative procedure and is time consuming with the standard data acquisition system. A dedicated study has shown that the trim bit map does not depend on the target threshold, the temperature and the irradiation dose. On the contrary, the V_{cThr} and V_{trim} values depend on the threshold and temperature. The dependence on the threshold can be parametrized as follows:

$$V_{\mathrm{cThr}}(V_{\mathrm{Cal}}) = V_{\mathrm{cThr}}(60) - 0.65 \times (V_{\mathrm{Cal}} - 60) \tag{3.1}$$

$$V_{\mathrm{Trim}}(V_{\mathrm{Cal}}) = V_{\mathrm{Trim}}(60) - 0.45 \times (V_{\mathrm{Cal}} - 60) \tag{3.2}$$

These parametrizations will be applied to trim modules for a threshold different from the laboratory target threshold. The V_{cThr} and V_{trim} DAC settings depend linearly on the temperature, whereas the dependence varies from ROC to ROC. Therefore, it is possible to interpolate V_{cThr} and V_{trim} to any operational temperature using the values measured at +17°C and -10°C.

3.1.3 Pulse height calibration

For each hit pixel, the height of the generated pulse is recorded. It is a measure for the ionization charge collected in the pixel. The measured pulse height in ADC counts has to be converted into the

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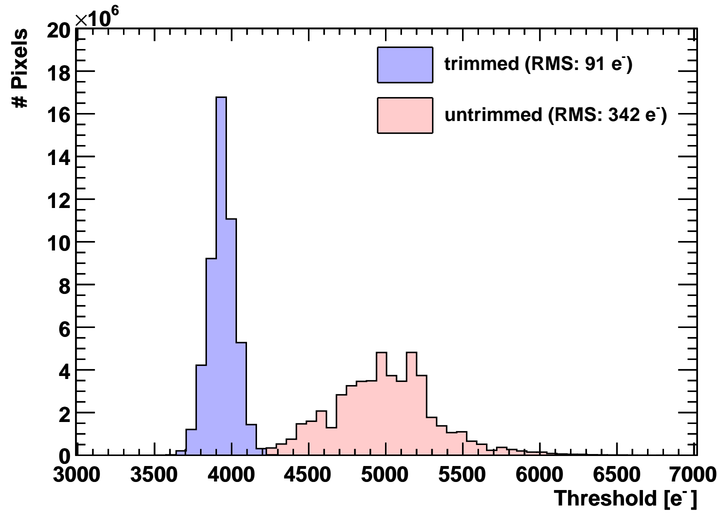

Figure 3. Threshold distribution of all pixels before and after trimming.

corresponding charge. This calibration is performed by injecting signals with various amplitudes to each pixel and measuring the corresponding pulse heights.

Before the calibration, the $V_{\rm sf}$ DAC register is adjusted to make the pulse height curve linear in the low $V_{\rm cal}$ range. The linearity is required for two reasons. On the one hand the non linear behavior (see figure 4(a)) in the low range does not allow to reconstruct the charge of the signal, on the other hand fewer parameters have to be stored in the data base. The saturation in the high range is less important since it occurs for charges of more than 30-40 ke$^-$. The pulse height curves can be parametrized with the following function:

$$y = p_3 + p_2 \cdot tanh(p_0 \cdot x - p_1) \tag{3.3}$$

If $p_1 \simeq 1$, the pulse height curve is linear in the whole region of interest (see figure 4(b)). Figure 4(c) shows the distribution of the parameter p_1 before and after optimization of the corresponding DACs.

The linearized pulse height curve can be parametrized by the slope (gain) and offset (pedestal) of a linear fit. The distributions of gains and pedestals for all pixels are presented in figure 5. Within a ROC the gain and pedestal variations are smaller than those in figure 5. Per ROC the average RMS of the gain distribution is 9.7×10^{-2} ADC/DAC and the RMS of the pedestal distribution is $1.6 \times 10^3\,\mathrm{e}^-$.

3.1.4 X-ray calibration

The X-ray calibration has a twofold purpose: the testing of the module response to the charge injected to the silicon sensor, and the calibration of the internal signal of each ROC. An X-ray source with Americium-241 as a primary source and different targets (Mo(4844 e$^-$), Ag(6139 e$^-$)) has been used for the test. First, the $V_{\rm cThr}$ value which corresponds to the injected charge has been determined for both sources. Then, the amplitude of the calibrate signal which corresponds to this

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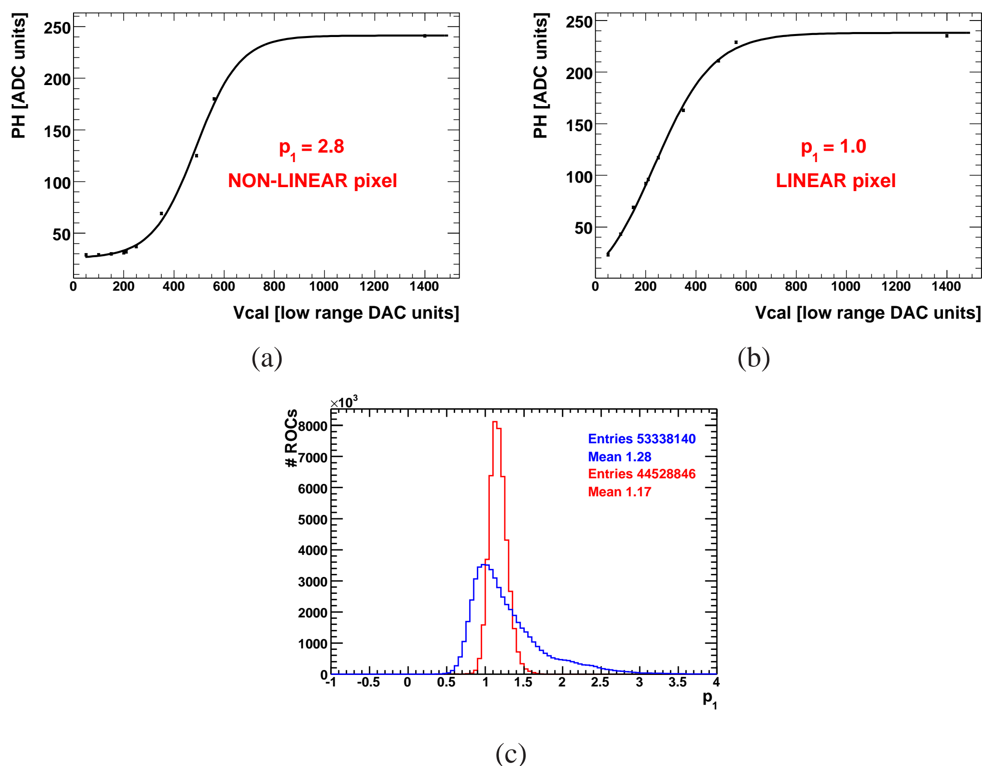

Figure 4. Non-linear (a) and linear (b) pulse height curves fitted with hyperbolic tangent function and the distribution (c) of the parameter p_1 before and after optimization for all pixels.

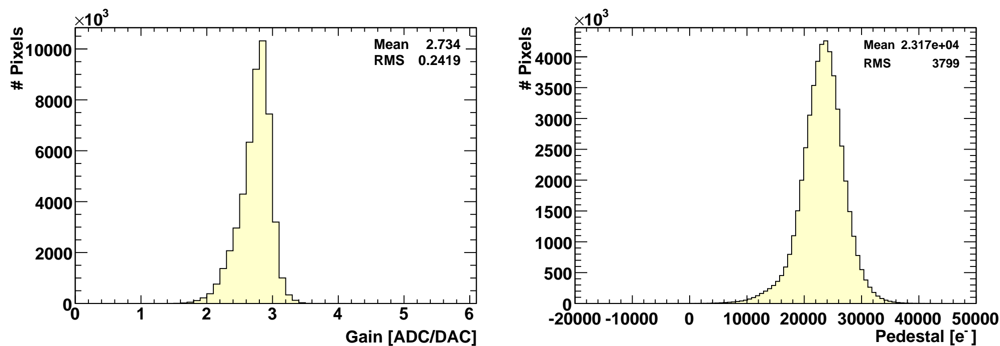

Figure 5. Gain (left) and pedestal (right) of the linear part of the pulse height calibration curves.

threshold has been measured. The calibration curve is linear in the range of interest, thus the slope and offset can be calculated from the two measured points. The average slope is 65.5±8.9 e^- per V_{cal} unit and the average offset is -414±574 e^- (see figure 6).

3.2 Module grading and test results

The grading scheme for modules comprises three categories A, B and C and is shown in table 1. Modules with grade A have no or only minor defects. Modules with grade B are of lower quality than modules with grade A, but are still working acceptably well. Modules with grade C are seri-

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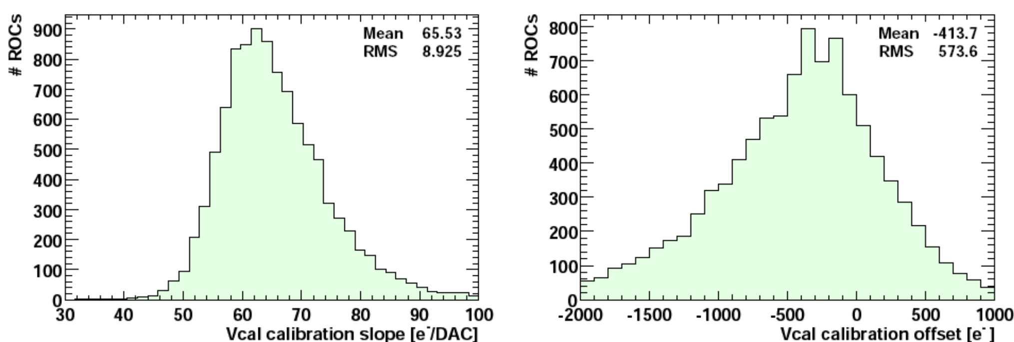

Figure 6. Slope (left) and offset (right) of the calibration curve V_{cal} versus ionization charge.

ously flawed or not working at all and were not used in the detector construction. The qualification criteria are divided into three groups: pixel defects, ROC performance and sensor leakage current.

A pixel is counted as defective if:

- it does not respond to the injected calibrate signal,
- a bump bond is missing or defective,
- any of the four trim bits is not working,
- it cannot be masked,
- its address cannot be decoded.

A ROC can be disqualified by the results of the noise measurement, trimming and pulse height calibration. For non-irradiated modules the threshold will be set at 2000-2500 e^-, hence the average noise level should be less than 500 e^- and the spread less than a few hundred electrons. After trimming, the RMS of the pixel threshold distribution is required to be less than 200 e^-. The spread in the gain and the pedestal is acceptable if the mis-calibration contribution to the track and vertex reconstruction is less than the effects of multiple scattering and misalignment. According to [4], the tolerable variation of the gains is about 20-40% and the pedestal variation might be as large as 1000-2000 e^-.

To detect eventual sensor damage during assembly, the limits for the leakage current were defined as shown in table 1. The leakage current at the initial operational voltage of 150 V should be less than 2 μA. With increasing radiation damage the modules will be operated at increasing depletion voltage V_{OP}. In order to ensure reasonable behavior at higher operating voltages a limit was set on the slope of the I-V curve $I(V_{\mathrm{OP}})/I(V_{\mathrm{OP}} - 50\ \mathrm{V}) \leq 2$.

The grading criteria for the sensor leakage current were defined at room temperature. Therefore, the leakage current measured at -10°C had to be recalculated to the corresponding leakage current at room temperature. The limit for the recalculated current was set 1.5 times higher than for the measured current.

In total 948 module have been tested, out of which 827 were full modules and 121 half modules. 565(87) full(half) modules have been graded as A. 161(23) modules have been graded as B. The remaining 101(11) modules have been graded as C. This leads to an overall yield of 88%(91%).

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Table 1. Grading criteria based on pixel defects, chip performance and the sensor leakage current.

	Pixel	Mask	Noise	Gain	Pedestal	Thr.Width	$I^{\mathrm{meas}}_{+17}(150\mathrm{V})$	$I^{\mathrm{calc}}_{-10}(150\mathrm{V})$
A	$\leq 1\%$	0	$\leq 500e^{-}$	$\leq 10\%$	¡2.5ke^{-}	¡200e^{-}	¡2μA	¡3μA
B	$\leq 4\%$	0	$\leq 1000e^{-}$	$\leq 20\%$	¡5.0ke^{-}	¡400e^{-}	¡10 μA	¡15μA
C	$> 4\%$	≥ 1	$\geq 1000e^{-}$	$> 20\%$	¿5.0ke^{-}	¿400e^{-}	¿10μA	¿15μA

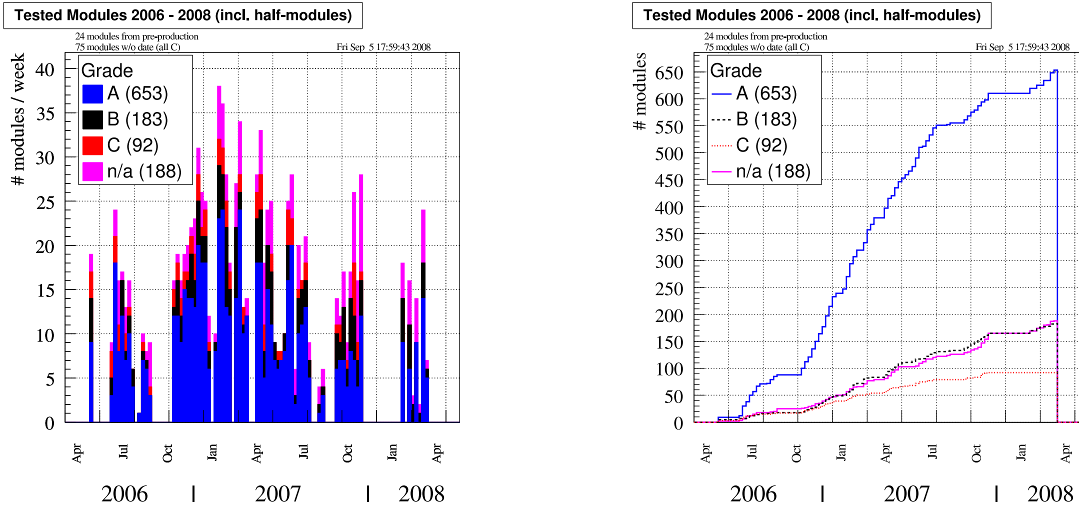

Figure 7. The module production rate (left) and the cumulative number of modules (right) produced and tested versus time.

Figure 7 shows the production rate and the cumulative amount of modules produced and tested versus time.

4 Integration and Commissioning of the CMS barrel pixel detector

The mechanical support structure on which the modules are placed and the so-called supply tubes which accommodate the detector readout and control electronics were fabricated at the University of Zurich. The integration of the CMS pixel detector took place between December 2007 and May 2008. The modules were mounted on the support structure at PSI while the assembly of the supply tubes happened at the University of Zurich. The final system was assembled and tested at PSI, transported as a whole to CERN and installed into CMS. The experiences of the commissioning, first at PSI and after the installation at CERN, will be discussed in the following.

4.1 Module mounting

The 768 modules of the barrel pixel detector were mounted manually on the carbon support structure. The support structure is divided into 6 half cylinders forming two independent detector half shells with 3 layers. The base plates of the modules were fixed with screws to the inner and the outer surface of the half cylinders. Sophisticated tools were developed to facilitate the demanding mounting procedure.

The mounting procedure consisted of different steps:

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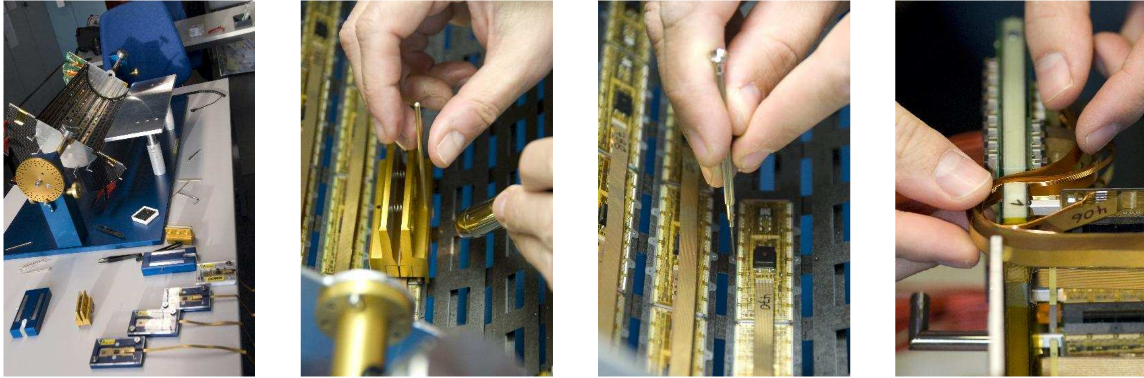

Figure 8. 1. Working place for the detector assembly. 2. Placing the module on the shell. 3. Screwing the module to the shell. 4. Placing cables at the end-flange.

- setting the TBM address,
- cutting and bending the signal and power cables according to the module's position on the support structure,
- soldering a plug to the power cable,
- screwing the module to the support structure,
- assembling the three layers of a half shell,
- connecting the module cables to a 6 layer PCB placed on the detector end-flange,
- testing the basic functioning of the modules.

The procedure proved to be very efficient and up to 60 modules could be mounted in a day. Only three modules were destroyed during the assembly, 10 modules were damaged but could be repaired and used in the final system. However, the replacement and repair of a broken module was an extremely delicate operation with a high risk of inducing more damage to the system. In the last iteration of testing at PSI, three modules were found to be non-working.

When the barrel pixel detector was fully assembled a clearance test between the two half shells was performed. The test showed that the cables of the closely approaching half modules have to be slightly rearranged in order to provide enough clearance for the installation of the detector.

4.2 Supply tube assembly

The readout and control circuits of the pixel detector are integrated on the supply tube. The supply tubes are a complex system as well in design as in production due to the thin radial shell thickness (1-2 cm), the large number of circuits, plugs and sensors, and the fine wires and thin printed circuit boards that were used.

The pixel detector readout system is described in detail in [10, 11]. The communication between the detector and the front-end modules in the underground service room is provided by optical links. The electronics of the readout and control circuits are placed on the supply tube together with the temperature and humidity sensors. In addition the supply tube brings the power and

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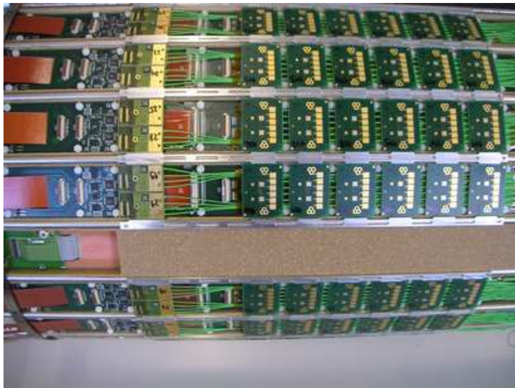

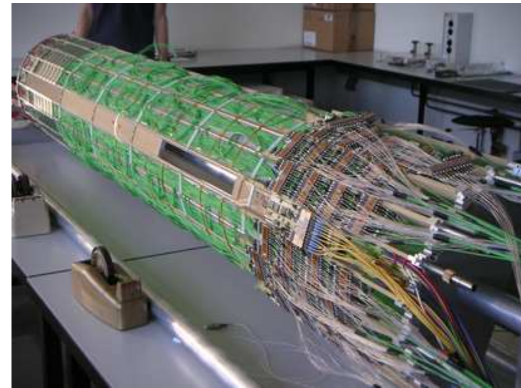

Figure 9. One of the four barrel pixel supply tubes during assembly. On the left hand side, a closer view to the detector near side equipped with AOHs, DOHs, Delay25, PLL and gate keeper chips is presented. On the right hand side, the arrangement of the optical fibers is illustrated.

cooling lines to the detector. The final system consists of two independent half cylinders, an inner (+x) and an outer (-x), with a detector half shell and two supply tubes.

The barrel pixel readout system is organized into 64 independent readout groups consisting of analog and digital opto-hybrid circuits which serve 8, 12 or 16 modules.

A supply tube is divided into 8 sectors which contain the power lines and the readout and control electronics of two readout groups. One sector includes an analog opto-board with 6 analog opto-hybrids (AOHs), a digital opto-board with two digital opto-hybrids (DOHs), two PLL chips, two Delay25 chips and two gate keeper chips. A total of 192 AOHs and 72 DOHs are used for the pixel barrel detector. To program the AOHs, DOHs and other components the standard CMS ring architecture is implemented with a front-end controller (FEC) and 9 communication control units (CCUs). A CCU board equipped with 2 DOHs and 9 CCUs is mounted on each supply tube, 8 CCUs each service one sector, the last CCU is used for redundancy.

The analog signals are sent to 32 front-end drivers (FEDs) which digitize the signals, build event fragments and send them to the central data acquisition. The stability of the analog signal is strongly affected by the undesirable temperature dependence of the AOHs. The level of the analog signal is shifted by 50 ADC counts when the temperature of the AOH changes by 1 °C. The FED is able to internally correct for a drift within a temperature range of $\pm 2\,^{\circ}$C. Consequently, the temperature of the AOHs has to be controlled within a very narrow range in order to assure a stable operation of the detector. The barrel pixel supply tubes are equipped with a total of 124 temperature sensors and 8 humidity sensors. The temperature sensors are placed on the CCU boards, the AOH motherboards and on the supply tube cooling lines.

Figure 9 shows the supply tube during the assembly. The main challenge in the assembly of the supply tube was the arrangement of the 1440 single optical fibers. To guarantee maximum light transmission the bending radii have to be more than 5 cm which made the management of the slack of the fibers difficult.

All components were tested during mounting. A standard PC with a FEC card was used to send the clock and the control commands to the CCUs. In a first step, the proper working of the ring architecture, the redundancy mechanism and the communication with the I2C devices on the digital opto-board was verified.

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Each DOH holds four optical fibers, two fibers are used for sending and returning the clock and trigger signal, the other two are used for the propagation of the control data. The functioning of these fibers in every readout group was tested in the next step. A 40 MHz clock signal was injected in each channel and the returned signal was checked with an oscilloscope. No broken DOHs were found.

The light transmission of the AOHs was checked by increasing the bias of the laser and measuring the output light intensity. 10 AOHs (out of 192) had to be replaced during the assembly due to broken wire bond connections of the laser.

An active cooling has to be provided in order to improve the temperature stability of the AOHs and the DOHs. For this reason, aluminum plates were placed on top of the AOHs and DOHs which connect them to the supply tube cooling lines.

In a final step, the power and control cables for each sector and the central slot were mounted on the supply tube.

4.3 Integration of the final system

The assembly of the detector with the supply tubes was done at PSI. The detector together with the supply tubes were integrated in two 5m long transport boxes which were designed for the installation into CMS. Within the transport box the detector was placed on wheels on a rail system which then could be used to slide the pixel detector inside CMS.

Each sector of the supply tube is connected with 4 Kapton cables (for digital and analog signal transmission of the two readout groups) and a power cable for low and high voltage to the PCB mounted on the detector end-flange. The PCB distributes power and signals to the individual modules.

Silicon rubber hoses fixed with aluminum clips provide the link between the aluminum cooling lines of the detector mechanics and of the supply tubes.

For testing purposes, a commissioning system with the true mechanical structure and prototype supply tubes was assembled first. In the commissioning system only two sectors were equipped with modules. The two halves of the final system were assembled and tested within only two month in May and June 2008. A picture of the pixel detector with the two supply tubes can be seen in figure 10.

At PSI one sector of the pixel detector could be connected to the readout system at a time. The readout system used the same FED and FEC modules which will be used during data-taking at CERN.

For each sector of the supply tubes the tests that were done before the integration were repeated: the proper working of the CCUs was verified, the I2C communication was tested and the clock and trigger distribution was checked. The signal to noise behavior of the analog optical fibers was tested by taking a calibration curve over the full laser bias range. An example is shown in figure 11. Channels with a noise value of more than 4 ADC counts were improved by re-cleaning the optical connections. The digital read-back of every module was verified, the separation of the analog address levels was determined, the pixel response to the internal calibrate signal was checked and the high voltage supply of each module was tested.

The number of dead channels was found to be less than 0.3%. The dead channels are due to one module without high voltage connection, two modules with a broken token passage and one

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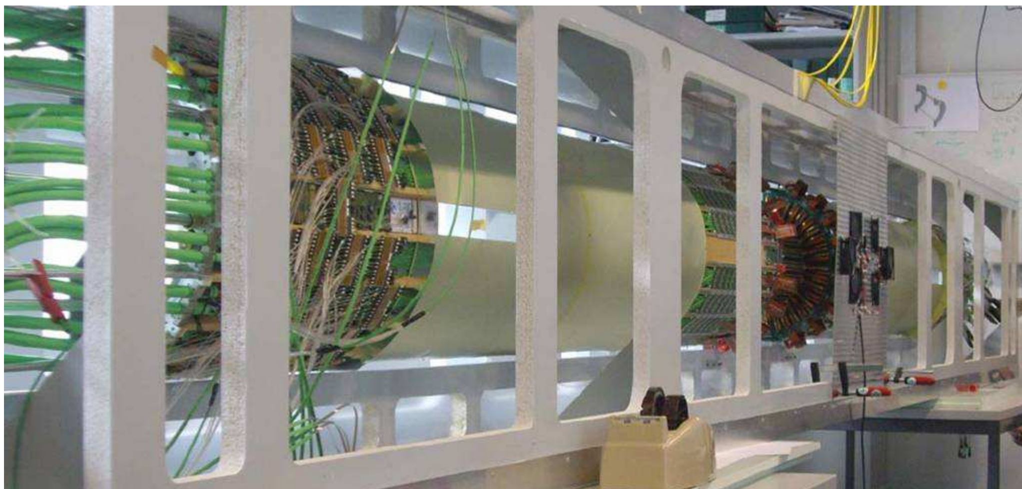

Figure 10. Half of the barrel pixel detector integrated with two supply tubes in a 5m long transport box.

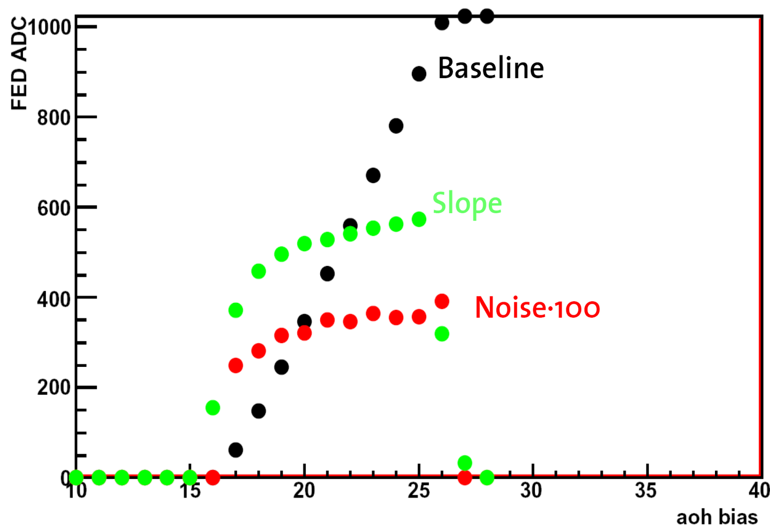

Figure 11. Baseline, slope and noise of an optical fiber as function of the bias of the laser measured at the FED. The response is highly temperature dependent.

module with a bad ROC header. In addition, a sector without digital read-back was found and two broken AOHs channels were observed. The former issue does not influence the analog readout and the latter was recovered by rerouting the signal through another channel.

The functioning of the temperature and humidity sensors was tested using the detector safety system [11]. One single temperature sensor was found to be non-working. The pixel cooling system uses C_6F_{14} as cooling fluid. A leak test of the 10 cooling lines of each half detector was performed by filling the lines and monitoring the amount of coolant. No leaks were detected inside the pixel system.

4.4 Commissioning at CERN

The pixel system was shipped by truck from PSI to CERN. In a test ride with the commissioning system in April 2008, the mechanical stress on the system was evaluated by measuring the shocks

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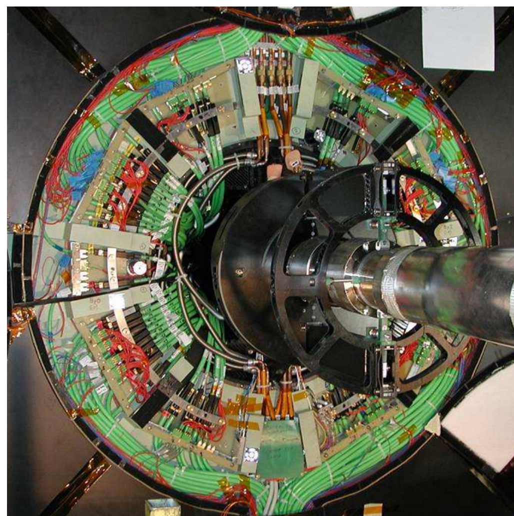

Figure 12. View of the barrel pixel detector in its final position inside CMS. On the left hand side, the central beam pipe and the detector end-flanges with cooling lines and power and signal cables can be seen. A picture of the connection area PP0 is shown on the right hand side.

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during the transport with an accelerometer. The transport of the final system took place on July 15. Before the installation, the system was fully tested at CERN and no additional damage was found.

4.4.1 Installation into CMS

The pixel detector is installed in the small volume between the beam pipe and the silicon strip tracker. A system with bending rails on top and bottom inside CMS was designed to insert the barrel pixel detector and the supply tubes along the beam pipe. A clearance of 7-8 mm to the beam pipe was calculated in simulations and checked with the help of a mock-up.

On April 25 the commissioning system was shipped to CERN and a test installation took place. The system was craned down to the cavern through the main shaft and lifted to the installation table. Temporary rails were used to extend the rails from the transport box to the rails inside CMS.

The installation of the commissioning system went smoothly and was finished within less than four hours. The power cables and the optical fibers of the equipped sector were connected to the patch panel 0 (PP0) and the correct cable lengths were verified. The installation test did not show any need for mechanical adjustment before the final installation.

The installation of the final system started on July 23. Both halves of the detector were lowered into the cavern the same day. The insertion of the inner shell was completed without any problems and all the connections were made, a total of 40 power and control cables and 16 multi-fiber ribbons. In order to make a fast check-out possible a temporary cooling system was used.

The second shell was inserted the following day. The first tries failed due to a collision of the inner and outer detector end-flange. This problem has been solved by mechanically modifying the suspension of the insertion wheels to allow for a larger clearance between the two half shells. All power and control cables and all optical fibers of the barrel pixel detector were connected by July 24.

A picture of the detector in the final position and the connection area PP0 is shown in figure 12. The barrel pixel services had to be disconnected again when the final cooling tubes were joined and when the forward pixel detector was installed.

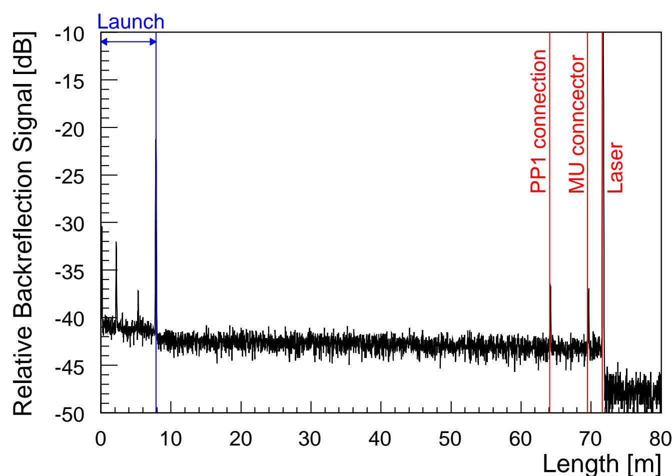

Figure 13. OTDR measurement of a fiber with a reflection peak at the MU and the PP1 connection.

The cooling lines of the pixel supply tube were connected to the cooling system using stainless steel flexible pipes. In the first running period after installation the cooling fluid had a temperature of +17°C. The 10 barrel pixel cooling loops do not show any leak. After about a week of daily turning on and off, the cooling system went into stable operation.

4.4.2 Testing after installation

The optical signals pass four connection points before they are translated into electronic signals in the front-end modules in the service room: a single fiber (MU) connection on the supply tube located at 2 m distance from the laser, a multi-fiber (ribbon) connection at the pixel detector PP0 at a distance of 3 m, a multi-ribbon connection at the strip tracker PP1 at 7 m distance and a connection to the front-end modules at 63 m distance.

The pixel fibers which connect PP0 and the counting room were laid out and tested in spring 2008. The PP1 connection at the strip tracker end-flange was not accessible at the time of the barrel pixel installation.

The digital-optical ring was tested by sending and receiving a 40 MHz clock signal, for the analog-optical lines the scan of the laser bias range was repeated. After three iterations of re-cleaning the PP0 connections, the optical fibers for the transmission of the digital signal showed an excellent performance while 29 out of 96 ribbons of the analog readout were spotted to contain noisy fibers. These 29 ribbons were investigated with the help of an optical reflectometer (OTDR) and a visual inspection of the connection to the FED. The OTDR measurement did not show any reflection at the PP0 connections which means that an optimum light transmission is provided. However, in 19 cases a reflection peak at a MU connection was spotted. In 11 cases this reflection influences either the noise or the slope of the calibration curve for the corresponding channel. In addition, a bad PP1 connection was found. The four fibers passing through that connection could be recovered by using a spare ribbon. An example of the OTDR measurement of a fiber with a reflection at the MU and the PP1 connection is shown in figure 13.

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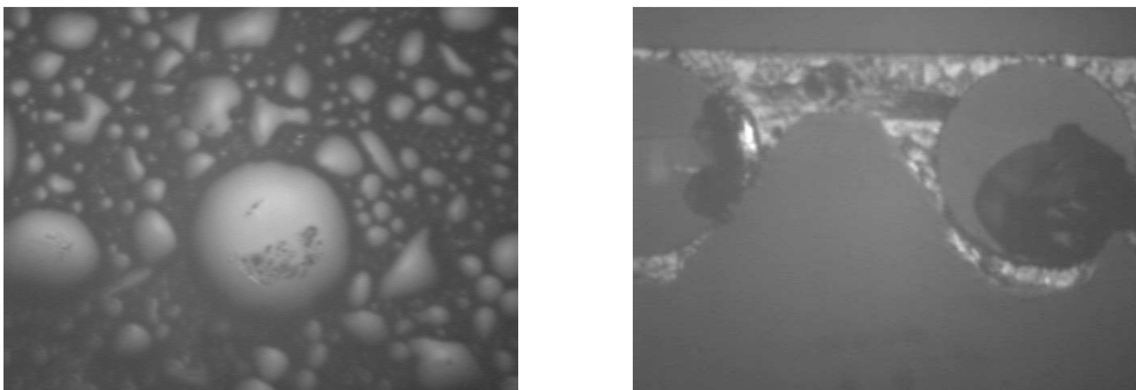

Figure 14. Microscope picture of a FED connection with marks on the fibers.

The visual inspection of the connection to the FED was performed with a microscope and 19 ribbons with marks on the fibers were spotted. In about 50% of the cases cleaning was successful and slightly improved the noise behavior. A microscope view of the FED connection with marks on the fibers can be seen in figure 14.

During all operation not a single optical fiber of the barrel pixel detector was lost.

The testing of the pixel system started as soon as the pixel services were connected and cooling was available. After a first check-out 9 (out of 32) sectors were observed having serious problems which would have prevented them from producing valid data. Except for one sector where a configuration error was located, all failures were caused by connection problems with the power supplies. Three power supply modules had to be replaced for the other 5 sectors the failure was cured by improving the connections.

On July 29 all sectors of the barrel pixel detector were working satisfactorily so that the construction of CMS could proceed with the installation of the forward pixel detector. On August 7, all access to the pixel detector was lost when the closing of the CMS detector started.

During further testing, an additional four modules were found to be broken after the installation: three modules without high voltage connection, one module with a bad ROC header and one module that cannot be programmed. Furthermore, 4 individual ROCs do not produce valid signals. An additional module with a bad TBM header could be recovered by rerouting the signal through the other TBM.

In summary, the barrel pixel detector shows an excellent performance with a working fraction of 99.13%. Details about the performance of the barrel pixel detector during calibration and data taking can be found in [12].

5 Conclusions

The CMS barrel pixel detector has been built, tested and successfully installed in about 2.5 years, from April 2006 until September 2008. The module production and testing was done in-house at PSI. Thanks to the development of dedicated tools and automated testing and qualification procedures a high production rate of high quality components could be achieved. The module production had an overall yield of 88%. The elaborated procedures for the module mounting, the supply tube assembly and the integration of the final system assured a fast and safe workflow with a very low

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loss rate. The barrel pixel detector was installed into CMS within only a few days. The first tests after the installation showed an excellent performance with less than 0.87% of dead channels.

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