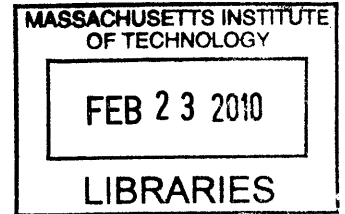


Equalized On-Chip Interconnect: Modeling, Analysis, and Design

by

Byungsub Kim

B.S., EE, Pohang University of Science and Technology, 2000
M.S., EECS, Massachusetts Institute of Technology, 2004



Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

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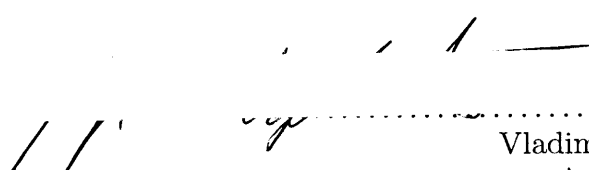
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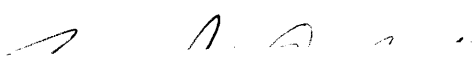
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Abstract

This thesis work explores the use of equalization techniques to improve throughput and reduce power consumption of on-chip interconnect. A theoretical model for an equalized on-chip interconnect is first suggested to provide mathematical formulation for the link behavior. Based on the model, a fast-design space exploration methodology is demonstrated to search for the optimal link design parameters (wire and circuit) and to generate the optimal performance-power trade-off curve for the equalized interconnects. This thesis also proposes new circuit techniques, which improve the revealed demerits of the conventional circuit topologies. The proposed charge-injection transmitter directly conducts pre-emphasis current from the supply into the channel, eliminating the power overhead of analog current subtraction in the conventional transmit pre-emphasis, while significantly relaxing the driver coefficient accuracy requirements. The transmitter utilizes a power efficient non-linear driver by compensating non-linearity with pre-distorted equalization coefficients. A trans-impedance amplifier at the receiver achieves low static power consumption, large signal amplitude, and high bandwidth by mitigating limitations of purely-resistive termination. A test chip is fabricated in 90-nm bulk CMOS technology and tested over a 10 mm, $2\mu\text{m}$ pitched on-chip differential wire. The transceiver consumes 0.37-0.63 pJ/b with 2-6 Gb/s/ch.

Thesis Supervisor: Vladimir M. Stojanović

Title: Associate Professor

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Chapter 1

Introduction

1.1 Application and Problem Overview

As the number of cores in processor chips increases under tight power and area constraints, networks-on-a-chip (NoCs) [2–6] are increasingly used to provide efficient all-to-all connectivity between on-chip modules. With increased focus on energy-efficiency and bandwidth density, NoC architectures are changing from traditional simple low-radix, high-diameter mesh networks (Figure 1-1 (a)), toward increased concentration, lower diameter, and higher-radix NoCs (Figure 1-1 (b), (c), and (d)) [7–10]. To ease programming and keep the bandwidth and latency relatively uniform under different traffic, higher-radix NoCs like a flattened butterfly (Figure 1-1 (c)) or a Clos (Figure 1-1 (d)) are preferred [1, 8, 11]. Both trends create the need for energy-and-area-efficient, fast, mid-range and global on-chip interconnects. Figure 1-2 shows example layouts of two NoC topologies: a concentrated mesh and a flattened butterfly with various interconnects assuming 2cm x 2cm processor die size. To construct the topologies, 5-mm, 10-mm, and 15-mm long interconnects must connect routers under power and metal area constraints. However, the power inefficiency and latency constraints of the traditional repeater insertion techniques [1, 12, 13] limit the application of these to less advanced NoC architectures.

To overcome these interconnect limitations, several signaling techniques have been explored in the past, mostly focusing on latency limits - RF interconnects [14, 15], a negative-impedance repeater [16], and a pulse-width modulated interconnect [17–19]. Only recently, equalization at the transmitter and receiver over RC-limited wires [15, 20–25] has been proposed as a way to improve not only the latency but also the energy and area (throughput)

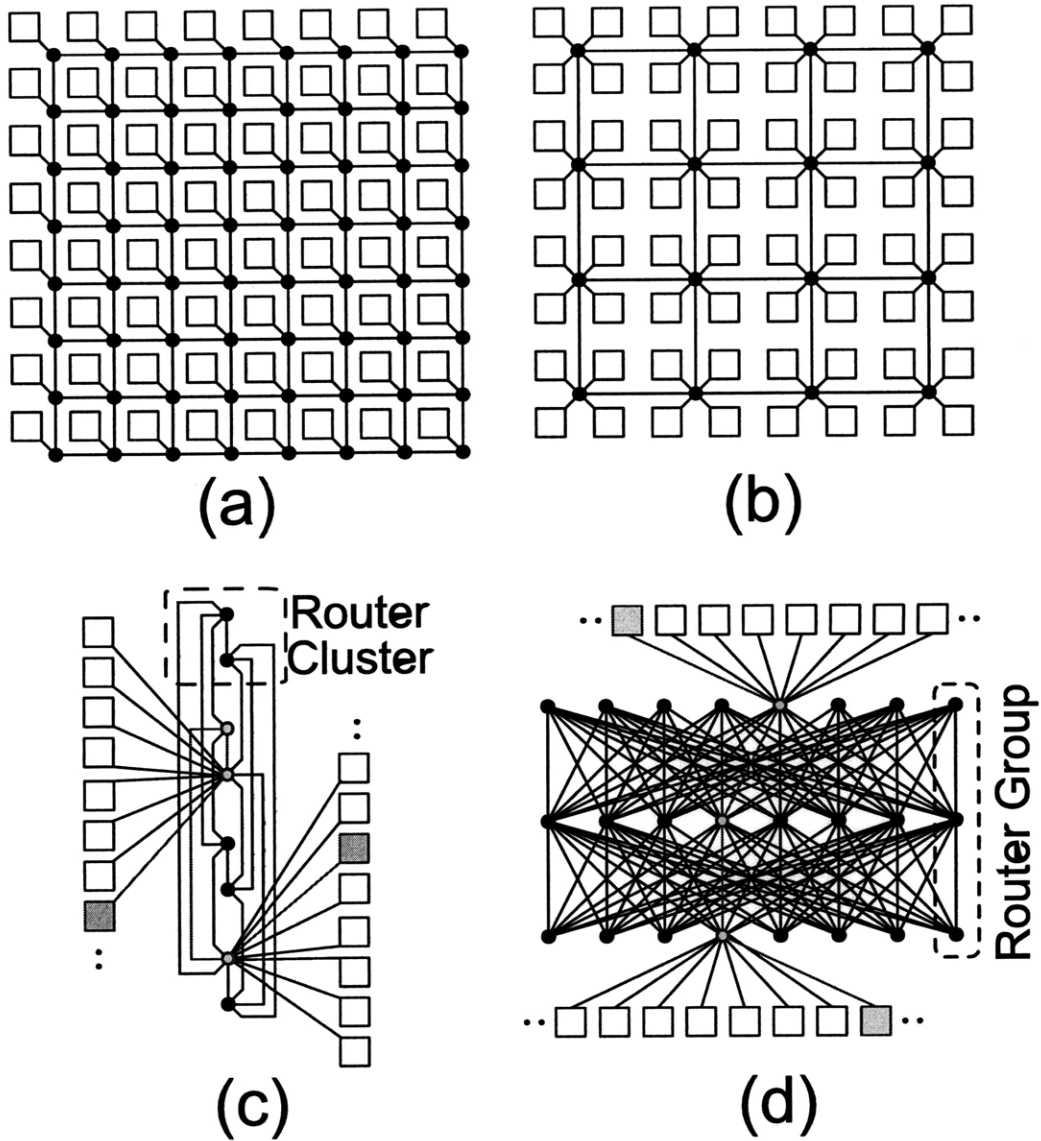


Figure 1-1: Logical view of 64-tile network topologies - (a) 2D 8x8 mesh, (b) concentrated mesh (Cmesh) with 4x concentration (c) a variation of 8-ary 2-fly flattened butterfly (flat-Fly) (d) 8-ary 3-stage Clos network with eight middle routers. In all four figures: squares = tiles, dots = routers. In (a), (b), and (c) inter-dot lines: two opposite direction channels. In (d) inter-dot lines: unidirectional channels [1].

efficiency, which are the key system metrics in the NoC context.

An equalizing transmitter flattens the overall link transfer function by suppressing the low frequency portion of the wire channel response. This eliminates the inter symbol interference (ISI), allowing faster data transfer at reduced power consumption, since the

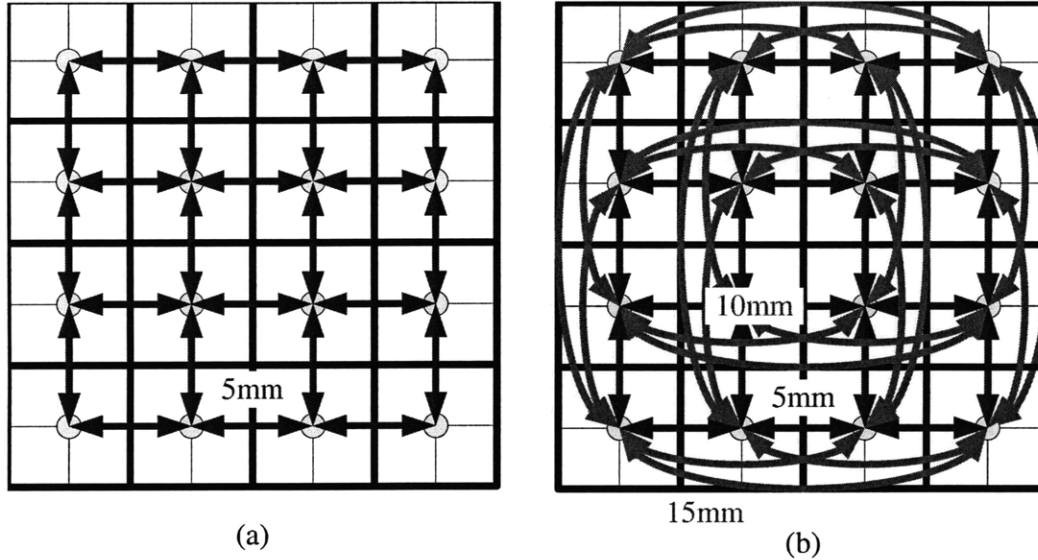


Figure 1-2: Global interconnects in modern NoC topologies: (a) concentrated mesh (b) flattened butterfly

suppression of low frequencies of the signal effectively decreases the voltage swing along the channel.

Although the benefits of equalization have been well recognized in off-chip applications, the impact on on-chip interconnects is debatable without a deeper study of the on-chip equalization environment since the answer is highly dependent on the additional power and area overhead of equalization circuits when the link is reasonably well optimized. Previous studies [18, 19] could not fully demonstrate the advantages of equalization over repeater insertion because the circuit techniques were not energy-efficient, and the wire-circuit simulation was not fully utilized to optimize the link. This is in part due to the lack of a proper modeling and analysis framework for an on-chip equalization and in part due to the lack of efficient equalization circuit techniques. This thesis work overcomes both limitations by first providing metrics for modeling and analysis and also improving circuit design based on this exploration. The modeling, analysis, and the circuit techniques described in this thesis can be applied to various other RC-dominant interconnect applications such as a silicon carrier and a display backplane.

1.2 Introduction to Equalization

In this section, we give a brief overview of link equalization in order to set the background knowledge for the rest of the thesis.

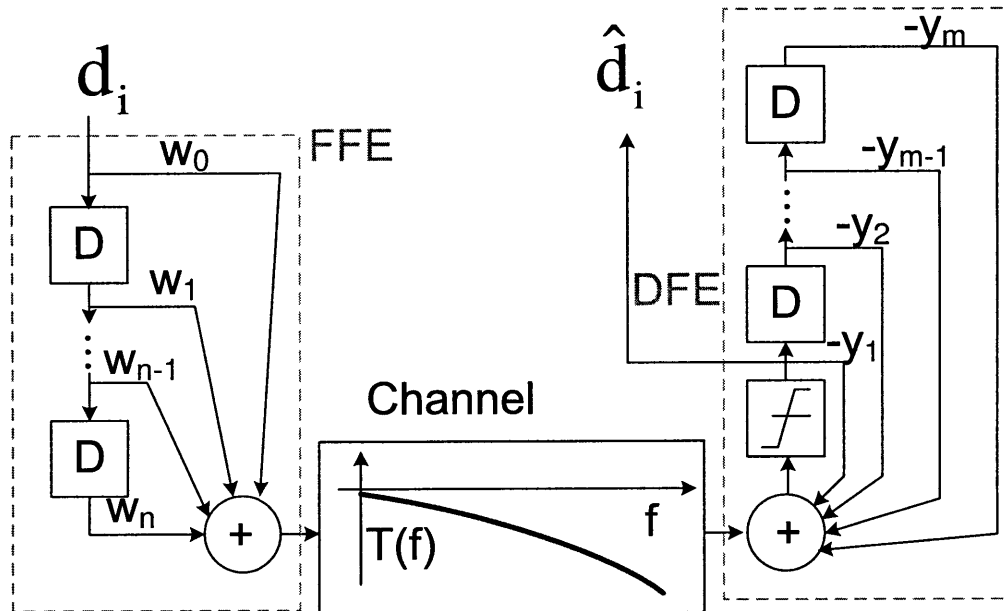


Figure 1-3: Typical Equalization Architecture

Figure 1-3 shows a block diagram of a typical high speed link system with an N-tap Feed Forward Equalization (FFE) transmitter (Tx) and a M-tap Decision Feedback Equalization (DFE) receiver (Rx) over a bandlimited channel. Figure 1-4 shows example pulse responses of equalized and unequalized channels. The channel typically has strong low-pass filtering (LPF) behavior, and therefore, the response of the unequalized square pulse (dashed-blue curve in Figure 1-4) creates inter-symbol interference (ISI) (solid-blue in Figure 1-4) that limits achievable data rate. To eliminate ISI, the Tx FFE is typically designed as a mixed-signal finite impulse response (FIR) filter which inverts the LPF characteristic of the channel [26]. The example transmitted 3-tap equalized pulse (dashed-red curve in Figure 1-4) efficiently eliminates ISI (solid-red curve in Figure 1-4). At Rx, a DFE is often used to further eliminate ISI after FFE. The solid-red waveform in Figure 1-4 has one post cursor remaining after FFE. In a typical RC-dominant wire, the remaining DFE tap can be efficiently eliminated by the 1-tap DFE architecture of Figure 1-3.

To easily explain energy efficiencies of two different interconnects - a repeated intercon-

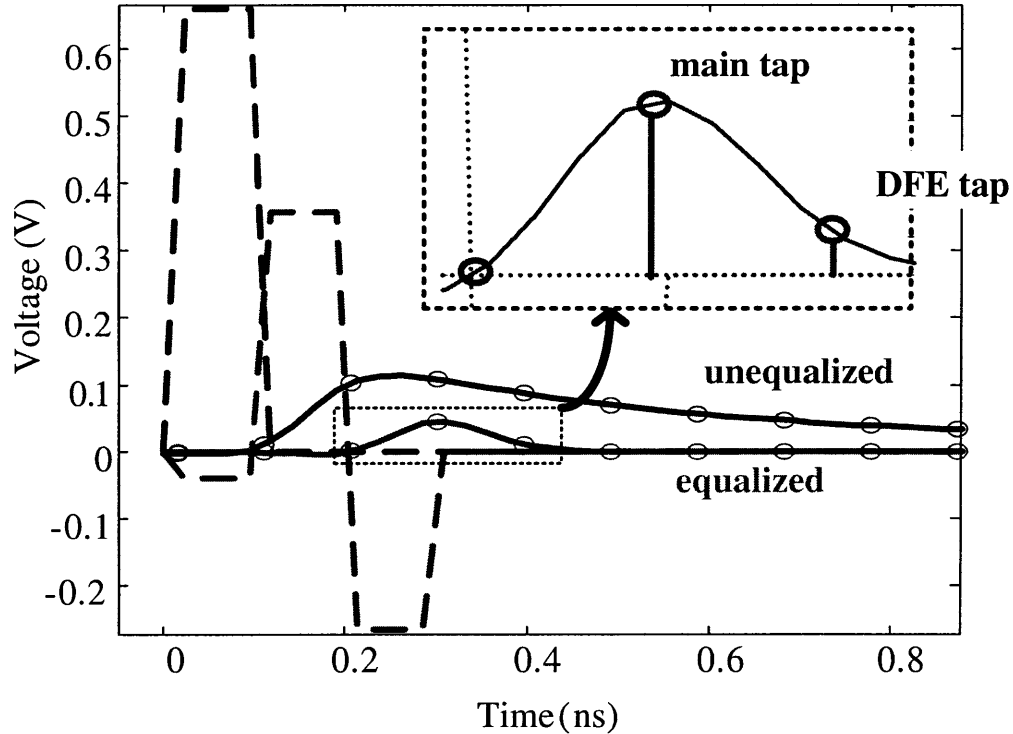


Figure 1-4: An example of equalized and unequalized pulse response

nect and an equalized interconnect - Figure 1-5 conceptually visualizes the voltage swing of two interconnects along the wire distance from the transmitter. As shown in Figure 1-5 (a), the voltage level of the repeater is either V_{dd} or G_{nd} along the wire since the inserted repeater is designed to completely pull up or down the repeater segment voltages. Therefore, per each bit transition, the voltage swing is always V_{dd} , and thus the energy per rising transition is proportional to CV_{dd}^2 where C is the wire's total capacitance. In an equalized interconnect, the voltage swing is effectively reduced due to the channel attenuation. As shown in Figure 1-5 (b), the signal amplitude is large at the transmitter side and small at the receiver side due to the channel attenuation. As a result, the power consumption to drive the wire can be reduced.

1.3 Thesis Contributions

The contributions of this dissertation include mainly two parts. The first is the analysis and modeling of the equalized on-chip interconnect. The second part is a new equalization circuit

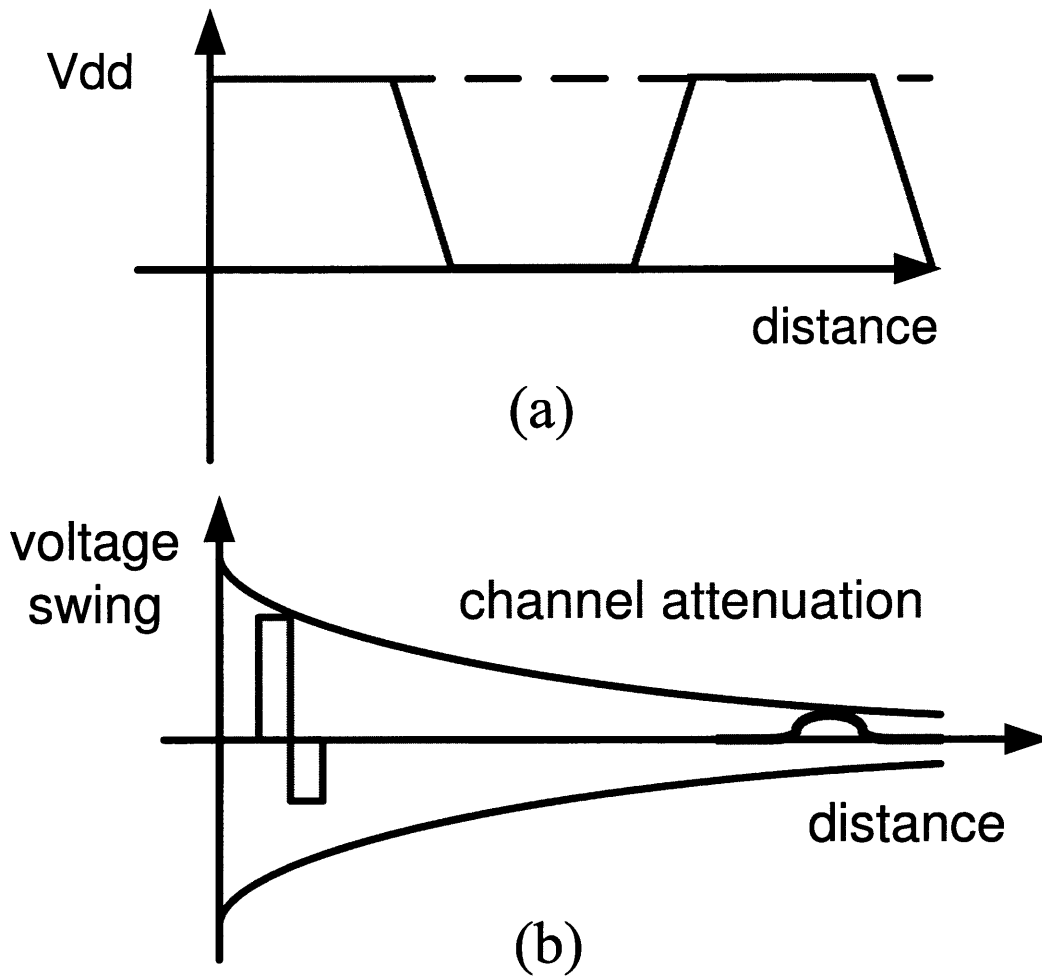


Figure 1-5: Conceptual voltage swing comparison: (a) a repeated interconnect and (b) an equalized interconnect.

technique that significantly improves performance-cost efficiency. The proposed circuits also have the potential to be used effectively in a wide range of applications (from off-chip links to new emerging silicon carrier technologies or flat panel displays)

1.3.1 Analysis and Modeling

This dissertation defines interconnect metrics and provides the first complete performance and power model of equalized on-chip links. Most previous models used for on-chip links are many stage RC-ladders or π -models which are not suitable to guide the designer in making

decision about equalized link circuits and wires. This thesis will provide mathematical tools for on-chip equalized interconnect modelings which couple circuit and wire modelings and are intuitive and accurate enough to guide a designer in on-chip link design exploration. This thesis also demonstrates that a computer-aided-design (CAD) tool based on the analytical model with simplified/linearized wire and circuit parameters as well as link parameters can find optimal link design parameters in a large design space within relatively short time. This tool has also been effectively used to provide equalized link metrics for the event-driven network-level traffic simulator in order to estimate the NoCs performance-power trade-off.

1.3.2 Circuit Design

This dissertation also demonstrates a new architecture and circuit implementation of a high-data rate and energy-efficient equalized transceiver for RC-limited on-chip interconnects. The new charge-injection transmitter directly conducts pre-emphasis current from the supply into the channel, eliminating the power overhead of analog current subtraction in conventional transmit pre-emphasis, while significantly relaxing the driver coefficient accuracy requirements. The transmitter utilizes a power efficient non-linear driver by compensating non-linearity with pre-distorted equalization coefficients. A trans-impedance amplifier at the receiver achieves low static power consumption, large signal amplitude, and high bandwidth by mitigating limitations of purely-resistive termination. A test chip is fabricated in 90-nm bulk CMOS technology and tested over a 10-mm, 2- μm pitched on-chip differential wire. The transceiver consumes 0.37-0.63 pJ/b with 2-6 Gb/s/ch.

1.4 Thesis Organization

The rest of this dissertation is organized as follows.

Chapter 2 presents the modeling and analysis of the on-chip link interconnect. This chapter explains the link channel, including a physical view and the model of the wire as well as the termination impedances of the transmitter and receiver. It, then, compares different driver types in terms of power consumption and sensitivity. During the comparative analysis, it also suggests and explains the proposed Charge Injection Feed Forward Equalizing (CI FFE) driver architecture. Using the channel's transfer function and the driver model, the analytical equalization solution is explained. In the last section of this chapter,

a CAD tool using this model is demonstrated.

Chapter 3 describes a test chip implementation and measurement. The concept proposed in Chapter 2 is implemented in 90-nm CMOS technology. The test chip focuses both on the proof of the concept design for the two new circuit techniques: Charge-Injection Feed Forward Equalization (CI FFE) transmitter and Transimpedance Amplifier receiver as well as on a link vehicle that explores the trade-off between link-energy and throughput as well as the static and dynamic power components.

In Section 3.2 and 3.3, the CI FFE transmitter and TIA receiver are explained. In Section 3.5 of this chapter, the experimental results illustrate the effectiveness of the proposed schemes as well as the trade-off between energy and throughput.

Finally, Chapter 4 summarizes this dissertation work and concludes with future work and projections of equalization on an RC-dominant channel.

Chapter 2

Modeling and Analysis

The performance/power model of an equalized interconnect described in this thesis guides a designer towards a proper design parameter selection and enables CAD tool development to support the hierarchical NoC design by passing the network-relevant link metrics to the network design layer.

The design of an equalized interconnect is complicated since an equalized link includes many different design layers, such as a wire engineering layer, a circuit layer, and a link communication layer. Figure 2-1 shows a simplified model connection diagram for this thesis work. The bottom layer models - circuit and wire models - are combined together to estimate the equalized link performance and power. The estimated trade-off number can be then used for an NoC layer later. As can be seen in Figure 2-1, too many design layers and options could confuse a designer or require a lot of effort in the iterative optimization process. The wide range of parameters, such as driver size, supply and signal voltages, wire width and space, equalization coefficients, and sampling time complicate the design choice. Due to the absence of a proper model, early equalized on-chip interconnects were not appropriately optimized and suffered from performance degradation [18, 19]. Often research papers would have different conclusions regarding termination strategies [19, 22] due to lack of a clear picture of the link behavior and a simulation method for trade-offs between performance and power efficiency.

For the first time, this thesis work develops a modeling framework that explores link power and performance, connecting all the way down to the wire and circuit parameters. This comes from the model combining design parameters and power/performance of the

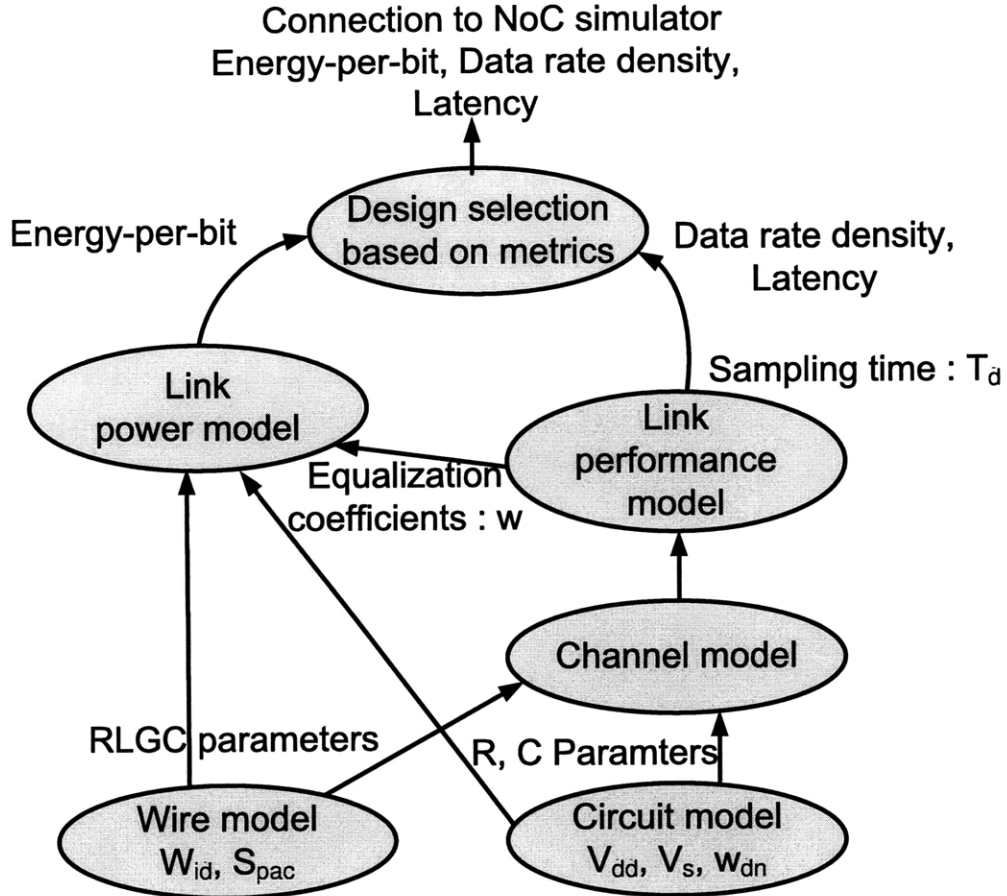


Figure 2-1: A simplified model connectivity diagram for an equalized link analysis tool.

link. The proposed model is based on the joint mathematical analysis of the wire, circuit, and equalization. Using the model, a fast design space exploration CAD tool that computes the link performance and power demonstrates usefulness of the equalized links in on-chip interconnect and NoC applications.

2.1 On-chip Interconnect Metrics

One of the unique features of an on-chip interconnect is the large demand for wiring in small metal area. According to Rent's rule, the number of wires out of a block is proportional to the number of logic gates inside the block to the power of a constant less than 1 [27, 28]. Therefore, as scaling continues, demand for high interconnect density will keep increasing and thus the RC-dominant nature of the on-chip interconnects will be the characteristics of

the future wires.

Unlike an off-chip wire, the on-chip interconnect has large channel attenuation for a short distance because the wire is thin and narrow. Increasing wire width may reduce resistance and increase inductance helping the channel loss. However, it also reduces the available number of wires and thus the aggregated data rate for a given cross-sectional metal area.

In metal-area- and power-constrained NoC design, we want to maximize the aggregated data rate (D_a) of an interconnect bundle through a given cross-sectional metal width (w_c) while satisfying the target latency (T_d) and a given interconnect power constraint. This problem is equivalent to maximizing data rate density (D_d) defined as data rate divided by cross-sectional pitch of each interconnect, while keeping the target latency and power constraints. In consideration of power consumption, regardless of the number of interconnects placed in the NoC, the fair comparison of the energy cost is the amount of energy to send one bit (E_b). Therefore, the optimization problem of an interconnect bundle is equivalent to the optimization problem for the following key metrics for each interconnect:

- data rate density: $D_d(\text{Gb/s}/\mu\text{m}) = \frac{D_a(\text{Gb/s})}{w_c(\mu\text{m})}$
- Latency: T_d (ps)
- Energy/bit: E_b (pJ/b).

2.2 Channel

Regardless to say, the channel is the most essential part of the high-speed wireline communication. Since equalization attempts to flatten the overall link transfer function, a good link cannot be designed without a proper modeling and analysis of the channel behavior. This section presents the analytical channel model for on-chip interconnect.

2.2.1 Overview of an RC-dominant Equalized Link Channel

Figure 2-2 describes the parameters and design-space of an equalized on-chip link channel consisting of the transmitter, wire, and receiver. Not only the wire, but also termination impedances affect the channel's transfer function. Therefore, the channel model must include transmitter and receiver circuits too, especially the termination impedances. A typical

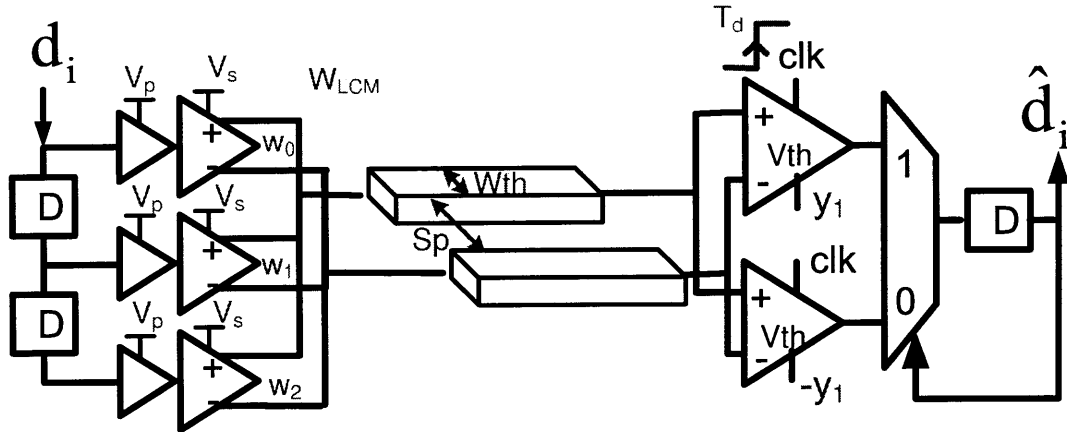


Figure 2-2: Overview of an RC-dominant Equalized Link Channel

transmitter consists of segments which are sized proportional to the FFE coefficients. The summation function of the FFE in Figure 1-3 is usually done through current summation or voltage division by tying up the segments. Typically, the output impedance of the transmitter is designed to be constant, and the transmitter can be modeled as a Thevenin/Norton source with FFE output value and a constant impedance as shown in Figure 2-4 in Subsection 2.2.3. At the receiver, the receiver input impedance works as the channel termination impedance. Therefore, a proper design of the receiver can improve the overall link performance. In the later part of this section, the transceiver and wire are modeled together to describe the transfer function of the channel.

2.2.2 Physical Model of On-chip Wires

The on-chip wires are modeled as lossy multi-port transmission lines with a standard stripline bus model sandwiched between two DC planes as shown in Figure 2-3. The top and bottom layers are typically filled with other signaling or supply wires but usually modeled as ground planes for simplicity [18]. In the final test chip design in Chapter 3, top M7 and bottom M9 layers are filled with supply grids and dummy metal pieces, respectively. The width and space are chosen $0.6\mu\text{m}$ and $0.4\mu\text{m}$ respectively in the final implementation in Chapter 3.

We choose narrow wire pitch for high wire density in contrast to the previous designs with wide interconnects [14–16, 19]. [14, 15] used $42\mu\text{m}$ and $12\mu\text{m}$ pitched transmission lines

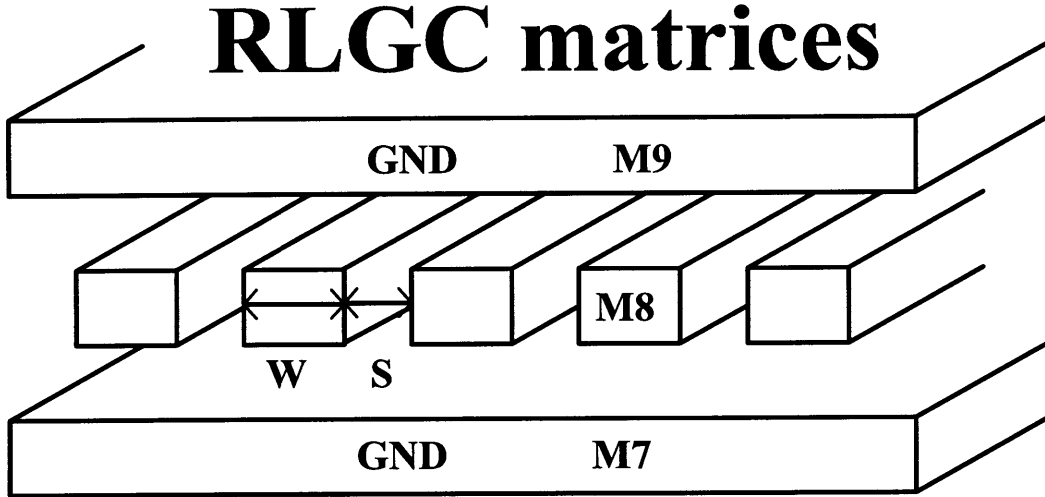


Figure 2-3: A 2D structural model of a wire

to reduce the channel loss of Radio Frequency (RF) carrier. [16, 19] used $32\mu\text{m}$ and $24\mu\text{m}$ pitched transmission line for loss compensation and easy equalization. However, these wide wire pitches significantly reduce the data rate density or the aggregated throughput over given metal area. [18, 22] used $1.6\mu\text{m}$ and $1.76\mu\text{m}$ pitched RC-dominant wires to achieve high data rate density. The wire used in the test chip described in this thesis has $2\mu\text{m}$ pitch which is comparable to the pitches in [18, 22].

Since we assume the uniform cross-section 2D structure, we use a 2D field solver to get *RLGC* matrices for multi-port lossy transmission line models. The *RLGC* matrices are parameterized by wire width and space but not by wire length. The matrices depend only on the process and the metal layer for given parameters. The S-parameters of wire length of l can be derived from *RLGC* matrices using the telegrapher's equation. Because of the skin effect, the R matrix is the linear addition of the static resistance matrix R_o and the skin effect matrix R_{sk} as shown in Equation (2.1). However, the skin effect is minor in typically-sized on-chip wires since the wire width and height are smaller than twice the skin depth.

$$R(f) = R_o + \sqrt{f}(1 + j)R_{sk} \quad (2.1)$$

By assuming that the crosstalk from the nearest neighbor is the most dominant, the

model reduces the extracted m-by-m *RLGC* matrices of an m-port bus to 2-by-2 *RLGC* matrices of two neighbor ports by selecting the corresponding 2-by-2 block, which has the diagonal terms (*RLGC* constants for through transfer function, written as r_o , l_o , g_o , and c_o) and the first off-diagonal terms (the crosstalk terms from the first neighbor, written as r_c , l_c , g_c , and c_c). By ignoring the skin effect terms, the 2x2 *RLGC* matrices are symmetric and can be expressed as follows.

$$R = \begin{bmatrix} r_o & r_c \\ r_c & r_o \end{bmatrix} \quad (2.2)$$

$$L = \begin{bmatrix} l_o & l_c \\ l_c & l_o \end{bmatrix} \quad (2.3)$$

$$G = \begin{bmatrix} g_o & g_c \\ g_c & g_o \end{bmatrix} \quad (2.4)$$

$$C = \begin{bmatrix} c_o & c_c \\ c_c & c_o \end{bmatrix} \quad (2.5)$$

For typical dense on-chip wires in the RC-regime, the L and G matrices can be ignored and the cross-resistance term r_c can also be ignored.

2.2.3 Channel's Transfer Function

Combining the driver's Thevenin equivalent model, the wire's *RLGC* transmission line model, and the receiver's input impedance model in Figure 2-2, Figure 2-4 shows the linear schematic model to derive the closed form formula for the channel frequency response of the interconnect with length l .

In Figure 2-4, C_L represents the receiver input capacitance, while R_s , C_s , V_{o1} , and V_{o2} represent the Thevenin equivalent model for two driver circuits to derive the through and crosstalk transfer functions. Typically, the driver's impedance R_S is an important parameter impacting the power consumption and transfer function while the driver's parasitic capacitance C_s can be neglected since the wire's capacitance dominates C_s . $V_1(z, \omega)$, $V_2(z, \omega)$, $I_1(z, \omega)$, and $I_2(z, \omega)$ are the traveling wave voltages and currents of interconnect 1 and interconnect 2 along the wire at distance z from the driver. For compactness, the

voltage and current variables are combined into vector forms as shown in Equations (2.6, 2.7, 2.8).

$$V(z, \omega) = \begin{bmatrix} V_1(z, \omega) \\ V_2(z, \omega) \end{bmatrix} \quad (2.6)$$

$$I(z, \omega) = \begin{bmatrix} I_1(z, \omega) \\ I_2(z, \omega) \end{bmatrix} \quad (2.7)$$

$$V_o(\omega) = \begin{bmatrix} V_{o1}(\omega) \\ V_{o2}(\omega) \end{bmatrix} \quad (2.8)$$

To arrive at the transfer function, a set of 2x2 telegrapher's equations (Equation (2.9, 2.10, 2.11)) are solved.

$$-\frac{\partial}{\partial z} \begin{bmatrix} V(z, \omega) \\ I(z, \omega) \end{bmatrix} = \begin{bmatrix} 0 & R + j\omega L \\ G + j\omega C & 0 \end{bmatrix} \begin{bmatrix} V(z, \omega) \\ I(z, \omega) \end{bmatrix} \quad (2.9)$$

$$V_o(\omega) = V(0, \omega) + R_s (I(0, \omega) + j\omega C_s V(0, \omega)) \quad (2.10)$$

$$I(l, \omega) = j\omega C_L V(l, \omega) \quad (2.11)$$

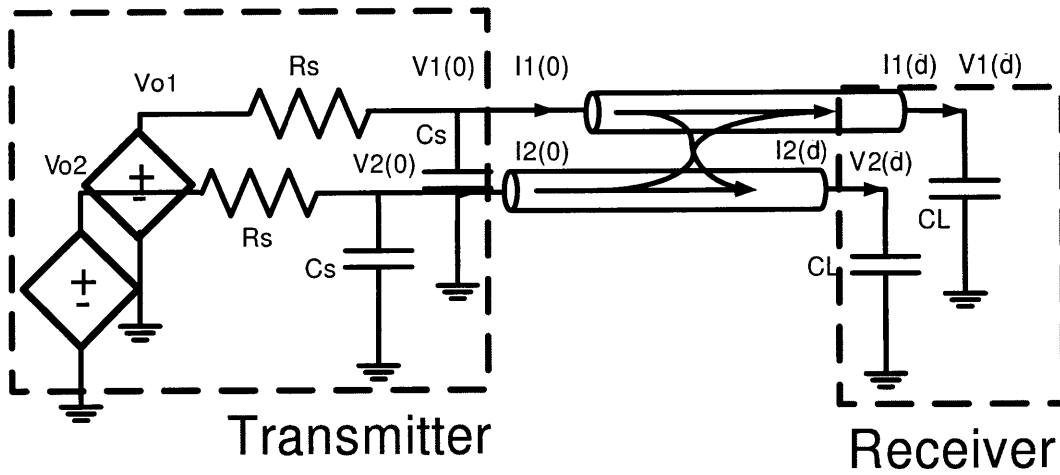


Figure 2-4: Schematics used to derive the channel's transfer function.

Equations (2.10, 2.11) are the boundary equations defined by the transmitter and receiver. Note that by replacing R_s , C_s , and C_L in Equation (2.10, 2.11) with the desired impedances, equations for other terminal impedances can be easily derived.

The solution of the telegrapher's equation is presented in Equations (2.12-2.17)

$$T(\omega) \approx T_{com}(\omega) + T_{diff}(\omega) \quad (2.12)$$

$$T_c(\omega) \approx T_{com}(\omega) - T_{diff}(\omega) \quad (2.13)$$

$$T_{com}(\omega) = \frac{e^{-l\sqrt{(z_o+z_c)(y_o+y_c)}}}{\left(j\omega C_L \sqrt{\frac{z_o+z_c}{y_o+y_c}} + 1\right) \left(1 + R_s \left(\sqrt{\frac{y_o+y_c}{z_o+z_c}} + j\omega C_s\right)\right)} \quad (2.14)$$

$$T_{diff}(\omega) = \frac{e^{-l\sqrt{(z_o-z_c)(y_o-y_c)}}}{\left(j\omega C_L \sqrt{\frac{z_o-z_c}{y_o-y_c}} + 1\right) \left(1 + R_s \left(\sqrt{\frac{y_o-y_c}{z_o-z_c}} + j\omega C_s\right)\right)} \quad (2.15)$$

$$Z = \begin{bmatrix} z_o & z_c \\ z_c & z_o \end{bmatrix} = R + j\omega L \quad (2.16)$$

$$Y = \begin{bmatrix} y_o & y_c \\ y_c & y_o \end{bmatrix} = G + j\omega C \quad (2.17)$$

where $T(\omega)$ and $T_c(\omega)$ are the through and crosstalk transfer functions of the channel. Figure 2-5 shows that the equation-based transfer functions and the SPICE simulations with a W-element transmission line wire model match very well.

Equations (2.12-2.17) are very accurate, but their forms do not provide intuition for the designer. Since the through transfer function is the most interesting one, by ignoring insignificant L and G matrices of $RLGC$ matrices and the coupling terms r_c and c_c of R and C , we simplify it into Equation (2.18).

$$T(\omega) = \frac{2e^{-l\sqrt{j\omega r_o c_o}}}{\left(j\omega C_L \sqrt{\frac{r_o}{j\omega c_o}} + 1\right) \left(1 + R_s \left(\sqrt{\frac{j\omega c_o}{r_o}} + j\omega C_s\right)\right)} \quad (2.18)$$

Equation (2.18) tells us that the overall transfer function has exponential dependencies on wire length and operating frequency. This exponential term shapes the pulse response

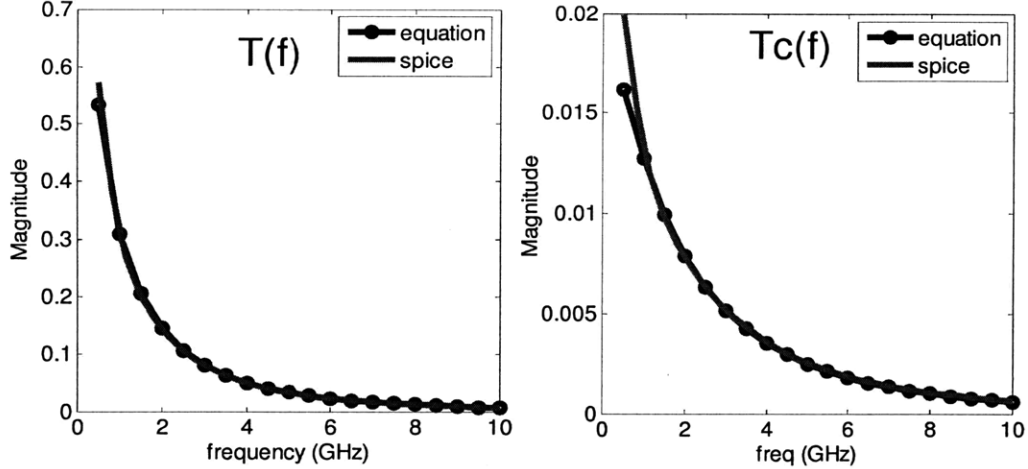


Figure 2-5: Comparison of the transfer functions from the closed form solution and the SPICE simulation [23].

of the channel in such a way that the channel can be equalized with a small number of FFE taps.

2.2.4 Impact of Termination Impedance

Unlike in off-chip transmission lines, the RC-dominant channel characteristics and the low power constraint of on-chip interconnects require different circuit designs and signaling strategies than the ones used for typical off-chip RLC transmission lines.

In RC-dominant channels, 50-Ohm impedance matching is neither necessary nor efficient for two reasons: 1) The characteristic impedance of the wire is not 50 Ohm but can actually be co-designed with circuits to maximize relevant system-level metrics [23,24]; 2) The large channel loss suppresses the reflected wave by impedance mismatch [18, 23–25, 29].

Figure 2-6 shows the small-signal circuit diagrams of interconnects in voltage and current driving modes with source impedance R_s and receiver’s termination impedance R_L . The wire is represented with wire length l , resistance and capacitance per unit length: R_o and C_o . Unlike an ideal transmission line, the wire’s characteristic impedance Z_c is a frequency dependent complex number, and results in the difference between voltage mode and current mode. By assuming RC-dominant operation ($R_o > j\omega L_o$, $j\omega C_o > G_o$), $Z_c(\omega)$ can be approximated as shown in Equation (2.19).

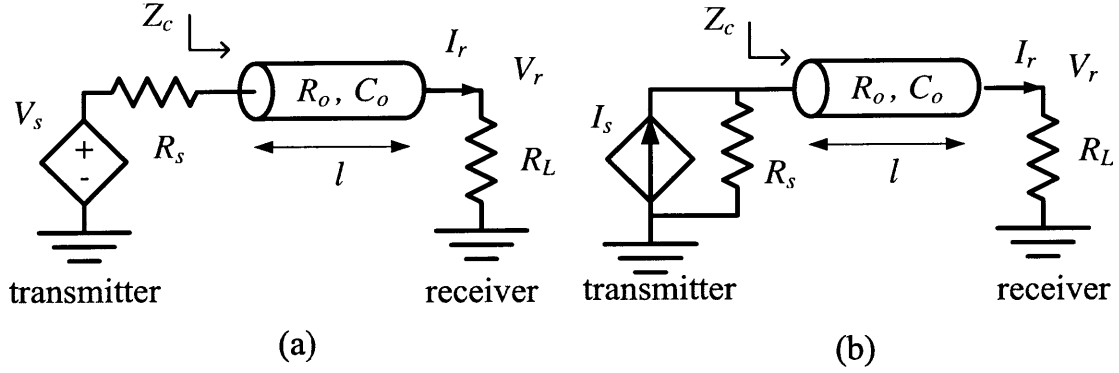


Figure 2-6: Small signal circuit diagram of interconnect in voltage and current drive/receive.

$$Z_c(\omega) = \sqrt{\frac{R_o + j\omega L_o}{G_o + j\omega C_o}} = \sqrt{\frac{R_o}{j\omega C_o}} \quad (2.19)$$

Figures 2-7 (a) and (b) present SPICE simulations of the channel's characteristic admittance which is defined as $Y_c(\omega) = 1/Z_c(\omega)$. $Y_c(\omega)$ can be approximated as shown in Equation (2.20) from Equation (2.19). The simulation setup is for a 10-mm differential signaling wire with $0.4\mu\text{m}$ width and $0.6\mu\text{m}$ spacing in 90-nm technology. The wires run in M8 layer over M7 and under M9 ground planes.

$$Y_c(\omega) = \sqrt{\frac{\omega C_o}{R_o}} e^{j\frac{\pi}{4}} \quad (2.20)$$

The square-root dependency in Figure 2.24 (a) and approximate 45 degree phase in Figure 2.24 (b) verify the Equations (2.19) and (2.20). In an RC-dominant channel, the impedance observed by the driver is approximately $Z_c(\omega)$, and does not depend on R_L due to large channel loss.

$$T_{vv}(\omega) = \frac{V_r(\omega)}{V_s(\omega)} = \frac{2e^{-l\sqrt{j\omega R_o C_o}}}{\left(\frac{Z_c(\omega)}{R_L} + 1\right) \left(1 + \frac{R_s}{Z_c(\omega)}\right)} \quad (2.21)$$

$$T_{vi}(\omega) = \frac{I_r(\omega)}{V_s(\omega)} = \frac{2e^{-l\sqrt{j\omega R_o C_o}}}{(Z_c(\omega) + R_L) \left(1 + \frac{R_s}{Z_c(\omega)}\right)} \quad (2.22)$$

$$T_{iv}(\omega) = \frac{V_r(\omega)}{I_s(\omega)} = \frac{2e^{-l\sqrt{j\omega R_o C_o}}}{\left(\frac{Z_c(\omega)}{R_L} + 1\right) \left(\frac{1}{R_s} + \frac{1}{Z_c(\omega)}\right)} \quad (2.23)$$

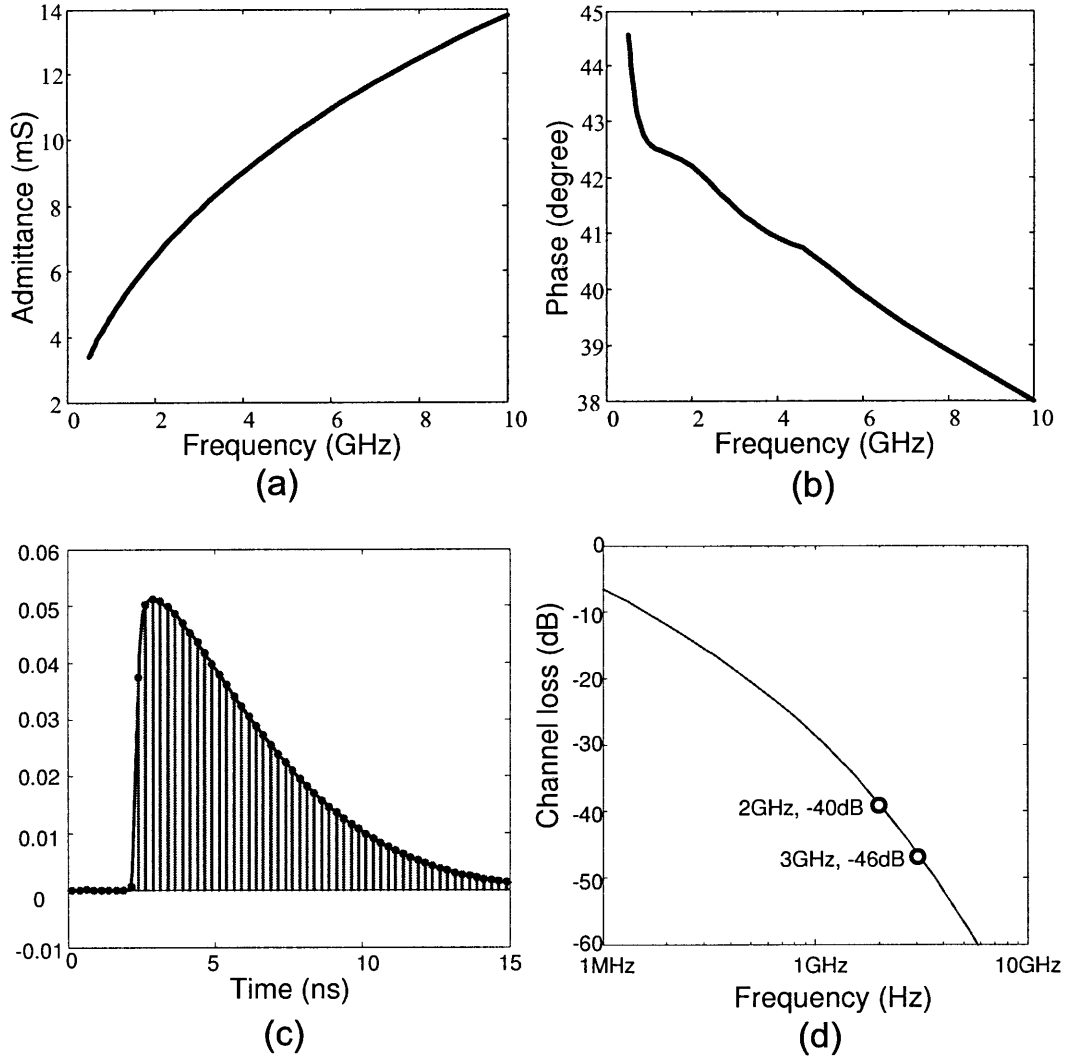


Figure 2-7: RC-dominant channel simulations: (a) magnitude of characteristic admittance; (b) phase of characteristic admittance; (c) normalized response to a 250ps square pulse and sequence sampled at 4GS/s; (d) channel's transfer function in current driving and receiving mode.

$$T_{ii}(\omega) = \frac{I_r(\omega)}{I_s(\omega)} = \frac{2e^{-l\sqrt{j\omega R_o C_o}}}{(Z_c(\omega) + R_L) \left(\frac{1}{R_s} + \frac{1}{Z_c(\omega)} \right)} \quad (2.24)$$

Equations (2.21, 2.22, 2.23, 2.24) describe the approximate the through transfer functions of four combinations of voltage/current driven and voltage/current receiving interconnects. The formulas are derived by solving telegrapher's equation and simplified by ignoring the coupling terms by side-wall capacitance between neighboring wires [23,24] as described

in Subsection 2.2.3. These formulas ignore the crosstalk just to intuitively describe the through transfer function for designers. For CAD purposes, the original forms in Equation (2.12) and (2.13) are preferred for accuracy. Although simplification results in minor quantitative error, the equations capture the qualitative behavior of an on-chip wire for designers. Note that all transfer functions would be identical with proper voltage-current transformation if $Z_c(\omega)$, R_s , and R_L were all equal (i.e. matched) as in a lossless transmission line. However, for RC-dominant on-chip wires, the selections of voltage/current mode and the termination impedances do affect the transfer function unlike off-chip equalized links.

However, regardless of mode selection, all transfer functions have strong exponential dependency on the channel length and the square-root of frequency resulting in a time-response close to an exponential form, which is a pre-requisite for small tap count FFE implementation.

Figure 2-7 (c) presents a simulated channel response to a 250 ps wide square pulse assuming 4 Gb/s binary pulse-amplitude modulation in current driving and current sensing mode. The wire is the same wire simulated in Figures 2-7 (a) and (b) and used for the test chip in Chapter 3. The response is normalized and sampled at 4 GSamples/s. The pulse width is about 50 samples, and the response peak height is only 5% of the magnitude of the transmitted square pulse. Figure 2-7 (d) shows a simulated current-drive-current-receive transfer function of the wire. The channel losses are 40 dB and 46 dB at 2 GHz and 3 GHz, respectively, which are difficult to equalize in general due to noise, speed, and mismatch-limited receiver precision (e.g. typical equalizable channel losses in off-chip links are up to 30 dB). As we mentioned previously, in spite of the large loss, the channel can be equalized with a small number of FFE-taps because the sampled sequence fits well in an exponential form [23,24] as illustrated in Equations (2.21, 2.22, 2.23, 2.24).

Since the overall link performance and power consumption strongly depend on the channel transfer functions and impedances, the equations in this section provide the key guidelines in RC-dominant link design.

Transmitter Impedance

In traditional off-chip interconnect applications, the difference between transfer functions of voltage and current driving interconnects is small when impedances are matched. However,

in an on-chip application with possibly mismatched impedances, the transfer functions of the two driving modes can be significantly different. From Equations (2.21, 2.22, 2.23, 2.24), unique factors of the transfer functions of voltage- and current- driving interconnects are expressed in Equations (2.25) and (2.26).

$$T_{vi}(\omega), T_{vv}(\omega) \propto \frac{1}{1 + \frac{R_s}{Z_c(\omega)}} \quad (2.25)$$

$$T_{iv}(\omega), T_{ii}(\omega) \propto \frac{1}{\frac{1}{R_s} + \frac{1}{Z_c(\omega)}} \quad (2.26)$$

These two expressions are in an identical form except for a multiplicative factor R_s since voltage driver and current driver can be transformed to each other by Norton- and Thevenin-equivalent forms. However, the different R_s values in practical current and voltage drivers result in different transfer functions since R_s is typically small in voltage mode and large in current mode. Equations (2.27) and (2.28) show the extreme cases when $R_s = 0$ in voltage mode and $R_s = \infty$ in current mode.

$$T_{vv}(\omega), T_{vi}(\omega) \propto 1 \quad (2.27)$$

$$T_{iv}(\omega), T_{ii}(\omega) \propto Z_c(\omega) \quad (2.28)$$

As shown in Equation 2.19, $Z_c(\omega)$ is a low pass filter-type load, and thus current mode driving has poorer spectrum than voltage mode driving by a factor of $\frac{1}{\sqrt{j\omega}}$ which is characteristic of low-pass filters. This can be understood simply as the loading effect of the wire on the driver. If a current source $I_s(\omega)$ drives the wire then the node voltage of the transmitter side wire becomes $V_{tx}(\omega) = Z_c(\omega)I_s(\omega)$. This is identical to driving the wire with voltage source $V_{tx}(\omega)$. Therefore, if an ideal current source and voltage source drive the channel with same spectrum shape, then the current driver experiences additional attenuation of $\frac{1}{\sqrt{j\omega}}$. Therefore, in comparison of these two different mode drivers, the difference of the transfer functions must be considered. The later Section 2.3 discusses this topic in detail.

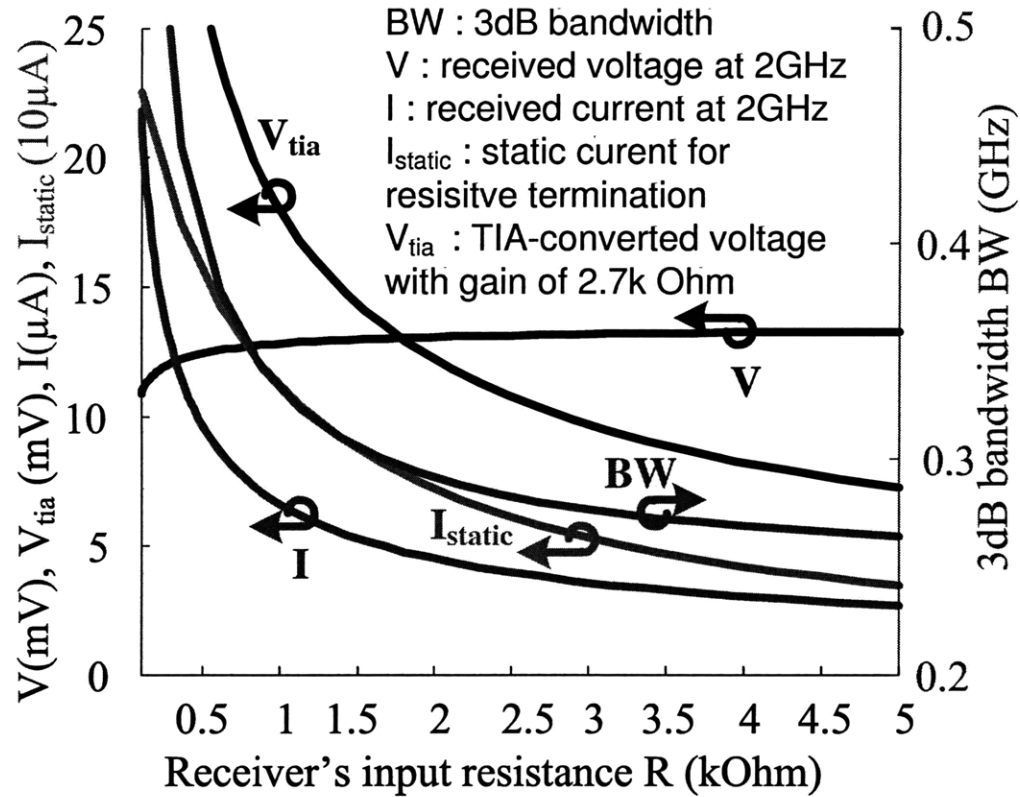


Figure 2-8: Various metrics versus receiver's termination impedance. Square markers represent resistive termination for the same bandwidth of TIA. Circle markers represent TIA termination.

Receiver Impedance

The receiver's input impedance significantly affects the channel's characteristics of the RC-dominant wires [30,31]. Figure 2-8 shows various metrics versus the termination impedance R_L in Figure 2-6 while keeping the common mode voltage of the transmitter as half the supply to guarantee enough voltage swing at the transmitter. The circle markers present the channel characteristics of the TIA terminated receiver of the test chip in Chapter 3 while the square markers present the channel characteristics of the resistive termination for the same bandwidth. The wire dimensions are as expressed for Figure 2-7 in Subsection 2.2.4.

As discussed earlier, the impedance affects the overall transfer function in an RC dominated channel. From Equations (2.21, 2.22, 2.23, 2.24), the difference between voltage and current receiving modes can be expressed as in Equation (2.29) and (2.30).

$$T_{vv}(\omega), T_{iv}(\omega) \propto \frac{R_L}{Z_c(\omega) + R_L} \quad (2.29)$$

$$T_{vi}(\omega), T_{ii}(\omega) \propto \frac{1}{Z_c(\omega) + R_L} \quad (2.30)$$

Both voltage mode and current mode have the same bandwidth for a given resistance since the denominator is the same while the amplitude shows a different trend due to the numerator term R_L .

In voltage mode, the receiver is usually terminated with a large resistor to achieve large amplitude and small static current. As R_L increases, the received signal voltage amplitude V at 2GHz (AC) increases as expected in Equation (2.29) but saturates as R_L becomes dominant. At the same time, the DC static current keeps the driver's common mode voltage at half the supply, decreasing the static power. However, the 3dB bandwidth of the channel also decreases, requiring increased equalization effort as R_L increases.

The trade-off between bandwidth and the signal amplitude is different in current mode. By terminating the receiver with small resistance, the received signal current I at 2GHz (AC) as well as the 3dB bandwidth increase as shown in Figure 2-8 and as expected from Equation (2.30). However, the cost of smaller input impedance is a larger DC static current. Therefore, a designer can buy bandwidth and amplitude by trading off dynamic for static power.

This thesis work proposes using a trans-impedance amplifier (TIA) at the receiver front-end to eliminate this fundamental trade-off between voltage mode and current mode signaling by separating the relation between the small signal input impedance and the TIA's gain resistance which determines the static bias current. A TIA in Figure 2-9 provides a small-signal input resistance (about 860Ohm) to the channel but requires 2x smaller static current ($160\mu\bar{A}$) than the one ($310\mu\bar{A}$) required by a pure 860Ohm termination for the same bandwidth (54MHz). After current-to-voltage conversion by the TIA, the converted voltage amplitude V_{tia} is about 3x higher than the received voltage with pure 860Ohm termination. Therefore, the TIA can achieve 3x higher signal amplitude with 2x smaller static power for the same bandwidth compared to the pure resistive termination. With a larger amplitude, the transmitter's driving amplitude can be smaller for the same eye opening at the receiver saving dynamic power. This benefit scales larger as the TIA's input impedance decreases and gain resistance becomes larger.

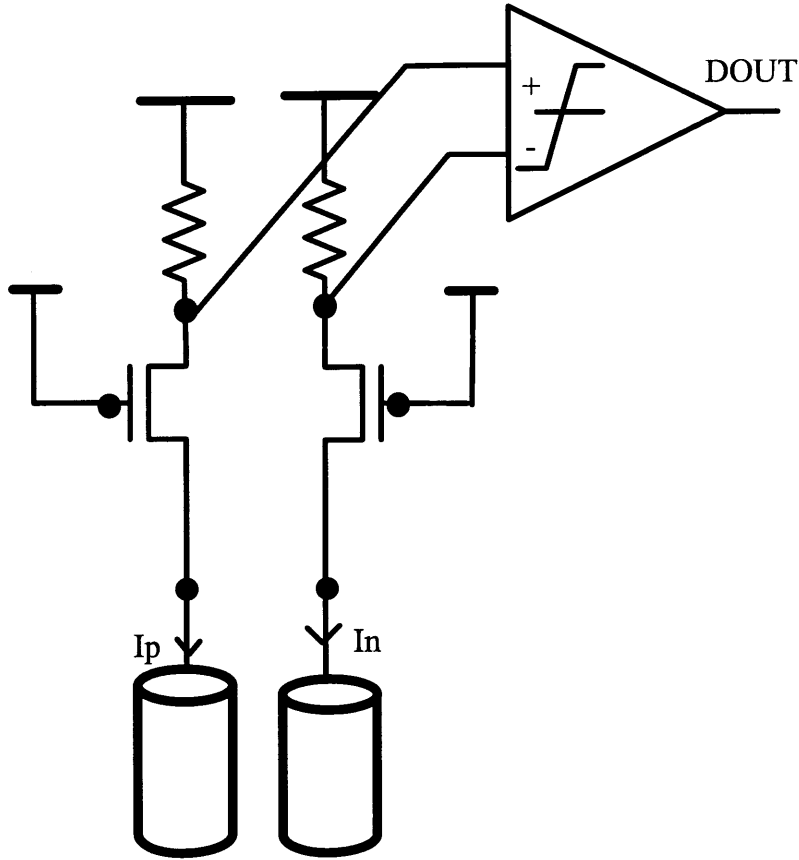


Figure 2-9: Trans-impedance amplifier receiver.

2.3 Drivers

In RC-dominated on-chip links, the transmitter typically consumes most of the link power producing an equalized signal and driving a large wire capacitance. To improve energy-efficiency, this thesis work introduces a CI FFE transmitter that in principle consumes 2x less power than the conventional analog-summing FFE. The CI FFE also significantly relaxes the coefficient accuracy requirement, allowing operation at high channel losses with relatively inexpensive low-resolution hardware. In this section, we review the typical driver types and compare them to the proposed CI FFE.

2.3.1 Conventional Drivers: Voltage Dividing Driver, Current Mode Logic, and Current Switching Driver

Voltage dividing (VD) drivers [32–35] (also known as a Low Common Mode (LCM) [33] or Source Series Termination (SST) [35] driver depending on the implementation) are widely used in low-power applications because they are more power efficient than current mode logic (CML) drivers [33].

A VD driver uses a programmable resistor network to generate FFE output voltages while providing a constant output impedance. Figure 2-10 shows the operation of a two-tap VD driver and its Thevenin equivalent circuit with an FFE coefficient vector $[(0.5 + \alpha_v) - (0.5 - \alpha_v)]$, for ‘11’ and ‘10’ data pattern D_0D_{-1} . Each driver segment has matched pull-up and pull-down resistance values $\frac{R}{0.5+\alpha_v}$ and $\frac{R}{0.5-\alpha_v}$. Since the pull-up and pull-down pairs are driven by the complementary signals, the impedance attached at each output terminal is always $R = \frac{R}{0.5+\alpha_v} // \frac{R}{0.5-\alpha_v}$ while the voltage is programmed. This can be easily mapped to a Thevenin equivalent voltage source model with a constant Thevenin impedance and a controlled voltage source as shown in Figure 2-10. For example, in Figure 2-10 (a), the Thevenin impedance is R , and the Thevenin voltages of the positive and the negative terminals are $(0.5 + \alpha_v)V_{dd}$ and $(0.5 - \alpha_v)V_{dd}$. In Figure 2-10 (b), the Thevenin impedance is R , and the Thevenin voltages of the two differential terminals are V_{dd} and 0. As a result, this driver can be modeled as the controlled voltage source whose voltage value is an FFE summation output modeled in Figure 1-3 with Thevenin impedance R .

A CML driver uses current switches to generate differential FFE pull-down currents which determine the Thevenin-equivalent voltages through resistors attached to a supply. Figure 2-11 shows the operation of a two-tap CML driver and its Thevenin equivalent circuit with an FFE coefficient vector $[(0.5 + \alpha_v) - (0.5 - \alpha_v)]$ for ‘11’ and ‘10’ data pattern D_0D_{-1} . The two tail current values $(0.5 + \alpha_v)V_{dd}/R$ and $(0.5 - \alpha_v)V_{dd}/R$ are mixed by data driven current switches generating the Norton-equivalent currents, and this can be easily mapped to a Thevenin equivalent voltage source model with a constant Thevenin impedance and a controlled voltage source as shown in Figure 2-11. Note that the tail current values $(0.5 + \alpha_v)V_{dd}/R$ and $(0.5 - \alpha_v)V_{dd}/R$ chosen in this figure provide the same Thevenin equivalent circuit in Figure 2-10. Since the Thevenin models are the same in Figure 2-10 and 2-11, these two drivers are identical in terms of signaling and equalization

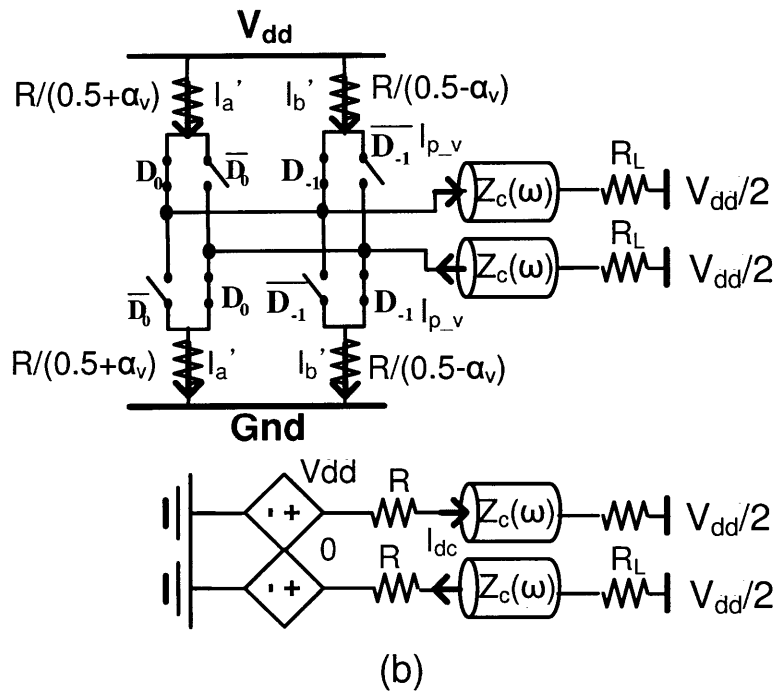
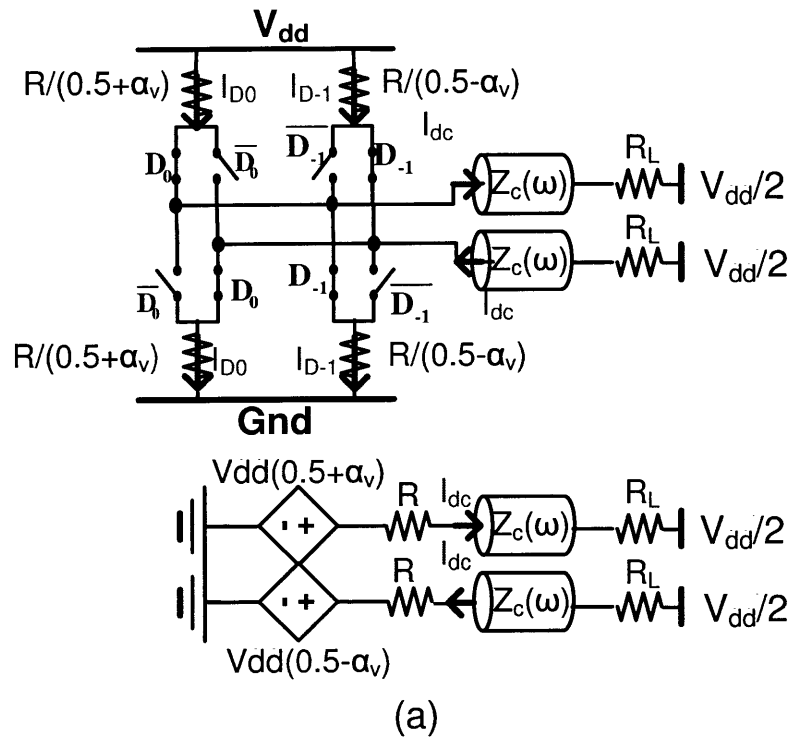


Figure 2-10: A 2-tap voltage dividing (VD) driver and its Thevenin equivalent circuit (a) VD when $D_0D_{-1} = '11'$ (b) VD when $D_0D_{-1} = '10.'$

ability.

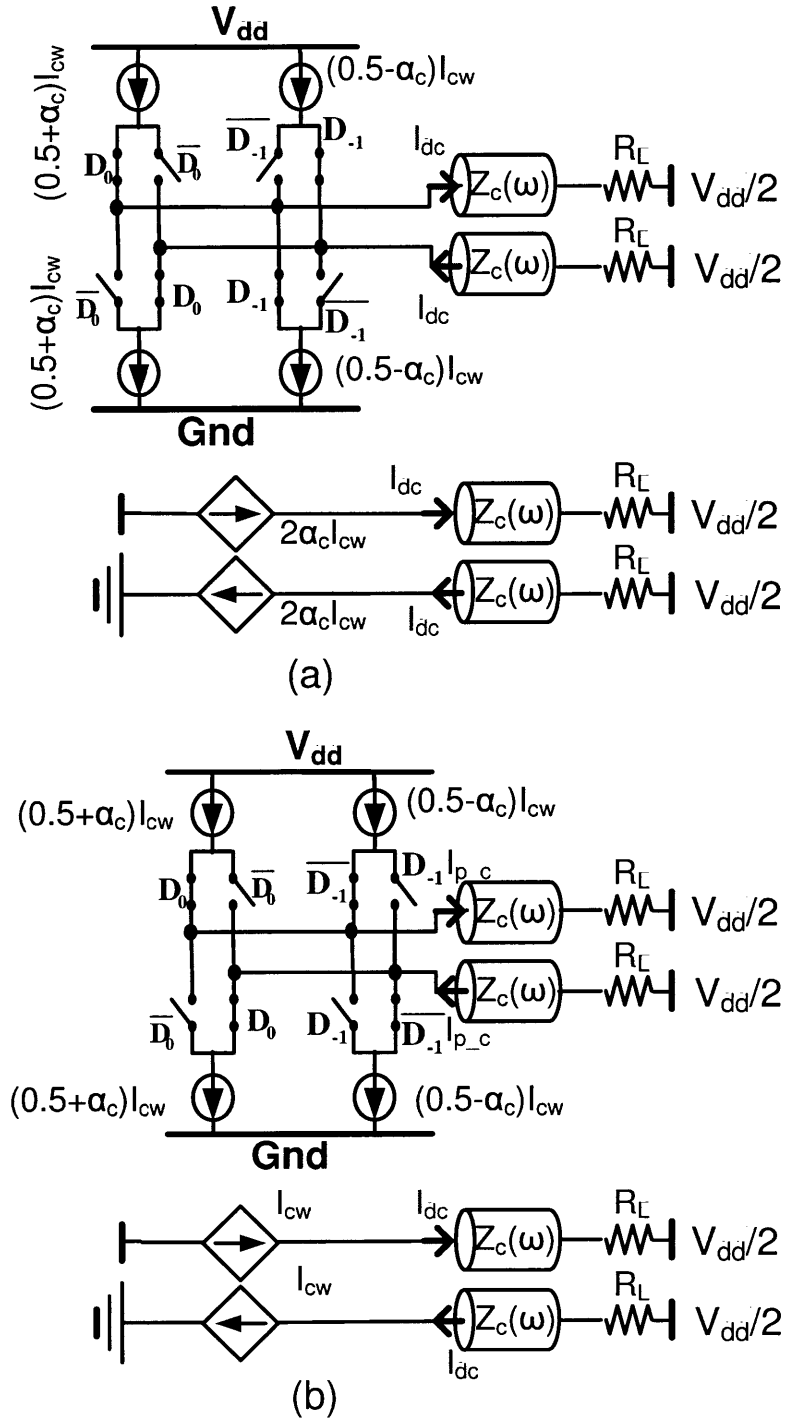


Figure 2-12: A current switch (CS) driver and its Norton equivalent circuit (a) CS when $D_0D_{-1} = '11'$ (b) CS when $D_0D_{-1} = '10'$.

Figure 2-12 shows a CS driver for the same function as in Figure 2-10 with an equaliza-

tion coefficient vector $[(0.5 + \alpha_c) - (0.5 - \alpha_c)]$. A CS driver sums currents to conduct the summation function of the FFE in Figure 1-3 while a VD driver does it by voltage division. Note that the variable for the equalization coefficients α_c for the CS driver is smaller than the variable α_v for the VD driver because of the termination impedance difference. The CS driver is modeled as a current mode driver since its output impedance is large while the VD driver is modeled as a voltage mode driver since its output impedance is small. As discussed in Subsection 2.2.4, the current mode transfer function is more lossy than the voltage mode transfer function. To compensate this, the FFE coefficients of the CS driver must form a stronger high-pass filter than the VD driver FFE. As a result, in the 2-tap FFE, α_c is smaller than α_v .

2.3.2 Charge Injection Driver

This subsection introduces the basic concept of the Charge Injection (CI) FFE driver. As will be explained in Subsection 2.3.3 and 2.3.4, the CI FFE driver improves the power efficiency and eye sensitivity compared to the conventional VD, CML, and CS FFE drivers.

Figure 2-13 (a) and (b) compares pull-down parts of the CS FFE and the proposed CI FFE when pattern $D_0D_{-1}D_{-2}='011'$ is being transmitted. The CS driver computes the FFE sum (I_0 in Figure 2-13) in the analog domain by addition or subtraction of currents w_0 , $|w_1|$, and w_2 , while a CI FFE just drives a pre-computed I_0 current directly into the channel. The CS FFE driver draws more current than a CI FFE driver from the supply due to the current wasted in subtraction.

$D_0D_{-1}D_{-2}$	CS FFE sum	CI FFE output	Tx voltage transition
1 1 1	$w_0 + w_1 + w_2$	I_0	$V_{MH} \rightarrow V_{MH}$
1 1 0	$w_0 + w_1 - w_2$	$-I_1$	$V_{High} \rightarrow V_{MH}$
1 0 1	$w_0 - w_1 + w_2$	$I_0 + I_1 + I_2$	$V_{Low} \rightarrow V_{High}$
1 0 0	$w_0 - w_1 - w_2$	I_2	$V_{ML} \rightarrow V_{High}$
0 1 1	$-w_0 + w_1 + w_2$	$-I_2$	$V_{MH} \rightarrow V_{Low}$
0 1 0	$-w_0 + w_1 - w_2$	$-(I_0 + I_1 + I_2)$	$V_{High} \rightarrow V_{Low}$
0 0 1	$-w_0 - w_1 + w_2$	I_1	$V_{Low} \rightarrow V_{ML}$
0 0 0	$-w_0 - w_1 - w_2$	$-I_0$	$V_{ML} \rightarrow V_{ML}$

Table 2.1: Construction of CI FFE by mapping from CS FFE.

Table 2.1 presents the mapping from the CS FFE sums to the corresponding CI FFE currents, and Table 2.2 shows the current values for the CI FFE coefficients and the corresponding CS FFE coefficients. These coefficients are based on the simulation for the test

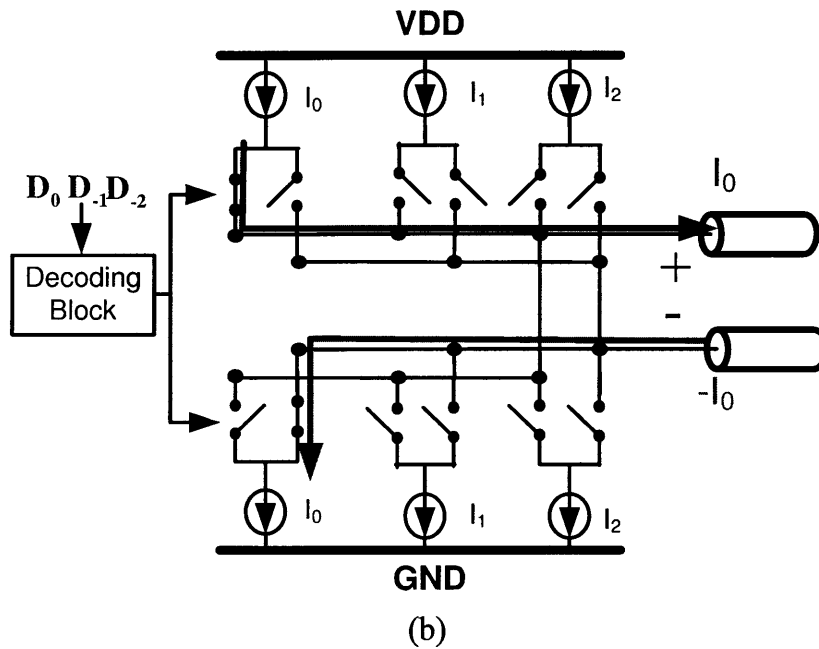
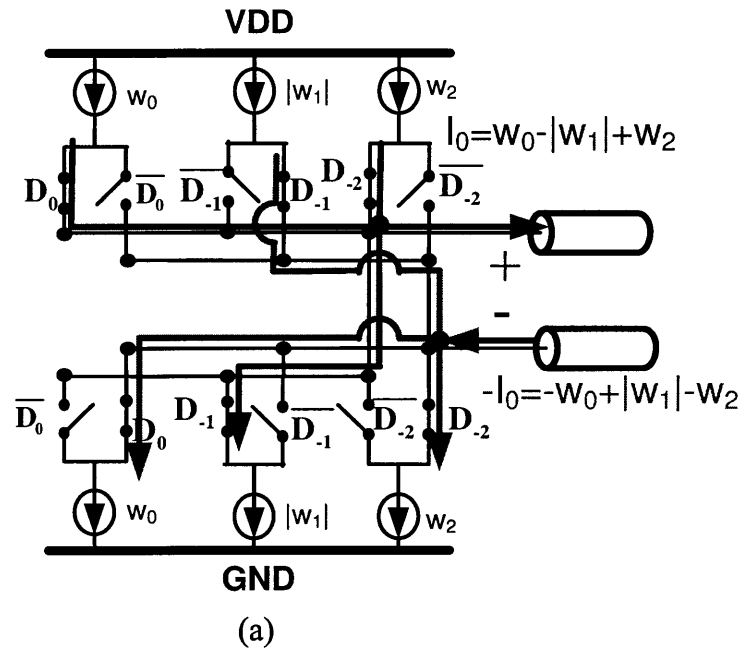


Figure 2-13: Comparison between (a) a conventional Current Switching FFE and (b) a Charge Injection FFE when data pattern is $D_0 D_{-1} D_{-2} = '111.'$

	current values in μA
I_0	14
I_1	220
I_2	558
$I_0 + I_1 + I_2$	792
w_0	286
w_1	-389
w_2	117

Table 2.2: CS FFE and CI FFE coefficient values.

chip in Chapter 3. For a given FFE coefficient $[w_0 w_1 w_2]$ and data pattern $D_0 D_{-1} D_{-2}$, the FFE sum I_T can be simply expressed in Equation (2.31) where d_i is defined as 1 if D_i is '1,' or -1 otherwise.

$$I_T = \sum_{i=1}^2 w_i d_{-i} = w_0 d_0 + w_1 d_{-1} + w_2 d_{-2} \quad (2.31)$$

Table 2.1 lists eight (2^3) distinct FFE sum values. Since three variables (w_0 , w_1 , and w_2) can span the FFE sum list, the other three positive variables I_0 , I_1 , and I_2 as defined in the table must be able to span the same FFE sum list by addition only, avoiding the power lost during current subtraction. Note that the list in the table is symmetric with opposite polarities since it is constructed from binary combinations of d_i with values ± 1 . With this mapping, the construction of CI FFE requires only 3 distinct currents (I_0 , I_1 , and I_2 are all positive since w_0 and w_2 are positive and w_1 is negative in a typical RC-dominant channel). In hardware implementation, I_0 , I_1 , and I_2 current sources can be connected to the channel independently with the proper polarity, or together for $\pm(I_0 + I_1 + I_2)$.

Figure 2-14 shows the simulated waveforms of the transmit FFE current I_T and voltage V_T when an isolated '1' pattern (i.e. single pulse) is being transmitted. The simulation setup models the test chip described in Chapter 3. Table 2.1 lists the corresponding current and voltage transition. While consecutive '0's are transmitted, the transmitter draws I_0 current from the channel ($-I_0$), and the Tx voltage V_T stays in the middle-low level voltage V_{ML} . When an isolated '1' is transmitted, the transmitter injects I_2 into the channel raising the voltage V_T from V_{ML} to V_{High} . Similarly, the CI FFE driver conducts $-I_{max}$, I_1 , and $-I_0$ currents for the '000' bit sequence following the isolated '1,' and the voltage changes from V_{High} , to V_{Low} , and then to V_{ML} . Note that I_{max} value is not exactly $I_0 + I_1 + I_2$ because of the non-ideality of the current source circuit, which will be explained in Chapter

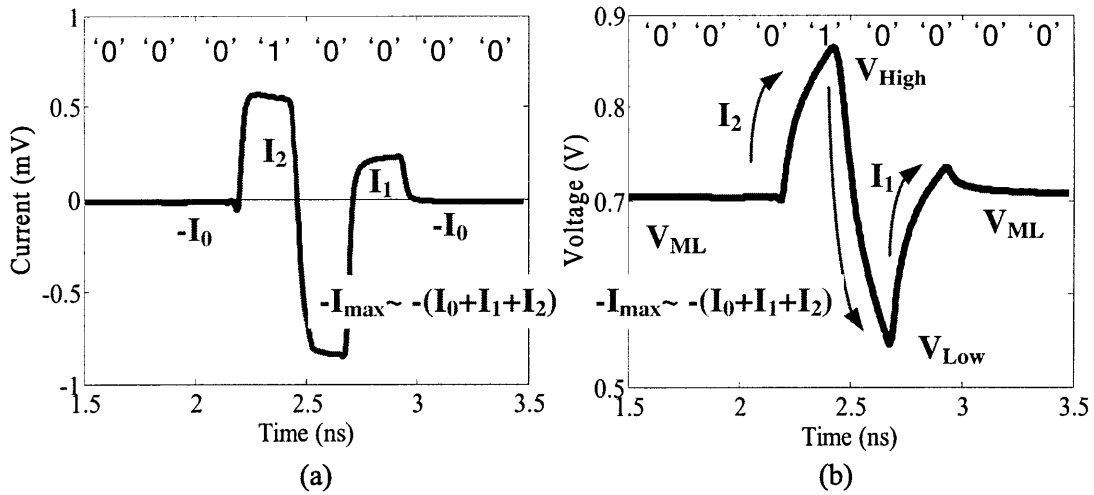


Figure 2-14: Simulated transmit current (a) and voltage (b) for isolated '1' pattern.

3.

To explain the role of different current segments (I_0 , I_1 , and I_2), Figure 2-15 presents the simulated receiver current I_R for the same isolated '1' pattern. The impact of each FFE current is represented as an arrow. During consecutive transmission of '0's, the transmitter sets I_T to $-I_0$. Since I_T stays constant at $-I_0$, this current is not attenuated by the channel, and thus, I_R stays at $-I_0$ which corresponds to bit '0' for the receiver. I_T current is set to I_2 at the data transition from '0' to '1' raising I_R from $-I_0$ to I_0 . Although I_2 amplitude is much larger than $2I_0$, the impact of the abrupt I_T change on the received current is attenuated to $2I_0$ by the high-frequency channel loss. When data transition from '1' to '0,' I_T changes to $-I_{max}$ (theoretically $-(I_0 + I_1 + I_2)$ but approximately $-(I_1 + I_2)$ since I_0 is much smaller than other currents). The role of $-I_{max}$ injection could be intuitively explained by a superposition of $-I_1$ and $-I_2$ injections. The $-I_1$ portion of $-I_{max}$ suppresses delayed overshoot (depicted as dashed curve in Figure 2-15) from the previous I_2 during the data transient from '0' to '1,' keeping the I_R at I_0 . The $-I_2$ portion of $-I_{max}$ current further pushes I_R value down to $-I_0$, just as I_2 previously raised I_R from $-I_0$ to I_0 . To finish the transition, I_T becomes I_1 correcting the delayed undershoot caused by the previous $-I_2$ portion of $-I_{max}$. To send consecutive '0's again after finishing transition, I_T settles to $-I_0$ keeping I_R at $-I_0$. This concept of the impact of each current CI FFE value on the received current will be used to explain eye sensitivity in Subsection

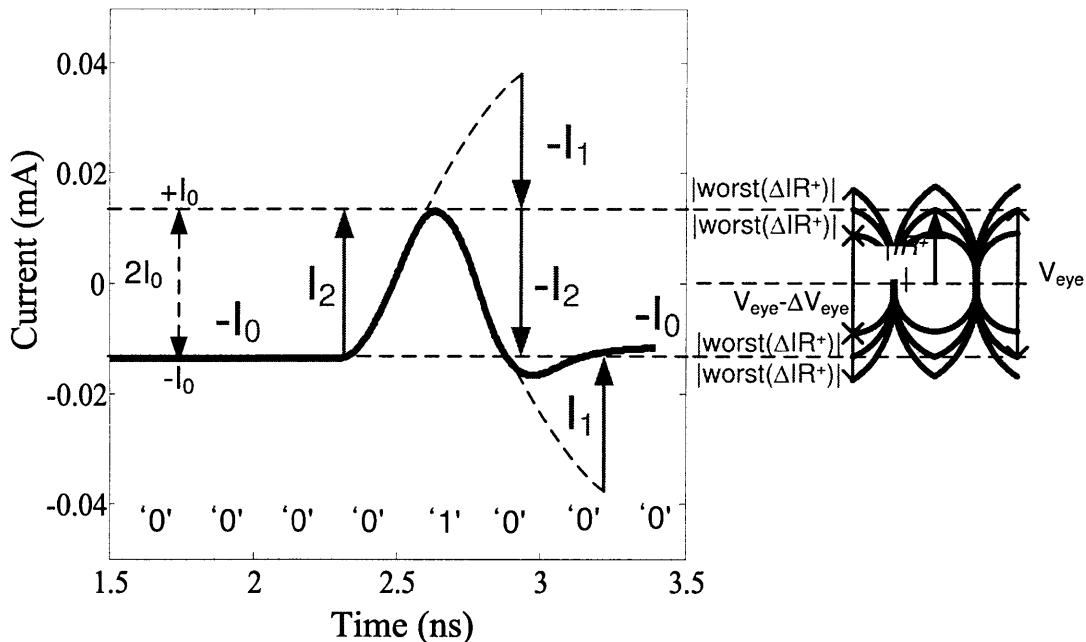


Figure 2-15: Simulated received current for isolated '1' pattern and eye perturbation.

2.3.4.

2.3.3 Power Consumption

In this subsection, we compare the power consumption of VD, CML, CS, and CI FFE drivers. The comparison is based on the mathematical analysis discussed in Section 2.2.

Due to the differential operation, the average supply current of the 2-tap VD driver in Figure 2-10 for a random data pattern is the average of the supply currents in Figure 2-10 (a) and Figure 2-10 (b). For a reasonably lossy channel, $\alpha_v \ll 0.5$ and Tx output voltages are approximately $V_{dd}/2$, making I_{dc} much smaller than I_{D_0} or $I_{D_{-1}}$. Therefore, the supply current in Figure 2-10 (a) is approximately I_{supa} in Equation (2.32).

$$I_{supa} = I_{D_0} + I_{D_{-1}} \approx \frac{0.5V_{dd}}{R} \quad (2.32)$$

We can compute the average supply current I_{supb} during the data pattern $D_0D_{-1}='10'$ or '01' from the average current I_{pv} flowing into the channel in Figure 2-10 (b). From the Thevenin equivalent circuit, for a given small α_v within a bit time T , I_{pv} can be approximated as Equation (2.33)

$$I_{pv}(\omega) \approx \frac{0.5V_{dd}}{R + Z_c(\omega)} u(\omega) \quad (2.33)$$

where $u(\omega)$ is the Fourier transform of a single square pulse with unit amplitude and duration of one bit time T . By taking the average of $I_{pv}(t)$ in time domain within a bit time and using Equation (2.33), the average supply current consumed in Figure 2-10 (b) is shown in Equation (2.34).

$$I_{supb} \approx \frac{1}{T} \int_0^T F^{-1}(I_{pv}(2\pi f)) dt = \frac{1}{T} \int_{-\infty}^{\infty} \frac{0.5V_{dd}}{R + Z_c(2\pi f)} |u(2\pi f)|^2 df \quad (2.34)$$

I_{supb} is always smaller than I_{supa} due to the characteristic impedance. For a matched lossless transmission line (i.e. $Z_c(2\pi f) = R_L = R$), I_{supb} is exactly the half of I_{supa} .

For a random data pattern, the average supply current for the VD driver is I_{vd} in Equation (2.35).

$$I_{vd} = (I_{supa} + I_{supb})/2. \quad (2.35)$$

Unlike the VD driver, which utilizes a resistive voltage divider, a CML driver subtracts or adds currents to generate pull-down currents while the pull-up currents are provided by the resistor loads. As shown in Figure 2-11, the supply current is V_{dd}/R for the CML driver which has the identical Thevenin model of the VD driver in Figure 2-10.

$$I_{cml} = \frac{V_{dd}}{R} \quad (2.36)$$

Similar to the CML driver, a CS driver subtracts or adds currents to generate the same signaling currents, but, unlike the CML driver, the pull-up currents are also generated from the current switches. Since the current drawn from the supply is always I_{cs} , the power consumption is the same in Figure 2-12 (a) and (b). For fair comparison, we have to match the channel current of the VD and CS drivers, especially, I_{pv} and I_{pc} at Nyquist frequency f_N as shown in Equation (2.38). The DC channel current I_{dc} in Figure 2-12 (a) can be easily matched to the one in Figure 2-10 (a) by adjusting α_c . The supply current of the CS driver I_{cs} is equal to I_{pc} as shown in Equation (2.38).

$$I_{cs} = I_{pc} = \left| \frac{0.5V_{dd}}{R + Z_c(2\pi f_N)} \right| \quad (2.37)$$

We can easily compare the theoretical power consumption of a CS FFE driver and a CI FFE driver by taking the average current in Table 2.1. The average supply current of a CS FFE, I_{cs} , is simply the sum ($w_0 + |w_1| + w_2$) or equivalently ($I_0 + I_1 + I_2$) according to Table 2.1 since w_0 , w_1 , and w_2 current sources in Figure 2-13 are always turned on. Therefore, I_{cs} is independent of the data pattern and is calculated as Equation (2.38).

$$I_{cs} = (w_0 + |w_1| + w_2) = (I_0 + I_1 + I_2) \quad (2.38)$$

The average supply current of a CI FFE for random data, I_{ci} is calculated by taking the average of current values in Table 2.1 as shown in Equation (2.39).

$$I_{ci} = \frac{1}{2}(I_0 + I_1 + I_2) = \frac{I_{cs}}{2} \quad (2.39)$$

According to Equations (2.38) and (2.39), for the same FFE functionality, the CI FFE burns half the power of the conventional CS FFE (assuming random data).

Figure 2-16 shows I_{vd} , I_{cml} , I_{cs} , and I_{ci} versus VD driver's output impedance R for 4 Gb/s data transmission through the channel when the signaling strength of all drivers are matched. Note that R is indication of a VD driver's strength. The channel is modeled for the wire used in Chapter 3. As expected from Equations (2.32) and (2.34), $I_{supa} \approx 2I_{supb}$, if R is close to the channel's characteristic impedance at the Nyquist frequency $|Z_c(2\pi f_N)|$ (which is about 160 Ohm in this example). In this region, I_{vd} is about 50% larger than I_{cs} and three times larger than I_{ci} according to Equation (2.39). I_{cml} is about twice as large as even I_{vd} . For a simple example of a matched lossless transmission line (i.e. $Z_c(2\pi f) = R_L = R$) case, the average supply currents are shown in Equations (2.40, 2.41, 2.42, 2.43).

$$I_{vd-matched} = \frac{3V_{dd}}{8R} \quad (2.40)$$

$$I_{cml-matched} = \frac{V_{dd}}{R} \quad (2.41)$$

$$I_{cs-matched} = \frac{V_{dd}}{4R} \quad (2.42)$$

$$I_{ci-matched} = \frac{V_{dd}}{8R} \quad (2.43)$$

As R becomes much larger than $|Z_c(2\pi f_N)|$, I_{vd} and I_{cs} converge, and VD and CS drivers burn twice the power of a CI driver while a CML driver burns twice the power of

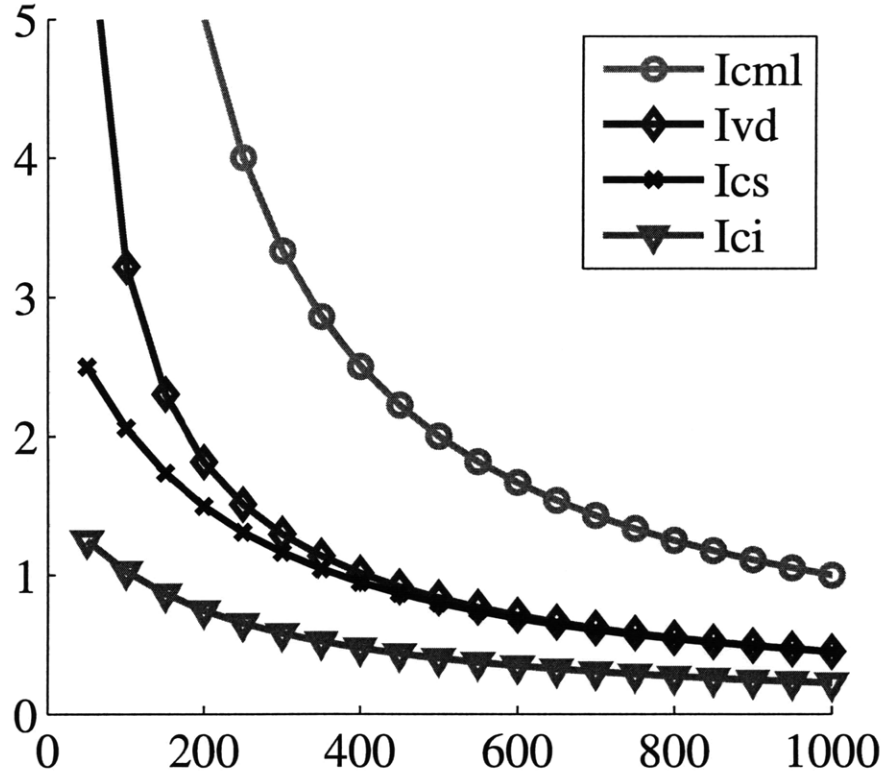


Figure 2-16: Supply currents of CML, VD, CS, and CI driver for the same signal driving ability. R is the VD driver impedance. CS and CI drivers are matched for the same signal driving ability to the VD driver at Nyquist Frequency.

the VD driver. The CI driver used in Chapter 3 has the equivalent driving current of the VD driver with $R = 625$ Ohm (which is larger than $|Z_c(2\pi f_N)|$), and thus burns half the power of the VD driver of the same driving ability and a quarter of the power of the CML driver.

At lower link utilizations, CI FFE is even more power-efficient since it only draws large current on bit transitions, while the CS FFE draws its peak current ($= w_0 + w_1 + w_2 = I_0 + I_1 + I_2$) all the time and the VD FFE wastes the most power in voltage division generating voltage near half V_{dd} . When the data pattern is all '0' or all '1,' the CI FFE only draws I_0 current which is, according to Table 2.2, less than 2% of $I_0 + I_1 + I_2$ due to the large channel attenuation. If the ratio of the idle time to the total operating time is α_{idle} , then Equations (2.44) and (2.45) show the average power consumptions of CS and CI FFE.

$$P_{cs-avg} = V_{dd}(I_0 + I_1 + I_2) \quad (2.44)$$

$$P_{ci-avg} = \alpha_{idle}V_{dd}I_0 + (1 - \alpha_{idle})\frac{V_{dd}}{2}(I_0 + I_1 + I_2) \quad (2.45)$$

In an RC-dominated channel, the ratio of I_0 to $(I_0 + I_1 + I_2)$ is proportional to the channel loss at Nyquist frequency f_N as described in Equation (2.24), which is derived from the first harmonic of the received current (a sinusoidal wave with amplitude I_0) when the transmitter current is a square wave with amplitude $(I_0 + I_1 + I_2)$ transmitting the alternating bit pattern ‘...0101010101...’

$$|T_{ii}(f_N)| \approx \frac{\pi I_0}{4(I_0 + I_1 + I_2)}. \quad (2.46)$$

The average power consumption of VD driver is slightly larger than the average power consumption of the CS driver in an RC-dominant channel. As shown in Figure 2-16, the supply current of a VD driver under full utilization is equal to the supply current of a CS driver. During idle period, however, the VD driver burns its peak current (I_{supa}), which is slightly larger than the CS driver current.

$$\begin{aligned} P_{vd-avg} &= \alpha_{idle}V_{dd}(I_{supa}) + (1 - \alpha_{idle})V_{dd}(I_{suba} + I_{supb}) \\ &\approx \alpha_{idle}V_{dd}(I_{supa}) + (1 - \alpha_{idle})P_{cs-avg} \\ &> P_{cs-avg} \end{aligned} \quad (2.47)$$

2.3.4 Eye Sensitivity

Inaccuracy of FFE coefficients often limits the performance of a link, especially for a high-loss channel, because a transmit FFE relies on the elimination of inter-symbol-interference (ISI) by canceling the LPF property of the channel response with the FFE response. For that reason, the accuracy error of FFE coefficients reduces the received eye. For the same percentage of eye reduction, the allowed percentage of the FFE coefficient error is different for different types of FFE. In this section, we mathematically show that eye opening is less sensitive to the coefficient error in CI FFE than in the traditional CS FFE, and therefore, the accuracy constraint on the CI FFE driver circuit is more relaxed. For the implementation

described in Chapter 3, the sensitivity difference between the CS and CI FFE drivers is about *ten* times. We also show that the accuracy constraint on a CI FFE driver is much less dependent on the channel loss than the one on a CS FFE, allowing inexpensive driver circuits to be used for CI FFE even for highly lossy channels.

Eye Sensitivity of CS FFE

To theoretically analyze the impact of FFE coefficient errors on the vertical eye, we assume perfect equalization and examine the eye sensitivity, which is defined as the percentage of the eye reduction divided by the percentage of each coefficient perturbation.

Let $[h_i]$ be the sampled sequence of the channel response to a square pulse in Figure 2-7. The received sampled current sequence $[I_R]$ can be expressed as a convolution of the FFE coefficient vector $[w]$ and a transmitted data sequence $[d_i]$ whose value is 1 for binary ‘1’ and 0 for binary ‘0.’

$$[I_R] = [h] * [w] * [d] \quad (2.48)$$

The n -th element of $[I_R]$ can be decomposed as a linear summation of each w_0 , w_1 , and w_2 coefficient.

$$I_{Rn} = w_0([h] * [d])_n + w_1([h] * [d])_{n-1} + w_2([h] * [d])_{n-2} \quad (2.49)$$

Under perfect equalization condition, the nominal I_{Rn} value is either I_0 or $-I_0$ as illustrated in Figure 2-15. From Equation (2.49), the perturbation of I_{Rn} is the linear sum of each FFE coefficient perturbation w_i multiplied by $([h] * [d])_{n-i}$ giving us Equation (2.50).

$$\Delta I_{Rn} = \Delta w_0([h] * [d])_n + \Delta w_1([h] * [d])_{n-1} + \Delta w_2([h] * [d])_{n-2} \quad (2.50)$$

The worst case perturbation of I_{Rn} in a CS FFE occurs when $[h] * [d]$ becomes the maximum (or minimum) value $\sum_{i=0}^{\infty} h_i$ (or $-\sum_{i=0}^{\infty} h_i$) when all $d_i = 1$ (or -1) for all i because h_i is all positive in an RC-dominant channel as shown in Figure 2-7 (b). Note that $\sum_{i=0}^{\infty} h_i$ corresponds to the DC value of the transfer function of the channel. By applying Kirchoff’s current law, the transmitter current must be equal to the receiver current at DC since there is no other current path, and therefore, $\sum_{i=0}^{\infty} h_i$ is equal to 1 giving us Equation (2.51) for the worst case I_R from Equation (2.50).

$$\Delta I_{R-worst} = \pm(\Delta w_0 + \Delta w_1 + \Delta w_2) \quad (2.51)$$

This result simply shows that the received current amplitude perturbation by the coefficient inaccuracy is the largest and direct sum of coefficient perturbation of w_0 , w_1 , and w_2 when the transmitting data pattern is all ‘1’ or ‘0,’ i.e. DC signal. This is because the transmit current is equal to the receiver current at DC, and the value is the sum of coefficient currents: w_0 , w_1 , and w_2 .

The right side of Figure 2-15 illustrates that I_R determines the received signal amplitude and thus the nominal vertical eye while I_R adds data dependent errors due to the coefficients perturbation on top of the nominal eye diagram, reducing the eye height. We can simply equate the relationships between the nominal values as well as the perturbations of the vertical eye and I_R .

$$E_{ye} = 2|I_R| = 2I_0 \quad (2.52)$$

$$\Delta E_{ye} = -2|\Delta I_{R-worst}| \quad (2.53)$$

From Equation (2.51), (2.52), and (2.53), we can derive the eye sensitivity on each FFE coefficient, which is the percentage of vertical eye change divided by the percentage of the coefficient error.

$$S_{w_i} = \frac{\left| \frac{\Delta E_{ye}}{E_{ye}} \right|}{\left| \frac{\Delta w_i}{w_i} \right|_{\Delta w_n=0, n \neq i}} = \frac{\left| \frac{2\Delta w_i}{2I_R} \right|}{\left| \frac{\Delta w_i}{w_i} \right|} = \left| \frac{w_i}{I_0} \right| \quad (2.54)$$

	current values ($\mu\bar{A}$)	Sensitivity	Accuracy requirement (% , ENOB) for $\Delta E_{ye} \leq 10\%$
w_0	286	20.65	0.48%, 7.7b
w_1	-389	28.19	0.35%, 8.2b
w_2	117	8.47	1.18%, 6.4b
I_0	14	1	10%, 3.3b
I_1	220	0.8	12.55%, 3b
I_2	558	2.02	4.95%, 4.3b

Table 2.3: Sensitivity and accuracy requirement to control eye reduction within 10%

Table 2.3 lists the computed eye sensitivities to each coefficient. Since magnitude of w_1 is the largest in Table 2.2, the eye is the most sensitive to w_1 according to Equation (2.54). For example, according to Table 2.2, 10% of w_1 current perturbation reduces the eye by

280%, completely closing it. Therefore, w_1 segment of a CS FFE has the most stringent accuracy constraint. From the mapping in Table 2.1, we can drive a formula for w_1 by solving simultaneous equation.

$$w_1 = -\frac{I_1 + I_2}{2} \quad (2.55)$$

From Equation (2.54) and (2.55), we can drive the eye sensitivity to w_1 as in Equation (2.56).

$$S_{w_1} = \left| \frac{w_1}{I_0} \right| = \frac{I_1 + I_2}{2I_0} \quad (2.56)$$

Since I_0 is much smaller than I_1 or I_2 , we can approximate S_{w_1} in terms of the channel loss $|T_{ii}(2\pi f_N)|$ at Nyquist frequency from Equation (2.46) and (2.56).

$$S_{w_1} \approx \frac{I_0 + I_1 + I_2}{2I_0} = \frac{\pi}{8|T_{ii}(2\pi f_N)|} \quad (2.57)$$

According to Equation (2.57), the eye sensitivity on w_1 becomes larger as the channel loss increases, limiting the performance of the link. From a designer's point of view, an interesting form of Equation (2.56) is the accuracy constraint on the w_i current source for a given target percentage of eye reduction β_{w_i} . As expressed in Equation (2.58) β_{w_i} is the desired bound of the eye reduction in percentage.

$$\beta_{w_i} = \left| \frac{\Delta E_{ye}}{E_{ye}} \right|_{\Delta w_n=0, n \neq i} \quad (2.58)$$

The accuracy requirement is expressed in Equation (2.59).

$$\left| \frac{\Delta w_i}{w_i} \right| = \frac{1}{S_{w_i}} \left| \frac{\Delta E_{ye}}{E_{ye}} \right|_{\Delta w_n=0, n \neq i} = \frac{\beta_{w_i}}{S_{w_i}} \quad (2.59)$$

By using equation (2.59), we can find the accuracy constraint on w_1 in terms of the channel loss and target eye reduction as shown in Equation (2.60).

$$\left| \frac{\Delta w_1}{w_1} \right| \leq \frac{8|T_{ii}(2\pi f_N)|}{\pi} \left| \frac{\Delta E_{ye}}{E_{ye}} \right|_{\Delta w_0, \Delta w_1=0} = \frac{8|T_{ii}(2\pi f_N)|\beta_{w_i}}{\pi} \quad (2.60)$$

Equation (2.60) states that w_1 must be controlled a lot more accurately than the desired eye reduction bound, due to the factor of channel loss. The computed accuracy constraint

of w_1 listed in Table 2.3 is about 0.35% when the target eye reduction bound β_{w_1} is 10%. The accuracy constraints on w_2 and w_0 are more relaxed than the one on w_1 because w_0 and w_2 have smaller values, as shown in Table 2.3, and thus have smaller sensitivity by Equation (2.54).

The relative accuracy constraint in CS FFE becomes too stringent because the small I_0 (or $-I_0$) current during a DC pattern, which directly affects the eye, is generated by linear addition and subtraction of three large current values: w_0 , w_2 and $|w_1|$. Since the differences between I_0 and w_0 , w_1 , and w_2 increase given larger channel loss, the accuracy constraint in Equation (2.59) becomes tougher as the data rate gets higher. This means that too tight accuracy requirements of the FFE coefficient become a limiting factor of high data rates (i.e. high channel loss) in VD, CML, and CS FFE designs that are based on analog summation for FFE computation.

Eye Sensitivity of CI FFE

In CI FFE, the eye sensitivities to the coefficients are much smaller and a lot less affected by the channel loss than the ones in the CS FFE because the DC transmit current I_0 is not generated by the subtraction from the large current taps: w_0 , w_1 , and w_2 . Instead, I_0 current is handled by a designated current source and the other large current segments (I_1 and I_2) are turned off while the transmitter conducts I_0 . Therefore, the CI FFE prevents large coefficient errors of the large current segments (I_1 and I_2) from affecting the transmit current ($= I_0$) for the DC pattern.

To theoretically analyze the error by each current source in CI FFE, we substitute $[w]*[d]$ with $[I_T]$ in Equation (2.48) and express ΔI_R in terms of ΔI_T as shown in Equations (2.61) and (2.62).

$$[I_R] = [h] * [I_T] \quad (2.61)$$

$$\Delta I_{Rn} = ([h] * [\Delta I_T])_n \quad (2.62)$$

For a DC pattern, I_T is a constant: I_0 or $-I_0$, and the magnitude of the channel's transfer function at DC, $\sum_{i=0}^{\infty} h_i$, is 1 as discussed earlier. Therefore, the received current is I_0 or $-I_0$ giving us Equation (2.63) and (2.64) for the I_R and ΔI_R when a DC pattern is being sent. This corresponds to the worst case ΔI_R due to error on I_0 .

$$I_R = I_T = \pm I_0 \quad (2.63)$$

$$\Delta I_{R-worst, \Delta I_1, \Delta I_2=0} = \Delta I_{T, DC} = \pm \Delta I_0 \quad (2.64)$$

From Equations (2.52), (2.53), (2.63), and (2.64), we can easily compute the eye sensitivity to the I_0 current segment as we did it for the one to w_1 in a CS FFE.

$$S_{I_0} = \frac{\left| \frac{\Delta E_{ye}}{E_{ye}} \right|}{\left| \frac{\Delta I_0}{I_0} \right|_{\Delta I_1, \Delta I_2=0}} = \frac{\left| \frac{2\Delta I_0}{2I_0} \right|}{\left| \frac{\Delta I_0}{I_0} \right|} = 1 \quad (2.65)$$

Equation (2.65) states that the percentage of eye change due to I_0 current error is equal to the percentage of I_0 error which is a lot smaller than the one in a CS FFE. As we derived the Equation (2.59), we can easily show that the required I_0 accuracy is exactly the same target percentage bound of eye reduction (β_{I_0}) by I_0 as shown in Equation (2.66).

$$\left| \frac{\Delta I_0}{I_0} \right| \leq \frac{1}{S_{I_0}} \left| \frac{\Delta E_{ye}}{E_{ye}} \right|_{\Delta I_1, \Delta I_2=0} = \beta_{I_0} \quad (2.66)$$

Therefore, to bound the eye reduction by I_0 current error to within 10%, the required accuracy constraint on I_0 is only 10%, which is a lot more relaxed than 0.35% in a CS FFE.

The accuracy constraints on other current sources (I_1 and I_2) are more complicated than that of I_0 because I_1 and I_2 are not always turned on. In the case of I_0 current error, the worst case transmit data pattern is simply a DC pattern (all 1 or 0) because the magnitude of the channel's transfer function at DC is 1. However, according to the mapping in Table 2.1, I_1 and I_2 cannot be turned on all the time. Rather, they are turned on/off depending on the data pattern and thus the impact of ΔI_1 and ΔI_2 on the received current I_R are modulated by the data pattern requiring worst case pattern study to get eye sensitivity on I_1 and I_2 .

Table 2.4 summarizes data-dependency of ΔI_T caused by error on the I_2 current source keeping all other current sources ideal. Since $I_{max} = I_0 + I_1 + I_2$ is conducted by turning all current sources on, ΔI_2 error shows up at the output node when I_T becomes $\pm I_{max}$ too.

Figure 2-17 visualizes $[\Delta I_T]$ sequence for an example bit pattern. For easy interpretation, Table 2.5 presents simplified data dependency of ΔI_T caused by the I_2 current error. ΔI_T becomes ΔI_2 at rising edge ('0'→'1') and $-\Delta I_2$ at falling edge ('1'→'0'). Otherwise, I_2

$D_0D_{-1}D_{-2}$	ΔI_T
1 1 1	0
1 1 0	0
1 0 1	ΔI_2
1 0 0	ΔI_2
0 1 1	$-\Delta I_2$
0 1 0	$-\Delta I_2$
0 0 1	0
0 0 0	0

Table 2.4: ΔI_T table caused by ΔI_2 error on I_2 current source

D_0D_{-1}	ΔI_T
1 1	0
1 0	ΔI_2
0 1	$-\Delta I_2$
0 0	0

Table 2.5: Simplified ΔI_T table caused by ΔI_2 error on I_2 current source

does not add an error to I_T . For an arbitrary bit pattern, the position of the edge can be at any place but the polarity must alternate because a rising edge must be eventually followed by a falling edge and vice versa. Therefore, $[\Delta I_T]$ is a sequence whose non-zero elements are placed at arbitrary positions of magnitude of $|\Delta I_2|$ and alternate polarities. For a given natural number m_i which satisfies $m_{i+1} > m_i$, we can express ΔI_R due to ΔI_2 .

$$\Delta I_R = \Delta I_2 \sum_{i=1}^{\infty} (-1)^{i-1} h_{m_i} \quad (2.67)$$

The worst case for a typical on-chip RC dominant channel occurs when there is a single transition at m_i where h_{m_i} is a peak value. The example sequence in Figure 2-7 (b) has its peak value at $n = 3$, and therefore, the worst ΔI_R is expressed in Equation (2.68).

$$\Delta I_{R-worst, \Delta I_0, \Delta I_1=0} = \pm \Delta I_2 h_{peak} = \pm \Delta I_2 h_3 \quad (2.68)$$

From Equation (2.52), (2.53), and (2.68), we derive the eye sensitivity on I_2 current source.

$$S_{I_2} = \frac{\left| \frac{\Delta E_{ye}}{E_{ye}} \right|}{\left| \frac{\Delta I_2}{I_2} \right|_{\Delta I_0, \Delta I_1=0}} = \frac{2\Delta I_2 h_{peak}}{2I_0} = \frac{I_2 h_3}{I_0} \quad (2.69)$$

According to Table 2.3, the percentage change in I_2 current results in twice the per-

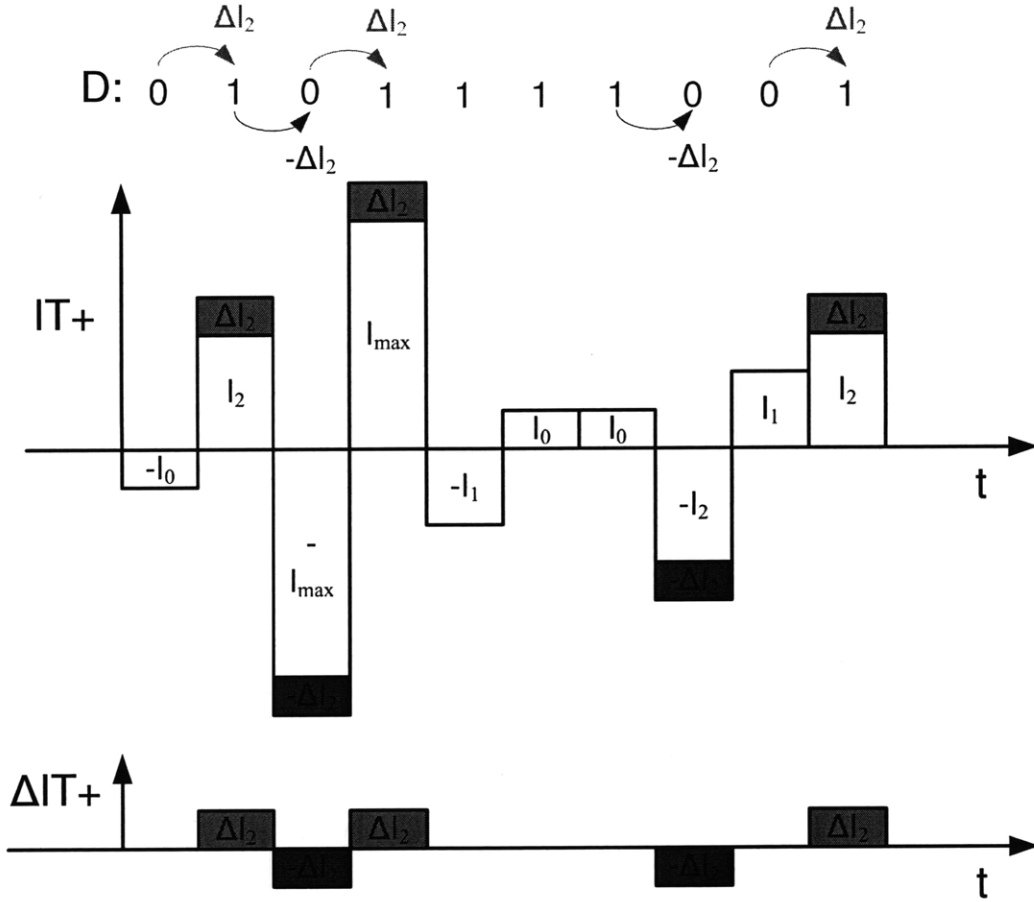


Figure 2-17: An example ΔI_T caused by ΔI_2 in CI FFE.

centage change in eye at the receiver. This is a lot less sensitive than the one for w_1 in CS FFE. This can be intuitively understood as follows. Although the current error by I_2 at the transmitter is larger than the vertical eye itself, the actual impact on the eye at the receiver is attenuated by the channel loss because I_2 only conducts at bit flips ('1'→'0' or '0'→'1'). Therefore, in Equation (2.67), the opposite polarities of h_i cancel each other and reduce the magnitude of the channel's transfer function for transient signal ΔI_2 . As a result, ΔI_2 is attenuated by factor of h_{peak} , and the impact on ΔE_{ye} is relieved.

For given accuracy requirement β_{I_2} for the eye, we can restate Equation (2.69) for I_2 accuracy constraint.

$$\frac{|\Delta I_2|}{I_2} = \frac{|\Delta E_{ye}|}{S_{I_2} E_{ye}} \leq \frac{\beta_{I_2}}{S_{I_2}} \quad (2.70)$$

Since $S_{I_2} \approx 2$, I_2 current source requires only twice that of target relative eye accuracy, and this accuracy requirement rarely depends on the channel loss.

We can find the sensitivity and relative accuracy requirement of I_1 using a similar approach. The difference is that the I_1 current source conducts the opposite polarity at one bit time after data edge. The worst case ΔI_R is similar to Equation (2.68) as shown in Equation (2.71).

$$\Delta I_{R-worst, \Delta I_0, \Delta I_2=0} = \pm \Delta I_1 h_{peak} = \pm \Delta I_1 h_3 \quad (2.71)$$

By using Equations (2.52), (2.53), and (2.71), we can derive the eye sensitivity to I_1 and accuracy constraint on I_1 as shown in Equations (2.72) and (2.73).

$$S_{I_1} = \frac{\left| \frac{\Delta E_{ye}}{E_{ye}} \right|}{\left| \frac{\Delta I_1}{I_1} \right|_{\Delta I_0, \Delta I_2=0}} = \frac{\frac{2\Delta I_1 h_{peak}}{2I_0}}{\frac{\Delta I_1}{I_1}} = \frac{I_1 h_{peak}}{I_0} = \frac{I_1 h_3}{I_0} \quad (2.72)$$

$$\frac{|\Delta I_1|}{I_1} = \frac{1}{S_{I_1}} \frac{|\Delta E_{ye}|}{E_{ye}} \leq \frac{\beta_{I_1}}{S_{I_1}} \quad (2.73)$$

Since I_1 is smaller than I_2 , the eye is less sensitive to I_1 than I_2 according to Equations (2.70) and (2.73).

Table 2.3 summarizes the required relative accuracy of each current source to restrict the eye perturbation to within 10% for the channel described in Chapter 3, assuming 4Gb/s operation. The most stringent accuracy constraints in CI FFE and in CS FFE are 5% for I_2 and 0.35% for w_1 , respectively. The result shows that the current source accuracy requirement in CI FFE is relaxed more than ten times compared to the one in CS FFE. The accuracy constraint in CI FFE weakly depends on the channel loss because I_0 current source is handled by a designated current source and the channel attenuates current perturbation on I_1 and I_2 . Therefore, CI FFE can work for a channel with much higher loss than CS FFE, without expensive high-resolution driver segments.

2.3.5 Parameter Extraction and Model Usage: LCM Driver Example

In order to build intuition about the design of an equalizing transceiver, in Subsection 2.2.3 and 2.2.4, the transfer function is explained in terms of the termination impedance of the driver. In real usage of the model for CAD applications, the impedance parameters must be

derived from the transistor models such as a SPICE raw data, and other link components such as a pre-driver must be considered. For some driver types such as VD Low Common Mode (LCM) [32, 33] drivers, transistor characteristics are necessary, and the pre-driver is sized proportional to the driver width.

In this subsection, as an example, we show how an LCM driver is simplified and modeled as an RC switch circuit to allow simplified transfer function computation. This subsection also shows how the model can be combined with extracted driver and pre-driver parameters. The RC switch model is accurate enough to capture the link behavior and provides much faster computation speed than a SPICE simulation. This RC switch model is also used for the pre-drivers. The other driver types such as a CML, CS, CI, and Source-Series-Terminated drivers can be modeled using similar approaches.

Figure 2-2 shows the overview of a 3-tap LCM equalizing transceiver with design parameters: V_p , V_s , w_0 , w_1 , w_2 , W_{LCM} , W_{th} , S_p , T_d , and y_1 . V_p and V_s are the pre-driver's supply voltage and signal supply voltage. w_0 , w_1 , and w_2 are the FFE coefficients. W_{LCM} is the total width of the LCM driver. W_{th} and S_p are the wire's width and space. T_d is the receiver's sample delay and y_1 is the DFE tap coefficient of the receiver. In this subsection, the normalized RC switch models for the pre-driver and driver are explained for given V_p and V_s parameters. These RC models can be used to construct simplified pre-driver and driver models when they are combined with w_0 , w_1 , w_2 , and W_{LCM} parameters.

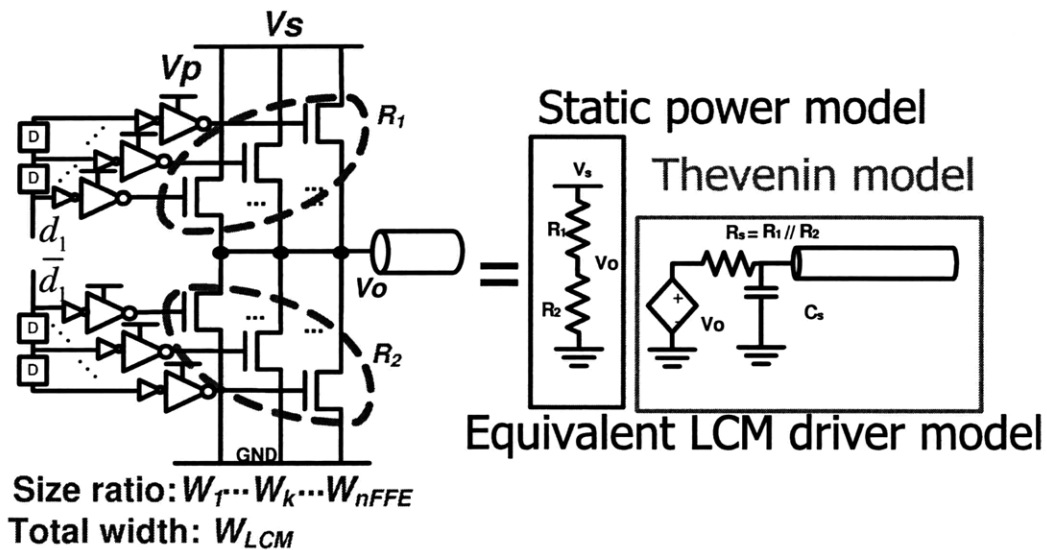


Figure 2-18: An LCM driver and its equivalent model.

Figure 2-18 shows a schematic and the equivalent linearized model of an LCM driver. The gate voltage of each transistor is digitally controlled by an inverter-based pre-driver which has separate power supply voltage V_p . To keep the NMOS in triode region, typically driver's signal power supply V_s is chosen less than V_p , and V_p is set to V_{dd} in this paper.

An LCM driver consists of pull-up and pull-down pair segments. In each segment, the pull-up and pull-down NMOSs are sized for the same resistance, and each segment corresponds to one of the FFE tap coefficients $\underline{w}^T = [w_1 \dots w_{n_{FFE}}]$, since the resistance of each segment is set to be proportional to the inverse of each tap coefficient w_i . Note that w_i is a normalized coefficient so that $\sum_{i=1}^{n_{FFE}} w_i = 1$. The total LCM driver width (the sum of widths of all segments) is parameterized by W_{LCM} .

By turning on either pull-up or pull-down transistors in each segment, the LCM driver controls the total pull-up and pull-down resistance R_1 and R_2 while keeping the Thevenin resistance R_s constant. The Thevenin equivalent output voltage V_o is determined by the R_1 and R_2 voltage divider.

When different segments are driven with delayed data, this driver becomes an analog FIR filter [32], which can be used as an FFE. At the link model layer, our tool uses the linearized LCM model as a controlled voltage source with impedance R_s and parasitic capacitance C_s that captures the transient response of the LCM driver.

As shown in Equations (2.74), (2.75), and (2.76), R_s and C_s as well as the LCM driver's total input gate capacitance C_g can be expressed in terms of the total driver width W_{LCM} by using the normalized technology- and voltage- dependent constants: R_{LCM} (Ohm-um), C_{dLCM} (fF/um), and C_{gLCM} (fF/um).

$$R_s = R_{LCM}/W_{LCM} \quad (2.74)$$

$$C_s = C_{dLCM}W_{LCM} \quad (2.75)$$

$$C_g = C_{gLCM}W_{LCM} \quad (2.76)$$

The normalized conductance ($1/R_{LCM}$) is obtained by driving static current through a triode-region transistor with various pre-driver supply V_p and driver supply V_s values and by the setting output voltage to $V_s/2$. The voltage ranges (V_p , V_s) that cause large non-linearity error are eliminated from the design space. As shown in Figure 2-19, the

conductance is then expressed as a linear function of V_p and V_s within the range of interest.

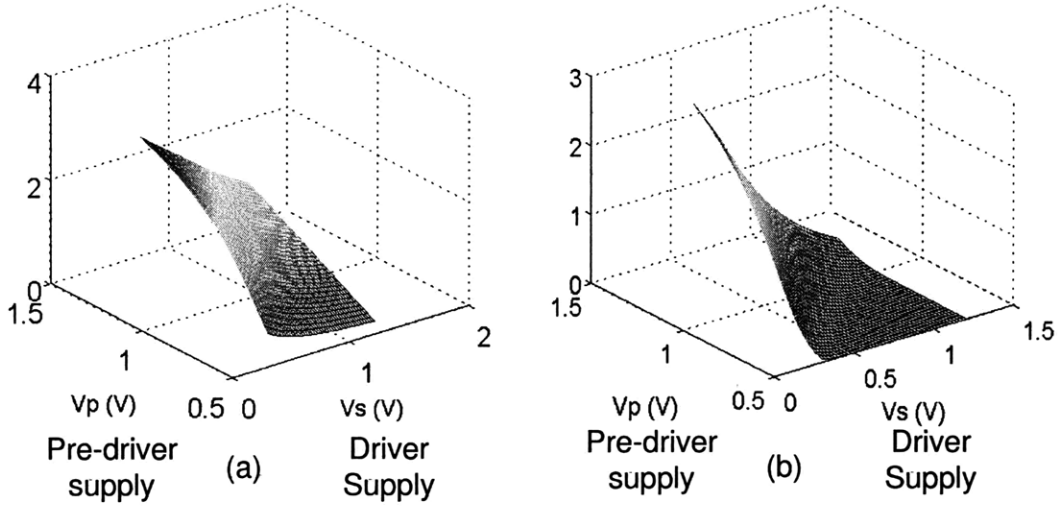


Figure 2-19: LCM driver's normalized (a) pull-down and (b) pull-up conductance.

The normalized capacitance (C_{dLCM}) is extracted by matching the delay of the LCM driver to an equivalent linearized model using the setup as shown in Figure 2-20 (a). Since the average of rising and falling delay can be modeled as $0.69R_s(C_{load} + C_s)$ as shown in Figure 2-20 (b), fitting the delay into a linear formula of normalized load capacitance C_{load}/W_{LCM} gives us C_{dLCM} .

The pre-driving inverters are sized proportional to the LCM driver's gate capacitance with fanout factor E_F using a linear model in Equations (2.77), (2.78), and (2.79) with normalized parameters: R_{Pre} (Ohm- μm), C_{gPre} (fF/ μm), and C_{dPre} (fF/ μm).

$$R_{inv} = R_{Pre}/W_{pre} \quad (2.77)$$

$$C_{ginv} = C_{gPre}W_{pre} \quad (2.78)$$

$$C_{dinv} = C_{dPre}W_{pre} \quad (2.79)$$

The normalized parameters for the pre-driving inverter are extracted using a similar procedure as for the LCM driver.

For pre-driver power, we assume that the inverter-based predriver is sized proportional to the driver size with fanout of E_F . This assumption gives us Equation (2.80).

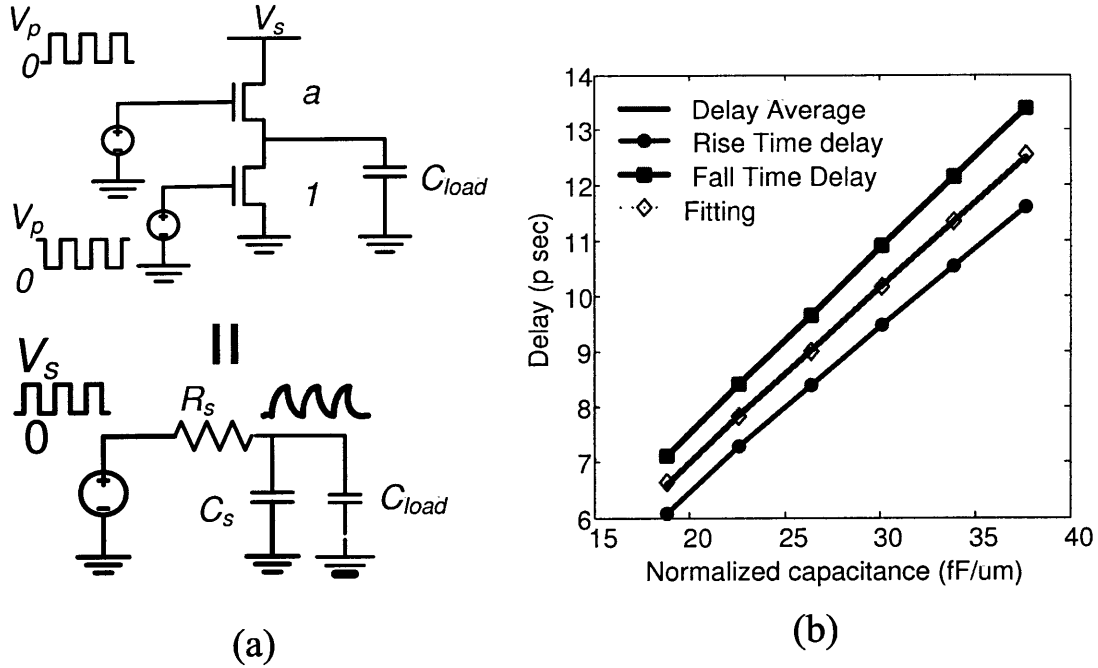


Figure 2-20: LCM driver's (a) C_s extraction setup and (b) delay versus normalized load capacitance.

$$E_{Pre} = \alpha \left(\frac{1/E_F}{1 - 1/E_F} \frac{C_{gPre} + C_{dPre}}{C_{gPre} + 1} \right) C_{gLCM} W_{LCM} V_p^2 \quad (2.80)$$

α is the average activity factor, and C_{gPre} , C_{dPre} are the transistor-width normalized pre-driver gate and diffusion capacitors, and C_{gLCM} is the gate capacitance of the LCM driver. Since the LCM equalized interconnects use a differential signaling scheme, the total energy consumption is twice the sum of the LCM driver energy and the pre-driver energy: $E_{btot} = 2(E_{LCM} + E_{Pre})$ when the transmitter power is dominant.

The extracted parameters such as Thevenin resistance of the LCM driver, or parasitic capacitance can be used in Equations described in Section 2.2 to compute the transfer function. Once the transfer function is computed, the equalization circuit can be realized from the transfer function for the given FFE and DFE tap counts.

2.4 Equalization

The performance estimation of the equalized link is time consuming due to the large number of numerical calculations needed to extract the performance and equalizer coefficients from

a variety of different channels (for various wire and circuit sizes) in design space exploration. An appropriate performance model speeds up the two major bottlenecks (finding optimal sampling time and equalization coefficients) by at least an order of magnitude each, resulting in more than two orders of magnitude faster design exploration. We derive the closed-form solution for near-optimal sampling time in terms of the frequency response of the channel and also show that, for RC-dominant channels, the swing-constrained least-mean square based equalization yields similar results (albeit much faster) than a conservative eye maximization algorithm.

2.4.1 Frequency Domain Analysis: Optimal Sampling Time

The received eye is affected by the channel attenuation, inter-symbol interference (ISI), and crosstalk. In a well equalized channel, the optimal sampling time maximizes received signal amplitude, assuming that crosstalk and residual ISI distributions are relatively uniform across the bit time. For n_{FFE} -tap FFE transmitter with an equalization coefficient vector \underline{w} , the frequency spectrum of the received signal $Y(f)$ is shown in Equations (2.81) and (2.82)

$$Y(f) = T_s \text{sinc}(fT_s) e^{-j\pi T_s T(f)} L(f) \underline{w} \quad (2.81)$$

$$L(f) = [1 \ e^{-j2\pi f T_s} \ \dots \ e^{-j2\pi f T_s (n_{FFE}-1)}] \quad (2.82)$$

where $\text{sinc}(f)$, $T(f)$, and T_s are the sinc function, transfer function of the channel, and the symbol time, respectively. $L(f)\underline{w}$ represents the FFE's transfer function. If we sample the received pulse response $y(t)$ after latency time T_d , then the frequency response of the sampled sequence $Y_{ds}(f)$ can be approximated as shown in Equations (2.83) and (2.84).

$$Y_{ds}(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} Y(f - 2kf_N) e^{-j2\pi 2kf_N T_d} \quad (2.83)$$

$$\approx \frac{1}{T_s} \left(Y(f - 2f_N) e^{-2\pi 2f_N T_d} + Y(f) + Y(f + 2f_N) e^{j2\pi 2f_N T_d} \right) \quad (2.84)$$

The received signal spectrum $Y(f)$ is assumed to be band-limited due to significant channel roll-off past 2x of the Nyquist frequency f_N . On the other hand, expressing $Y_{ds}(f)$ with received signal samples y_k gives Equation (2.85)

$$Y_{ds}(f) = e^{-j2\pi f T_d} \sum_{k=-\infty}^{\infty} y_k e^{-j2\pi f k T_s} \approx e^{-j2\pi f T_d} (y_0 + y_1 e^{-j2\pi f T_s}) \quad (2.85)$$

where y_0 is the main tap of the sampled received pulse response, i.e. the value to be maximized. FFE will minimize all received pulse response samples except the main (y_0) and the first post-cursor (y_1), which is handled by the DFE. By setting the frequency f in Equations (2.84) and (2.85) to zero and the Nyquist frequency (f_N), and ignoring frequency response above 2x of the Nyquist frequency, we obtain a set of equations to solve for y_0 and y_1 as expressed in Equations (2.86) and (2.87).

$$Y_{ds}(0) \approx \frac{1}{T_s} Y_{ds}(0) \approx y_0 + y_1 \quad (2.86)$$

$$Y_{ds}(f_N) \approx \frac{1}{T_s} \left(Y(-f_N) e^{-j2\pi 2f_N T_d} + Y(f_N) \right) \approx e^{-j2\pi f_N T_d} (y_0 - y_1) \quad (2.87)$$

Solving Equations (2.86) and (2.87) for y_0 and y_1 allows us to approximate y_0 in terms of the received frequency spectrum at $f=0$, f_N , and the sampling delay T_d .

$$y_0 \approx \frac{Y(0)}{2T_s} + \frac{1}{T_s} |Y(f_N)| \cos(2\pi f_N T_d + \angle Y(f_N)) \quad (2.88)$$

Using Equations (2.81), (2.82) (2.88), the T_d that maximizes the received signal is derived in Equation (2.89).

$$T_d \approx -\frac{\angle Y(f_N)}{2\pi f_N} = \frac{T_s}{2} - \left(\frac{\angle(L(f_N)\underline{w})}{2\pi f_N} + \frac{\angle T(f_N)}{2\pi f_N} \right) \quad (2.89)$$

In Equation (2.89), $T_s/2$ is the time interval from the edge of the square pulse to its center (i.e. half the symbol time). $-\frac{\angle(L(f_N)\underline{w})}{2\pi f_N}$ is the delay of the FFE equalizer that is equal to $(n_{main} - 1)T_s$ where n_{main} is the index of the maximum valued equalization coefficient, and $-\frac{\angle T(f_N)}{2\pi f_N}$ is the channel delay at the Nyquist frequency.

2.4.2 Swing Constrained Least Mean Square Error Solution

Maximization of The Worst-Case Eye Opening

The preferred solution for conservative on-chip circuit design environment is to optimize the equalizer coefficients to satisfy the worst-case eye opening requirement. This problem can be formulated as a large linear program [36]. The equalized received sequence \underline{y} and

received crosstalk \underline{c} can be written as shown in Equations (2.90) and (2.91)

$$\underline{y} = \mathbf{H}\underline{w} = [\underline{h}_1 \ \underline{h}_2 \ \dots \ \underline{h}_n]\underline{w} \quad (2.90)$$

$$\underline{c} = \mathbf{H}_c\underline{w} = [\underline{h}_{c1} \ \underline{h}_{c2} \ \dots \ \underline{h}_{cn}]\underline{w} \quad (2.91)$$

where \mathbf{H} and \mathbf{H}_c are the Toeplitz matrices whose column vectors are the time shifted sampled pulse response vectors of \underline{h} (through-channel) and \underline{h}_c (crosstalk). Here we assume that all equalizers in a parallel link bus are optimized to have the same coefficients and that these coefficients are found to jointly minimize the ISI and crosstalk. The optimal T_d determines the main received signal sample, corresponding to the transmitted bit, y_{main} and the ISI term y_{isi} .

$$y_{main} = \underline{h}_{sig}^T \underline{w} \quad (2.92)$$

$$y_{isi} = \mathbf{H}_{isi}\underline{w} \quad (2.93)$$

\underline{h}_{sig} is the row vector of \mathbf{H} at the index corresponding to T_d and \mathbf{H}_{isi} is the inter-symbol interference matrix derived from \mathbf{H} by puncturing the row vectors that correspond to the main and post-cursor taps covered by DFE. The vector \underline{y}_{isi} represents the ISI sequence generated by one bit transmission.

The worst case eye opening when independent and identically distributed (i.i.d.) random bit patterns are transmitted is expressed in Equation (2.94).

$$E_{ye,worst} = \underline{h}_{sig}^T \underline{w} - \|\mathbf{H}_{isi}\underline{w}\|_1 - \|\mathbf{H}_c\underline{w}\|_1 \quad (2.94)$$

Equation (2.94) gives the following formulation for optimal equalization coefficients \underline{w}

$$\text{maximize} \quad E_{ye,worst} \quad (2.95)$$

$$\text{subject to} \quad \|\underline{w}\|_1 \leq 1 \quad (2.96)$$

where l_1 -norm of \underline{w} limits the maximum voltage swing of the FFE. By using the epigraph form and expanding the l_1 -norm terms in Equations (2.94), (2.95) and (2.96) we get the linear program formulation.

$$\text{maximize} \quad E_{ye} \quad (2.97)$$

$$\text{subject to} \quad E_{ye} - \underline{h}_{sig}^T \underline{w} + \underline{d}_j^T \mathbf{H}_{isi} \underline{w} + \underline{d}_k^T \mathbf{H}_c \underline{w} \leq 0 \quad (2.98)$$

$$\underline{s}_n^T \underline{w} - 1 \leq 0 \quad (2.99)$$

$$\forall j, k | \underline{d}_k, \underline{d}_k \in \{\pm 1\}^{length(\mathbf{H}_{isi} \underline{w})} \quad (2.100)$$

$$\forall n | \underline{s}_n \in \{\pm 1\}^{length \underline{w}} \quad (2.101)$$

The first $2^{length(\mathbf{H}_{isi} \underline{w})}$ constraints represent Equation (2.94) and the next $2^{length(\underline{w})}$ constraints represent the l_1 -norm of \underline{w} . Since the number of constraints grows exponentially with the length of the pulse response, linear program in Equations (2.97-2.101) can be rather slow, so we use the numerical gradient solver on the original problem in Equation (2.95) and (2.96) to directly compute the l_1 -norms. Although it speeds up the computation, this method is still about an order of magnitude slower than the closed-form least-mean-square equalization (LMSE) algorithm described next.

Swing Constrained Least Mean Square Error Solution

Although in general LMSE does not maximize the worst-case eye opening, the LMSE is very close to the worst-case eye opening solution for RC-dominant on-chip wires. The LMSE finds the equalization coefficients that minimize the ISI and crosstalk energy (i.e. their l_2 -norm) with closed form solution for equalization.

In the LMSE algorithm, we first set the main received signal to unity and then minimize the ISI and crosstalk energy from Equations (2.90), (2.91), (2.92), and (2.93) using a method of Lagrange multipliers.

$$y_{main} = \underline{h}_{sig}^T \underline{w} = 1 \quad (2.102)$$

$$E_N = |\underline{y}_{isi}|^2 + |\underline{c}|^2 = \underline{w}^T (\mathbf{H}_{isi}^T \mathbf{H}_{isi} + \mathbf{H}_c^T \mathbf{H}_c) \underline{w} \quad (2.103)$$

$$\underline{w}_{lmse} = \frac{(\mathbf{H}_{isi}^T \mathbf{H}_{isi} + \mathbf{H}_c^T \mathbf{H}_c)^{-1} \underline{h}_{sig}}{\underline{h}_{sig}^T (\mathbf{H}_{isi}^T \mathbf{H}_{isi} + \mathbf{H}_c^T \mathbf{H}_c)^{-1} \underline{h}_{sig}} \quad (2.104)$$

To satisfy the maximum voltage constraint $\|\underline{w}\| \leq 1$, \underline{w}_{lmse} must be normalized.

2.5 CAD Flow and Modeling Integration

In this section, infrastructure for design space exploration of equalized links is explained [37]. Subsection 2.5.1 shows how the CAD tool is organized. Subsection 2.5.2 shows a case study using this CAD tool. Subsection 2.5.3 describes how the link estimation tool is connected with a network simulation tool.

2.5.1 CAD Flow

As a summary of modeling of all the link components, in this section we illustrate the CAD flow that combines all the models to explore the link design space. Figure 2-21 shows an example hierarchical optimization flow of an LCM driver serial link through an RC-dominant wire with technology-dependent and independent parameters. The model is based on the fundamental technology database such as a SPICE transistor model, a wire's conductivity model, and a wire's dielectric constant model. By using 2D field solver as explained in Section 2.2, the wire's *RLGC* matrix database is constructed with the wire's dimension parameters: W_{th} and S_p . A linear RC extraction program simplifies the inverter and LCM driver into normalized RC switches as in logical effort model for various pre-driver and signal voltages, as explained in Section 2.3. The channel's transfer function for a given wire length can be constructed based on the 2D *RLGC* matrix and the normalized RC switch model database for a given W_{th} , S_p , W_{LCM} , V_p , V_s , and target distance l . Multi-channel property can be described by two dominant through- and crosstalk- transfer functions ($T(f)$, $T_c(f)$) with minor accuracy degradation. For a given channel's transfer functions and a link architecture (eg. FFE and DFE tap number), the link performance tool finds the optimal FFE and DFE coefficients as well as the optimal sample delay as explained in Section 2.4. From those, the tool also estimates the eye height and data rate density. The link power tool evaluates the power consumption of the link with parameters given by the link performance tool. Finally, the performance (*eye height*, *data rate density*, *latency*) and the power/energy consumption are combined, summarized, and reported. These reported numbers are all associated with basic design parameters so that designers at upper levels of hierarchy can utilize the results in network architecture design.

Table 2.6 summarizes the total design exploration run time using closed form equalization and optimum delay expressions. The test run shows that the run time is improved

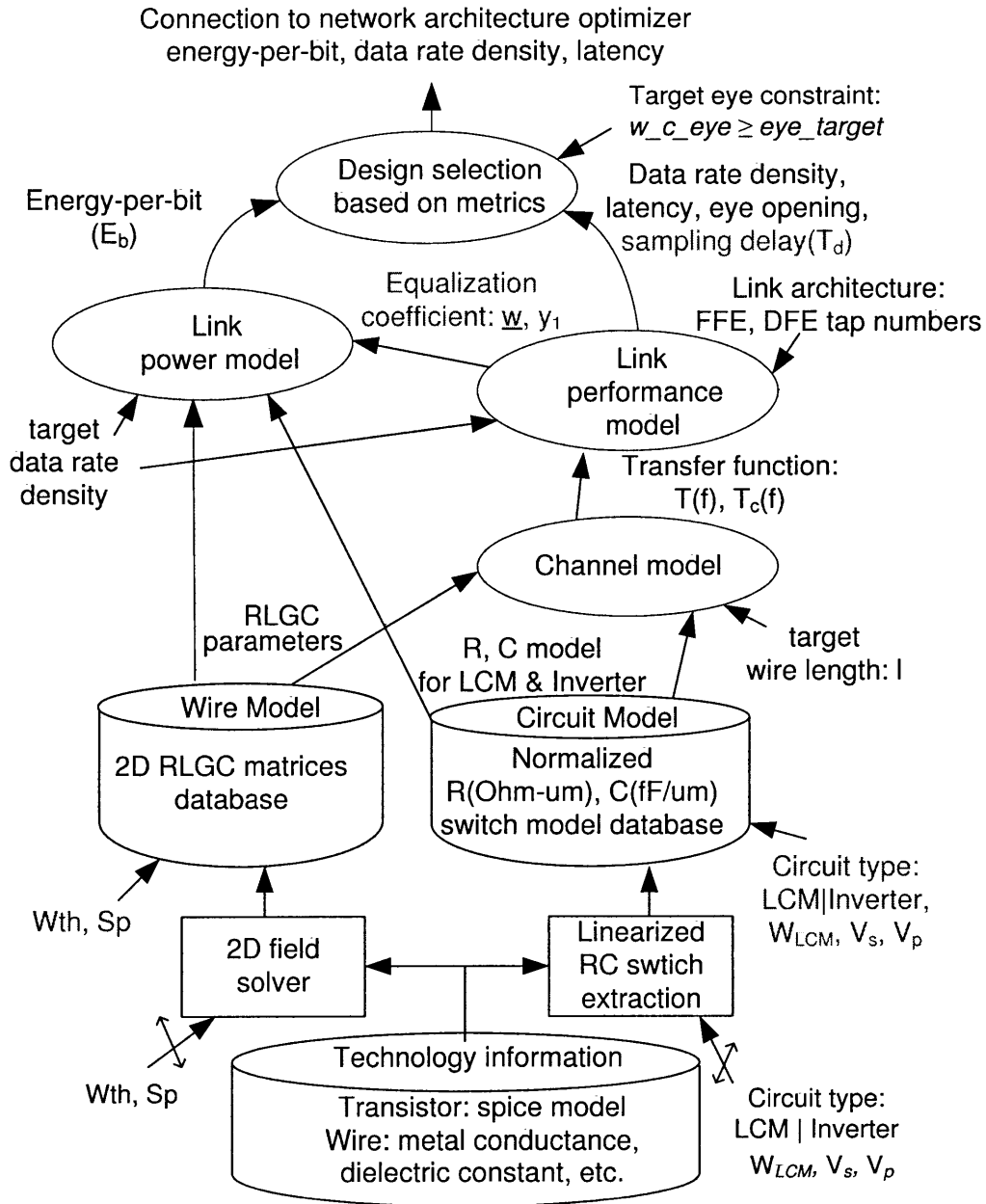


Figure 2-21: CAD flow.

by thirteen times by using the swing constrained least mean square solution. By using the closed form optimal sampling time, the run time is improved by twenty times. By combining two methods, the algorithm improved the run time by 244 times compared to the brute force method. Note that the brute force method itself is still much faster than the SPICE simulation.

423,000 design points	Swing constrained Least Mean Square Error and optimal sampling time	Maximization of the worst case eye and optimal sampling time	Maximization of the worst case eye and 20x oversampling
Run time (h)	0.74	9.7	180
Normalized run time	1	13	244

Table 2.6: Exploration time comparison

2.5.2 Link Design-Space Exploration

90nm Example Run

We use our tool to explore the link design space for a 10 mm long wire, in 90 nm, 1.2 V CMOS technology. We use the link architecture in Figure 2-2, with a 3-tap LCM FFE transmitter and a 1-tap loop-unrolled DFE receiver. To illustrate the results of joint wire and circuit sizing, we use this architecture and explore the link metrics trade-offs by varying the wire width and spacing, driver size, and supply voltage as well as the worst-case eye requirement. In Figure 2-22 we show a comparison of the optimized equalized interconnect and repeated interconnect. Repeaters are also optimized jointly with wires to reduce energy cost for the same throughput density and latency as equalized wires [38, 39].

For the M8 wire, the equalized interconnect consumes much less power than the repeated interconnect. In metal layers M2-6, equalized interconnects are still superior to repeaters but the benefit of equalization is smaller than at the M8 layer. Equalization at these lower metal levels enables the use of medium-to-long wires, therefore potentially alleviating the congestion at the top M8 layer in hierarchical on-chip networks. The energy savings and data-rate density are strong functions of the required worst-case eye opening since that determines the required voltage swing on a wire. Interestingly, the equalized interconnect not only decreases the energy-per bit for the same data rate density, but also pushes the trade-off to larger data rate density.

In Figure 2-23 the energy breakdown for each link component, with pre-driver fanout $E_F=3$, shows a dominant static power component. This is a shortcoming of the LCM drivers and indicates room for further improvement at the circuit level. Note that in on-chip applications, even with this static power component, LCM drivers are a lot more energy-efficient than high common mode differential pair (CML) drivers [32].

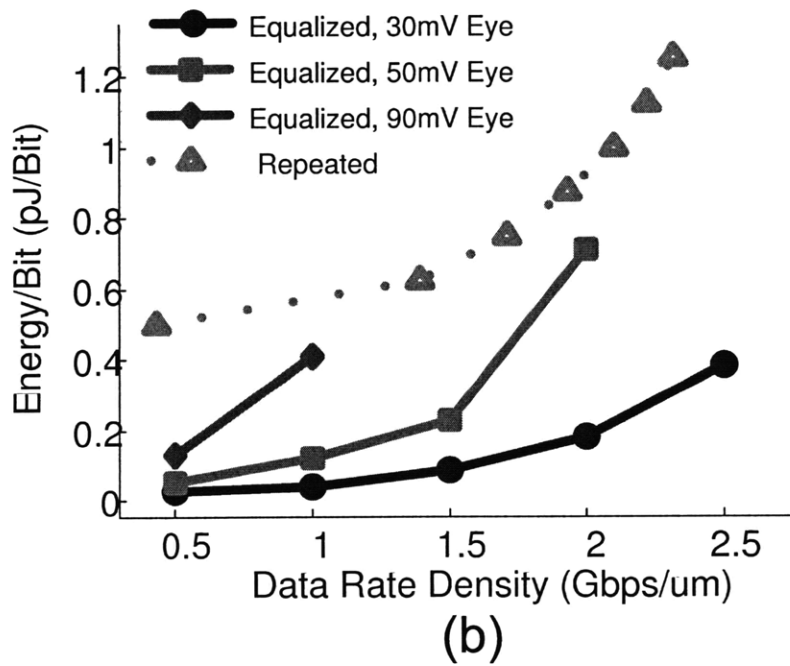
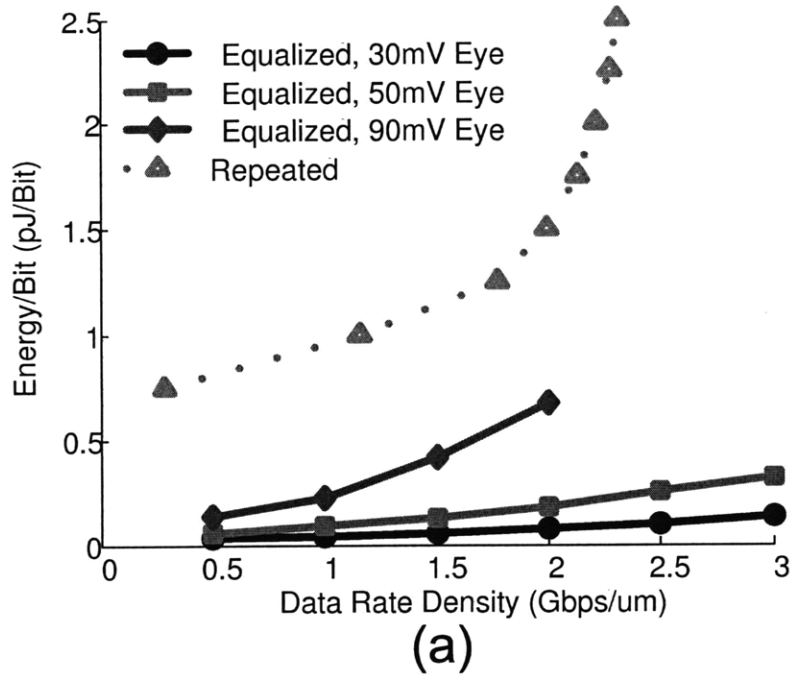


Figure 2-22: Comparisons of repeated and equalized interconnects: (a) M9 10mm wire (b) M2-6 10mm wire.

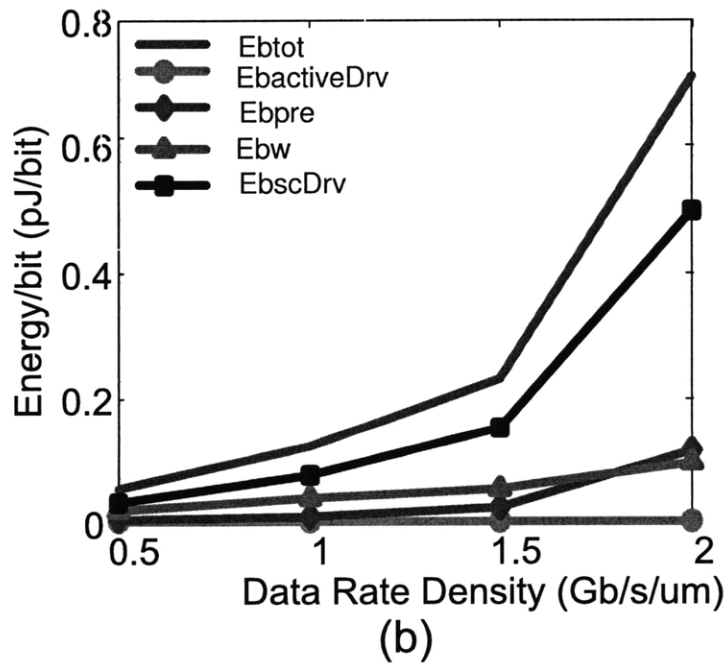
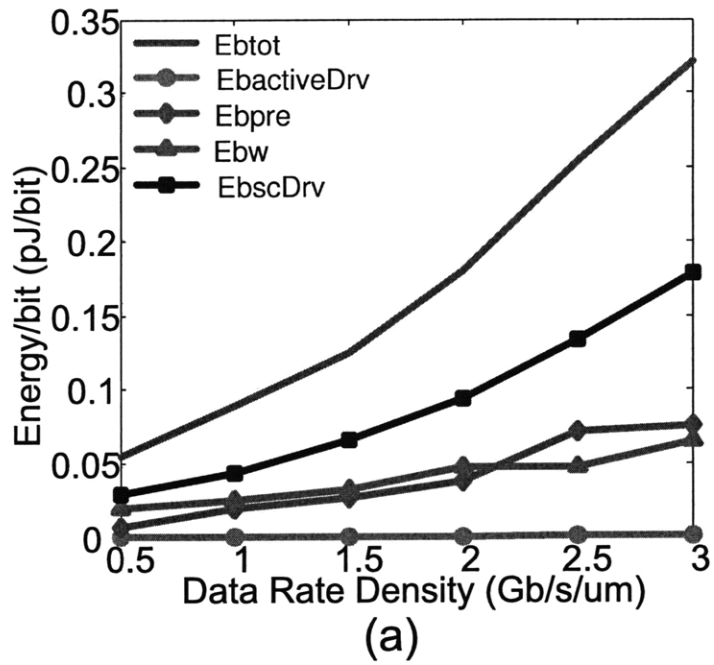


Figure 2-23: Energy breakdowns of LCM equalized interconnects: (a) M9 10mm wire (b) M2-6 10mm wire. E_{btot} is a total power consumption. $E_{bactiveDrv}$ is power consumption due to the parasitic capacitance at the transmitter output node. E_{bpre} is the energy consumption by pre-drivers. E_{bw} is energy to drive wire. E_{scDrv} is energy wasted in voltage division.

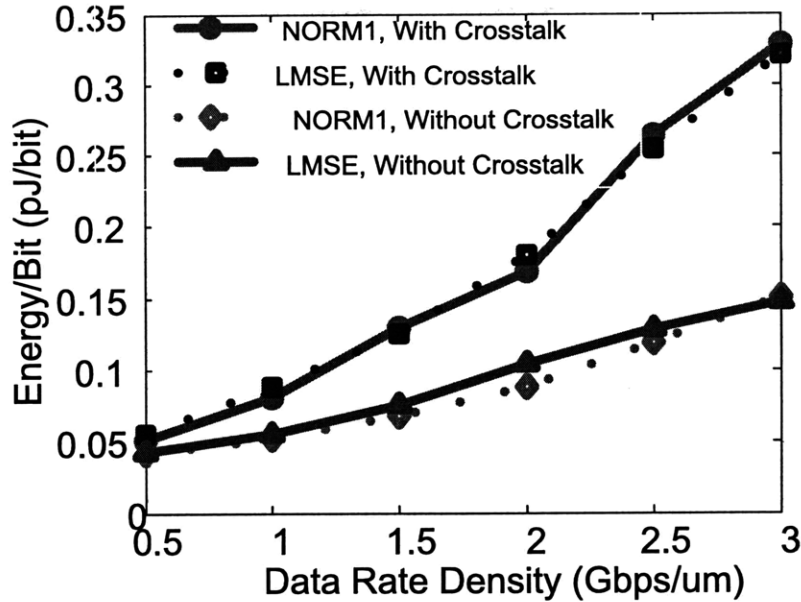


Figure 2-24: Impact of crosstalk and comparison of equalization algorithm.

Figure 2-24 shows that crosstalk is a significant factor in energy cost per bit and data rate density computation. Some improvement is still possible since we did not use differential wire criss-crossing [40] to make the crosstalk common-mode. In Figure 2-24, we also compare LMSE and worst-case eye (l_1 -norm) equalization, showing very little difference between the algorithms, even with crosstalk, although the worst-case eye method requires 13x more computation time than LMSE. The optimal delay formula speeds up the tool by another order of magnitude.

Figure 2-25 compares the estimated energy cost of the equalized interconnect with the result of SPICE and 2D field solver simulation. Figure 2-26 compares the estimated eye sizes by the proposed tool and the simulated eye sizes by SPICE and a 2D field solver. Both Figure 2-25 and 2-26 verify the accuracy of the tool.

32nm Case Study

Using the tool explained in Subsection 2.5.1, this subsection presents the case study of the trade-offs of both repeated and equalized interconnects for various NoC scenarios in a 32 nm technology node. By exploring the interconnect design space, we obtain the optimized interconnect metrics necessary for higher-level NoC architecture study. In the following

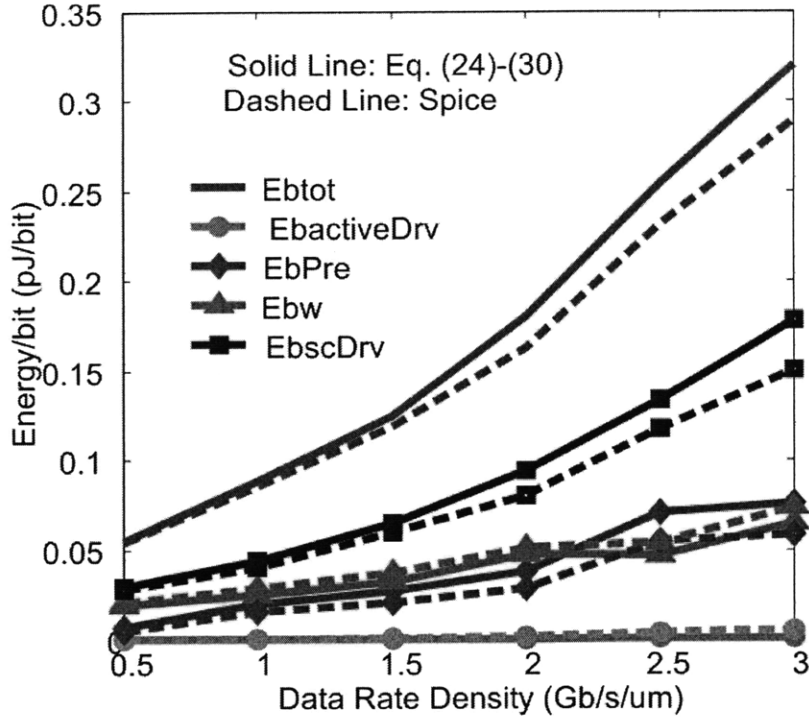


Figure 2-25: Energy cost comparison to SPICE and 2D field solver simulation.

sections, we first describe the cross-hierarchical NoC design flow, followed by different motivating NoC interconnection scenarios and models for design space exploration of equalized and repeated interconnects. The results indicate significant latency (at least 2x) and energy-efficiency (up to 10x) savings when equalized interconnects are used in place of repeated interconnects for 5-15 mm express-lanes in global routing layers. At lower metal layers the energy-efficiency benefits diminish with a break-point occurring at M5-6 semi-global layers, while the latency benefits remain.

Figure 2-27 shows the trade-off contours of repeated interconnects compared to the equalized interconnect trade-off curve with energy cost label using the tool explained in this chapter. Each contour of the repeater trade-off surface represents the equi-energy level. The energy-contours indicate the sensitivity of the trade-off between data rate density and latency for a given energy budget. In an M9 metal layer, the plots show that repeated interconnects cost 3-10x more energy than equalized interconnects for the same range of data rate densities while having at least 2x higher latency.

In an M6 metal layer, the equalized interconnect energy-efficiency gain is smaller than in a M9 metal layer due to poorer wire resistance and higher capacitance per unit length.

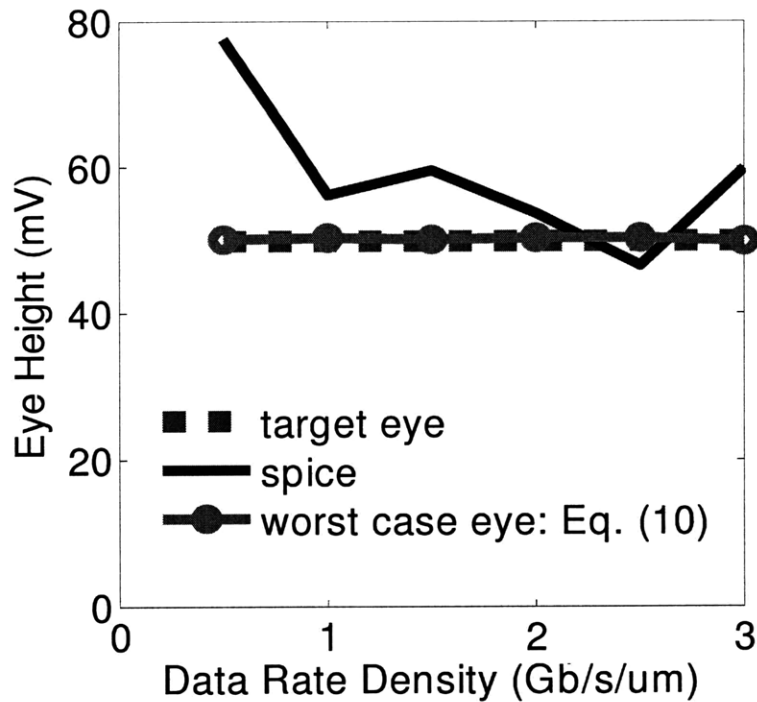


Figure 2-26: Eye size comparison to SPICE and 2D field solver simulation.

Still, the latency benefit of the equalized interconnect is about 2x better than the repeated in both M6 and M9 layers. The high attenuation in a M6 layer does not significantly affect phase delay of equalized interconnect but requires many repeater stages resulting in poor delay.

2.5.3 Connection to Network Simulation

Figure 2-28 shows the connection of the link simulation tool and the NoC simulation tool. At the bottom layer, the link CAD tool explained in Chapter 2 provides the link trade-off curve within given design space and the link design parameter associated with the trade-off curve. The trade-off curve can be taken and combined with an NoC CAD tool. The NoC CAD tool can analyze NoC metrics for various NoC topologies and access patterns. By using the generated NoC trade-off curve, the NoC design can be selected for a design purpose, and the link parameter associated with the NoC simulation run can be used for the link designer.

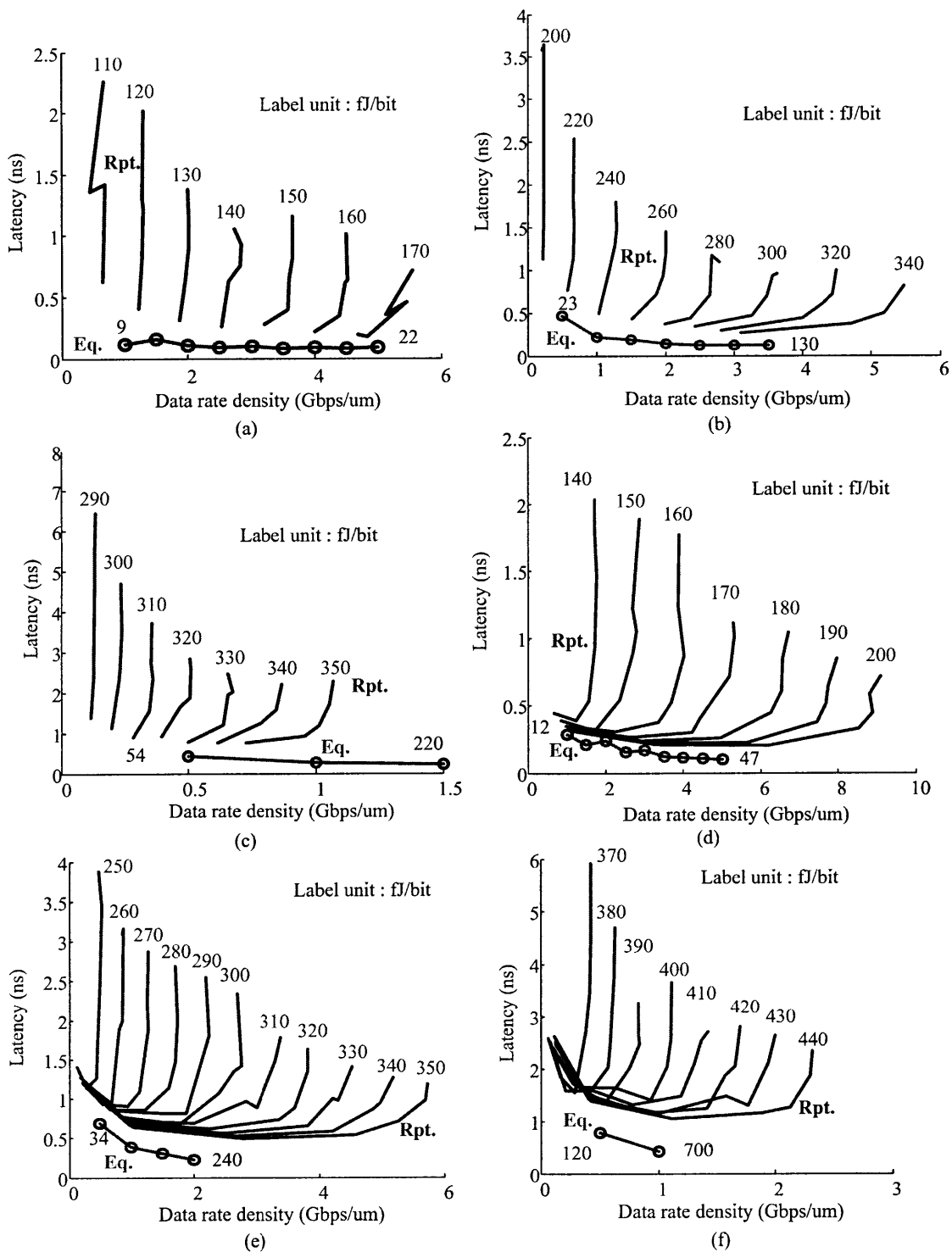


Figure 2-27: Trade-off contours of repeated interconnect and equalized interconnects over M9-5 mm (a), M9-10 mm (b), M9-15 mm (c), M6-5mm (d), M6-10mm (e), and M6-15mm (f) wires.

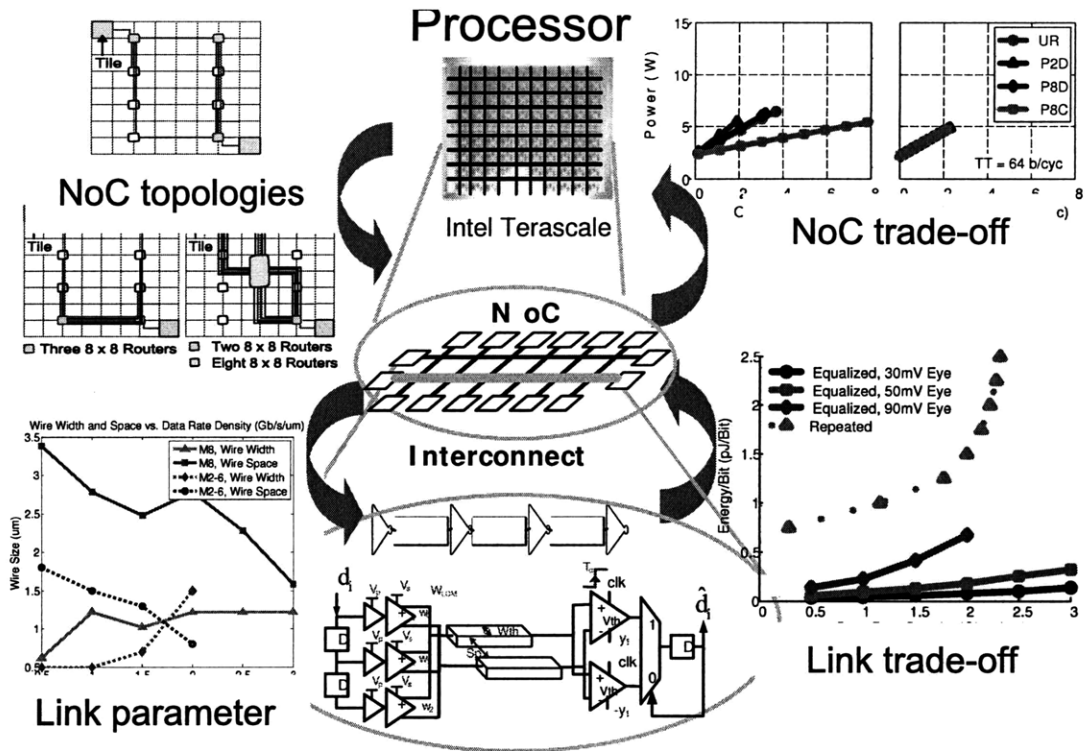


Figure 2-28: Connection of the link simulation and NoC simulation flow.

Network topologies

For our case study, we consider a 64-tile system designed using 32 nm technology, operating at 5 GHz and having an area of 400 mm^2 . The proposed analysis is independent of the exact nature of the tile. Each tile could be heterogeneous consisting of one or more logic cores and a part of the on-chip cache, or the tiles could be homogeneous having either only logic cores or only memory blocks. Irrespective of the individual tile architecture, these multi-tile systems will require an on-chip network that uses message passing, request-response or some other protocol for communication between the various tiles. We adopt a message passing protocol for our analysis. For our analysis, we consider systems with ideal throughput per tile (TT) of 64 b/cyc and 128 b/cyc under uniform random traffic pattern. Figure 1-1 shows the 4 different network topologies mesh, concentrated mesh (Cmesh), modified flattened butterfly (flatFly) and Clos, that we will be analyzing in this Section.

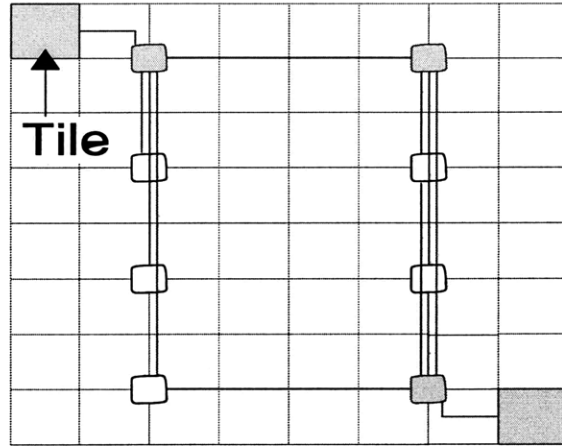
Figure 1-1(a) shows a 2D 8×8 mesh network. This network uses a distributed flow control and is commonly used in today's multicore designs [3, 4] for its ease of implementation.

However, the mesh network has a high average hop count resulting in high latency. For every hop, energy is consumed in the routers and wires. As the core count increases, this energy could become significant, specially for global traffic patterns. In addition, it is difficult to map both local and global traffic patterns to a mesh network such that they have uniform latency and throughput. Therefore, this non-uniform latency and throughput reduce the programmer's productivity.

The hop latency could be reduced by moving to higher dimensional networks. This would improve the network performance, but these high-dimensional networks need high-radix routers and long channels, when mapped to a 2D layout. These high-radix routers and long channels consume higher energy and area. Another way to lower hop count without too much overhead is by using concentration [7]. Figure 1-1 (b) shows an example of a mesh with a concentration of 4. Here, a lower router and a lower channel count balance with the higher router radices and wire lengths, in turn providing lower latency than mesh at comparable area and energy. However, like in the mesh network case, it is difficult to uniformly map the various applications to a Cmesh network.

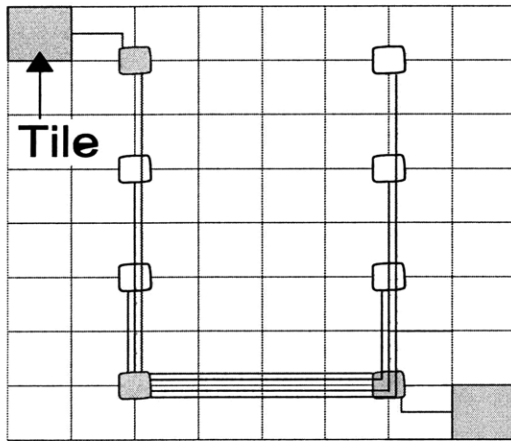
To provide low latency and high throughput, lowdiameter networks like flatFly [8, 9] (Figure 1-1 (c)) and Clos [10] (Figure 1-1 (d)) could be used. However, both these networks require high-radix routers and long point-to-point channels, which can increase the energy and area cost. The flatFly in Figure 1-1 (c) is a variation of a 8-ary 2-fly butterfly and has 8 tiles connected to each high-radix requires a maximum of two hops (intra-cluster and inter-cluster) for communication. Figure 2-29 (a) shows a possible layout of a flatFly network. The flatFly network, however, provides limited path diversity resulting in network congestion. In addition, like the mesh and Cmesh, a uniform mapping of various applications is difficult.

The Clos network provides an improvement over the flatFly by providing larger path diversity, while maintaining a hop count of 2. Figure 1-1 (d) shows a 8-ary 3-stage Clos network, where there 8 possible path between each pair of tiles. This path diversity can be used to minimize congestion in the network. Figure 2-29 (b) and (c) show two possible mappings of the Clos network to a 2D layout [41]. In the layout in Figure 2-29 (b) the three routers in a single column in Figure 1-1 (c) are clustered together. On the other hand, for the layout in Figure 2-29 (c) the intermediate set of routers are placed at the center of the chip. The first layout requires wires of 2 different lengths, while the second layout



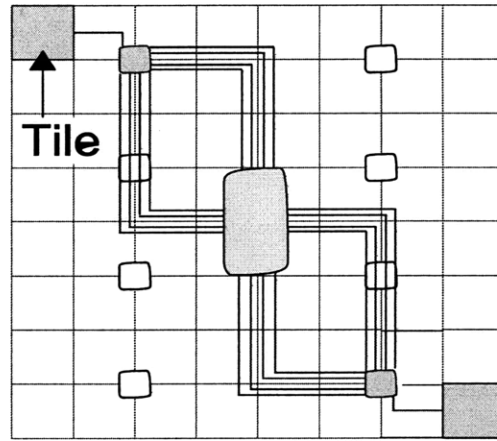
■ One 12 x 12 Router

(a) flatFly layout



■ Three 8 x 8 Routers

(b) Clos layout 1



■ Two 8 x 8 Routers

□ Eight 8 x 8 Routers

(c) Clos layout 2

Figure 2-29: Physical layouts of flatFly and Clos networks. Only a subset of channels is shown in each layout.

requires wires of 5 different lengths. From a power perspective, the layout in Figure 2-29 (c) is better (20% lower power), and therefore we use that layout for our analysis. In the Clos network, the data always has to travel through the intermediate set of routers, which results in uniform latency and throughput across various traffic patterns.

Evaluation

We compare the performance and power of mesh, Cmesh, flatFly and Clos networks using repeater-inserted interconnects and equalized interconnects. A 64-tile system is modeled and simulated using a cycle-accurate microarchitectural simulator. For our analysis, we considered synthetic traffic patterns based on partitioned application model [41]. The entire set of tiles is divided into partitions and tiles communicate only with the other tiles in the same partition. Depending on the mapping of these logical partitions to the actual physical layout, the tiles in a partition could be co-located or distributed across the die. A uniform random (UR) traffic pattern corresponds to a single partition case. A P8C traffic pattern divides the tiles into 8 groups with the tiles within a partition being co-located. The P8D partition traffic pattern too consists of 8 partitions and the cores are striped across the chip. In case of the P2D traffic pattern, the tiles are located in the diagonally opposite quadrants of the chip. We use the Booksim [42] simulator to simulate these topologies. The simulator models router pipeline latencies, router contention, credit-based flow control and serialization overheads. Warmup, measure and drain phases of several thousand cycles are used to accurately determine the average latency at a given injection rate.

Throughput per tile (b/cyc)	Channel width (b)			
	Mesh	CMesh	FlatFly	Clos
64	128	128x2	128x2	64
128	256	256x2	256x2	256

Table 2.7: Channel widths for various system types and topologies. For CMesh and FlatFly we use two parallel networks.

The channel widths in Table 2.7 for the various networks calculated using the bisection bandwidth criteria are chosen such that the peak network throughputs for all topologies under uniform random traffic were the same. For Cmesh and flatFly, instead of using a single network, we used two parallel networks with half the calculated channel widths. This is required as in some cases the calculated channel widths were evaluated to be larger than the message size. These two networks are therefore referred to as the CmeshX2 and flatFlyX2. The mesh, CmeshX2 and flatFlyX2 use dimension-ordered routing, while Clos uses randomized oblivious routing where the intermediate router is randomly chosen. All four topologies have credit-based backpressure [42]. For configurations with no virtual channels (VCs), each flit experiences a 2-cycle latency within the router’s first cycle for

arbitration and the second cycle for router crossbar traversal. The route computation is done only for the head flit. For the configurations with VCs, the head flit has a latency of four cycles, one each for route computation, virtual-channel allocation, switch allocation, and switch traversal, while the remaining body flits have a latency of two cycles, the first for switch allocation, and the second for switch traversal. The latency of the channel is dependent on the topology and its physical layout. A message passing interface is adopted and each message size is assumed to be 512 bits. We assume that the input buffer for each port of the router can store 4 messages. The following events - channel utilization and switch traversal - are counted while simulating each traffic pattern on each topology. These event counts are then used for calculating power dissipation. While calculating power, we considered both M6 and M9. Both M6 and M9 showed similar trends in power savings through equalization and VCs. Here, we present the results for M9. We consider two types of configurations of networks with no VCs and networks with 4 VCs.

Networks without virtual channels

Figure 2-30 shows the latency versus offered bandwidth plot for the four NoCs, running different traffic patterns. The tested NoCs are 64-tile Mesh, CMesh, FlatFly, and Clos. Here we consider the two types of system listed in Table 2.7. For the mesh network (Figure 2-30 (a)), out of the four traffic patterns, the UR and P8D traffic patterns have comparable saturation throughput as the source and destination pairs are distributed across the chip. In the case of the P2D traffic pattern, all communication paths are between diagonally opposite quadrants of the chip, which increases contention among the network resources, thus reducing the saturation throughput. On the other hand, for the P8C traffic patterns all the paths are local, resulting in lower contention and higher saturation throughput. As we double the channel width ($TT = 64 \text{ b/cyc} \rightarrow TT = 128\text{b/cyc}$), there is a 50% increase in the saturation throughput. On an average, the cmeshX2 (Figure 2-30 (b)) network exhibits higher saturation throughput than the mesh network due to path diversity and it also has lower latency due to lower hop count. The flatFlyX2 (Figure 2-30 (c)) exhibits behavior similar to the mesh and CmeshX2 networks across various traffic patterns. The saturation throughputs for P2D, UR and P8D are comparable to the CmeshX2, but the saturation throughput for the P8C traffic pattern is much higher as none of the router-to-router channels are required for communication. The flatFly network, however, does provide

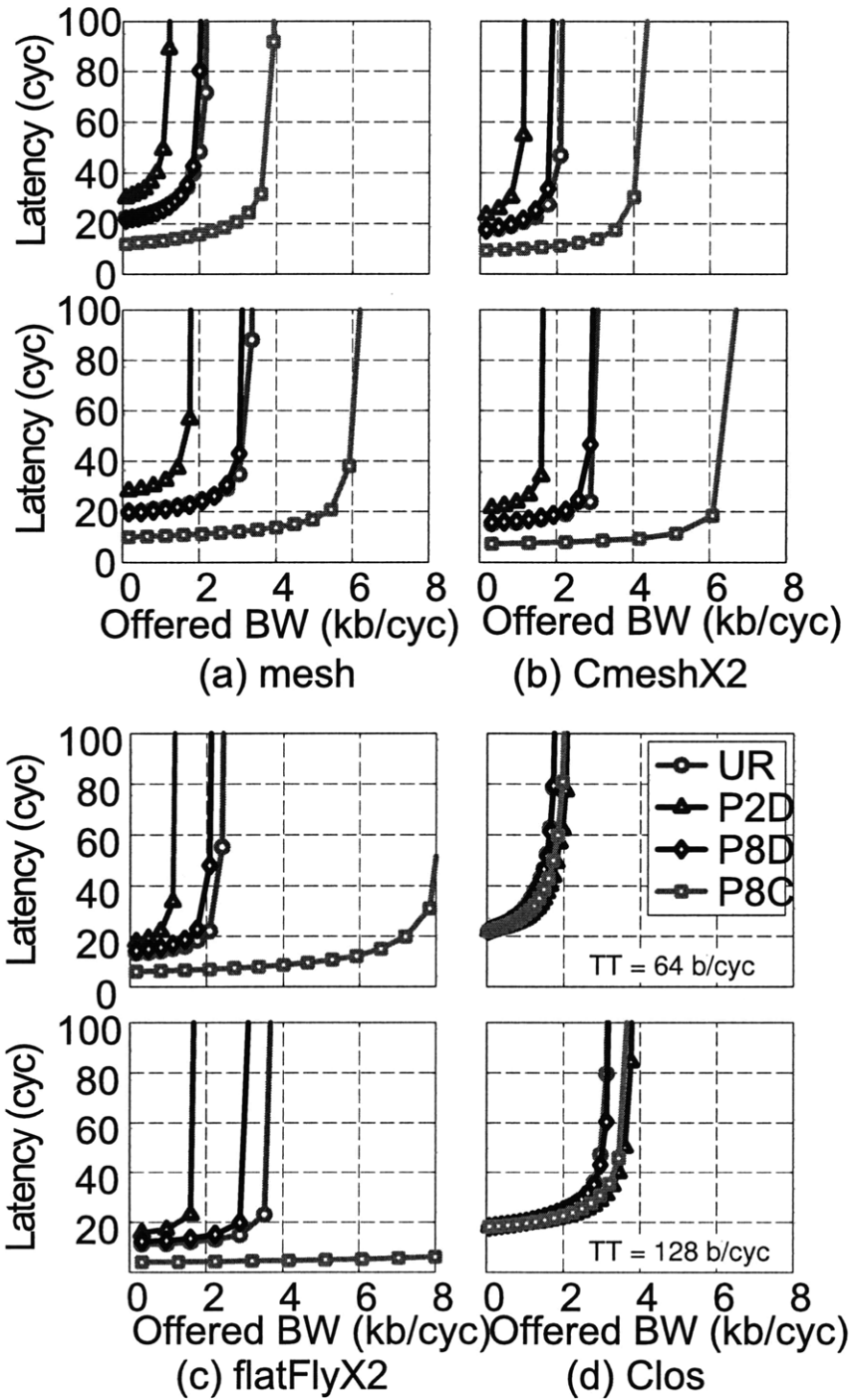


Figure 2-30: Latency versus offered bandwidth - no vertical channels. TT=throughput per tile (for that row).

lower average latency than mesh and Cmesh. The Clos (Figure 2-30 (d)) network exhibits a much more uniform latency and throughput across various traffic patterns as, irrespective of the traffic pattern, the flits always have to travel through an intermediate router. This uniform latency and throughput is helpful from a multicore programming perspective.

Figure 2-31 shows a plot of the power dissipation versus the offered bandwidth for the various topologies and traffic patterns. Here repeater-inserted wave-pipelined interconnects are used for router-to-router communication. The power dissipated in the interconnects is calculated using energy per bit numbers provided by the interconnect CAD tool described in this section, while the power dissipated in the routers is calculated using router models in [43]. The CmeshX2 has 4x less the number of routers and channels. Hence, even if the channels are wider (2x) and router radix is higher (1.6x), CmeshX2 consumes lower power at comparable throughput. For a given topology, going from $TT = 64$ b/cyc to $TT = 128$ b/cyc systems increase the power dissipation. At saturation, the flatFlyX2 network consumes power comparable to the mesh and CmeshX2 at their respective saturations for the UR, P2D and P8D traffic patterns. In the case of the P8C traffic pattern, the power dissipation is lower in flatFlyX2, as none of the global channels are used and power is dissipated only in the routers. In the case of the Clos network, the power consumed for various traffic patterns is almost the same and is comparable to that of the UR/P8D in the mesh network.

Interconnect equalization is beneficial in the flatFlyX2 and Clos networks where we have long global channels. Figure 2-32 shows the power versus bandwidth plots for flatFlyX2 and Clos networks. At low offered bandwidth, the power consumption is dominated by the fixed energy components (clock, leakage, etc) in the interconnects. As described earlier, the power consumed in repeater-inserted and equalized interconnects is comparable at low offered bandwidths. Since the power consumed in the routers would be the same, the power consumed in the repeater-inserted design is comparable to that in the equalized-interconnect design at low offered bandwidth. As offered bandwidth increases, the data-dependent component starts to dominate and we observe an average of 2x the lower power in the equalized-interconnect design at saturation. Though the data-dependent energy in the repeater-inserted interconnects is more than 2x the data dependent energy in the equalized interconnects, we do not see a greater reduction in power dissipation because of the fixed channel and router energy cost.

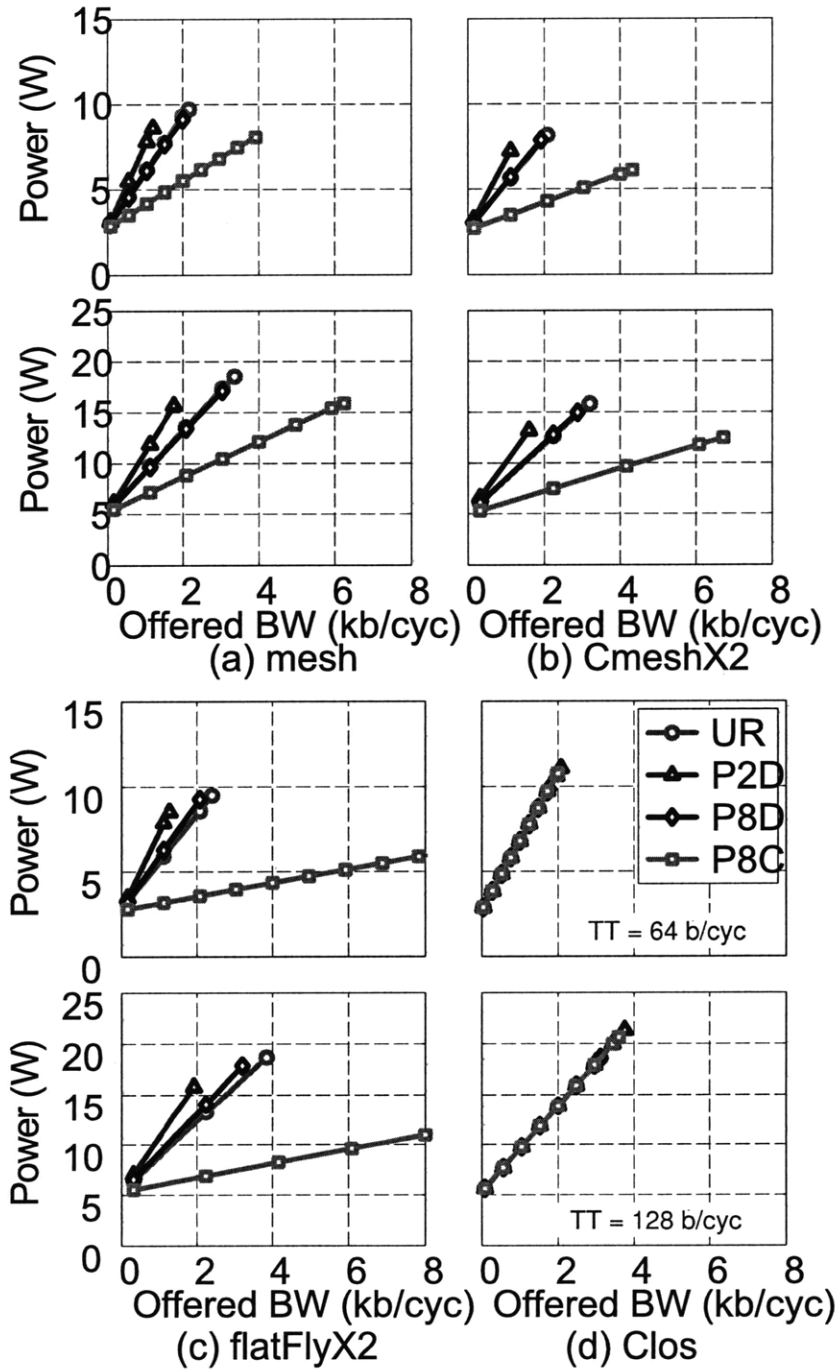


Figure 2-31: Power vs. offered bandwidth. interconnects are designed using repeater insertion, no VCs, TT = Throughput per tile (for that row).

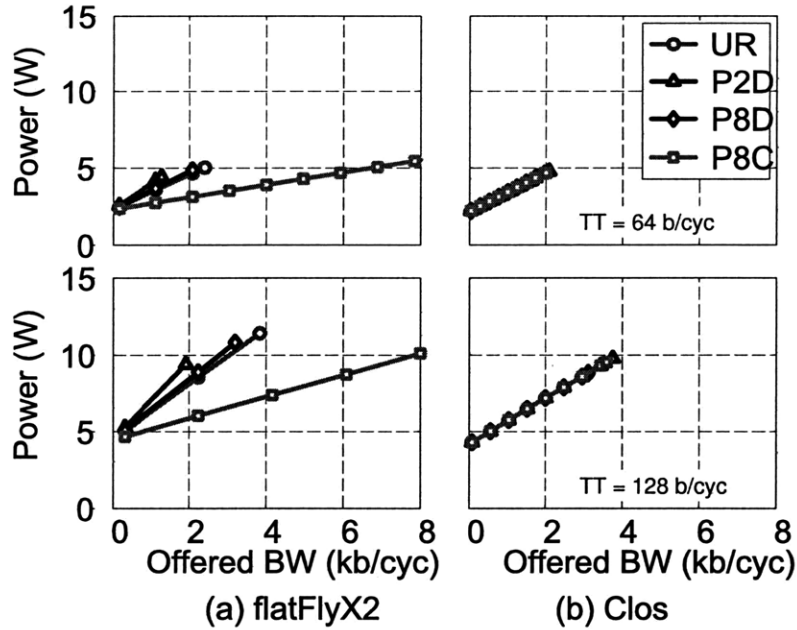


Figure 2-32: Power versus offered bandwidth. Interconnects are designed using equalization, No VCs, TT = Throughput per tile (for that row).

Networks with virtual channels

Virtual channels [42] can be used to improve the performance of all four topologies. Figure 2-33 shows the latency versus bandwidth plots for the four topologies with TT = 64 b/cyc with four VCs. While implementing VCs, the total size of the input buffer (in bits) per port is maintained to be equal to the no VC case. The crossbar for both routers is assumed to have the same size. For the mesh, CmeshX2 and flatFlyX2 networks, 1.52x improvement in the saturation throughput is observed by using 4 VCs. On the other hand, for the Clos network the improvement in the saturation throughput is minimal because of the inherent path diversity in the topology. An interesting result of using VCs is that a system with TT = 64 b/cyc with 4 VCs roughly matches the saturation throughput of a system with TT = 128 b/cyc with no VCs. There is minimal change in the latency when VCs are used due to increase in the router latency and credit-loop latency.

Figure 2-34 shows the power versus offered bandwidth plots for systems with TT = 64 b/cyc and with 4 VCs. At comparable throughput, the system with TT = 64 b/cyc and 4 VCs consumes 25-50% lower power than the corresponding system with TT = 128 b/cyc and no VCs. This is because the overhead due to VCs is lower than the energy savings due

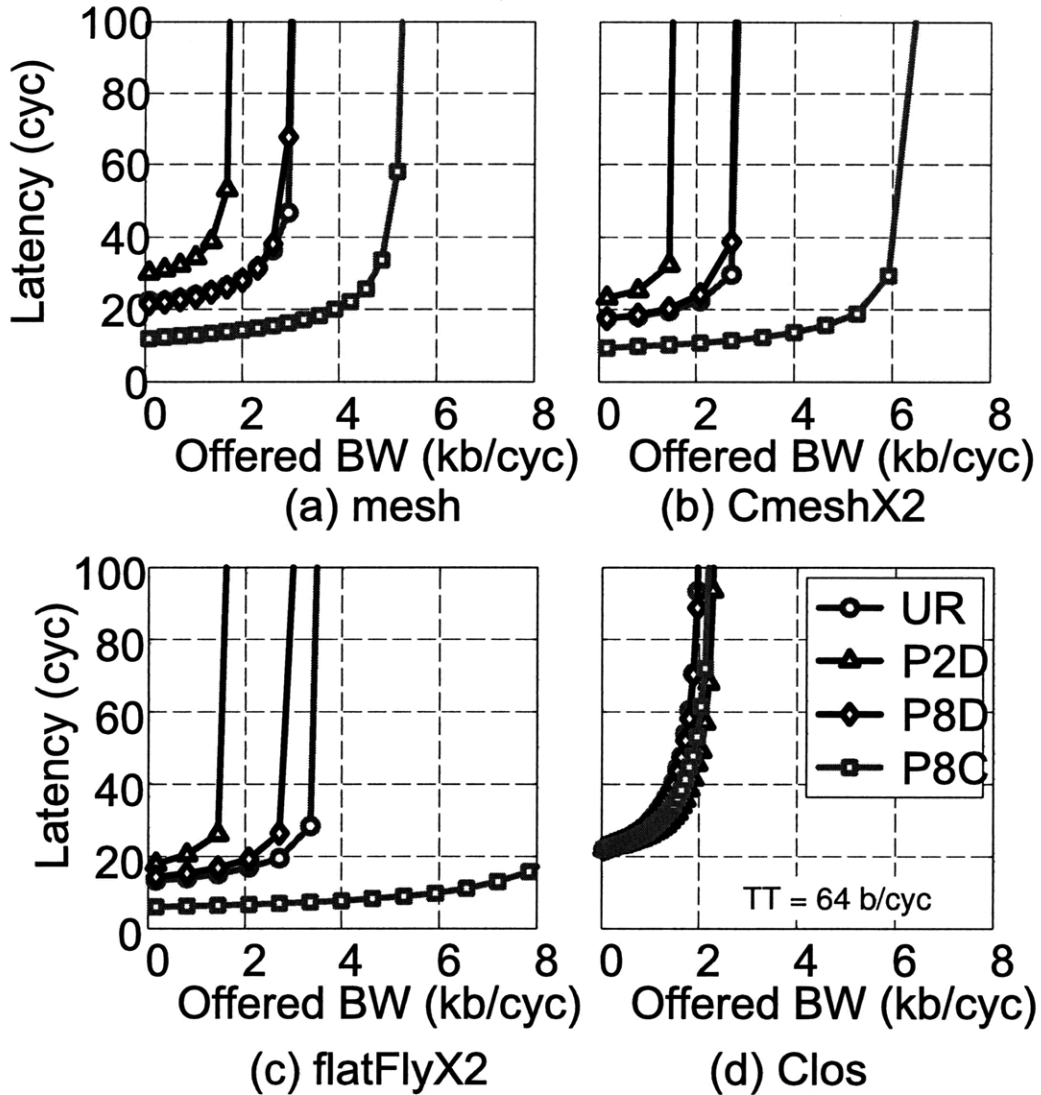


Figure 2-33: Latency vs. offered bandwidth- 4 VCs per router, TT = Throughput per tile (for that row).

to narrower channel widths and smaller crossbar in the router. A similar saving in power consumption can be observed when equalized interconnects are used (See Figure 2-32 and Figure 2-35).

Overall, compared to a flatFlyX2(clos) with TT = 128 b/cyc with no VCs and repeater-inserted wave-pipelined interconnects, a system with TT = 64 b/cyc, 4 VCs and equalized interconnects consumes more than 2-3x(2x) lower power at comparable throughput. In addition, since the system with TT = 64 b/cyc has 2x narrower channels, a 2x savings in the network wire area can be obtained. If we compare a mesh or CmeshX2 network designed

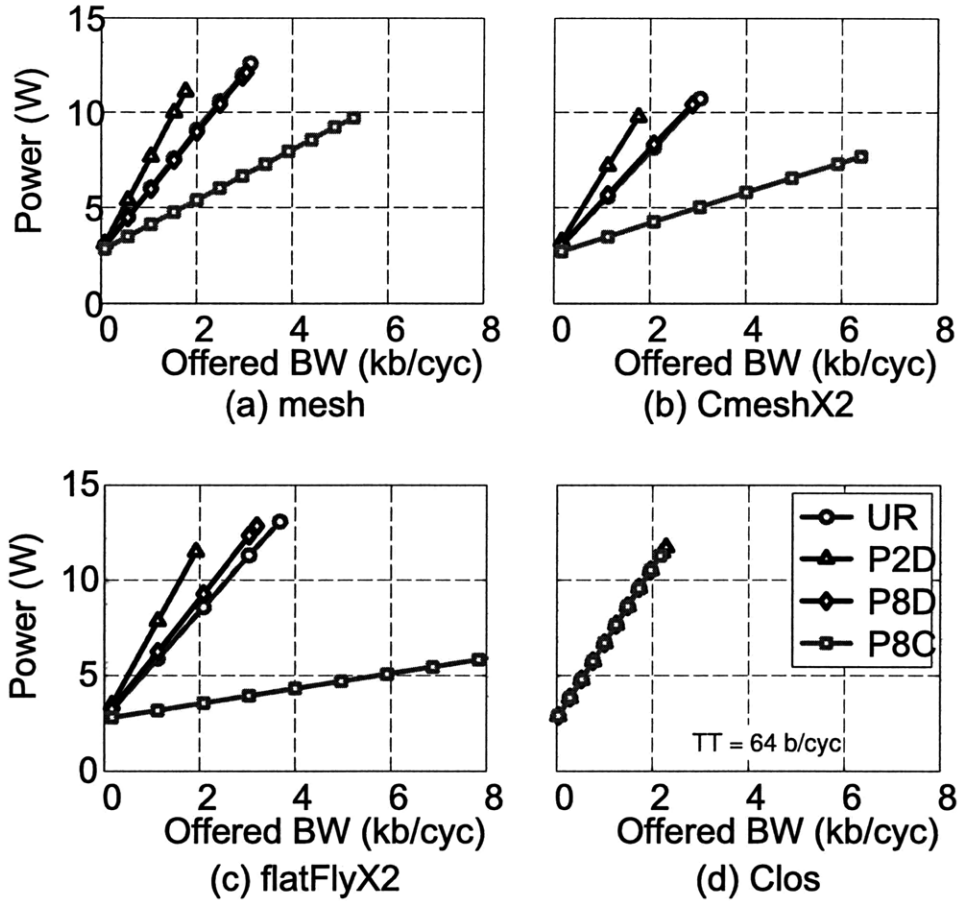


Figure 2-34: Power vs. offered bandwidth. Interconnects are designed using repeater insertion, 4 VCs per router, TT = Throughput per tile (for that row).

using repeater insertion to a flatFly designed using equalized interconnects and VCs, then flatFly consumes more than 3x lower power and 2x lower area at comparable throughput. The Clos network cannot match the saturation throughputs of mesh/CmeshX2 for local traffic patterns, but for global traffic patterns, the Clos network can match the throughput, while consuming more than 3x lower power and 2x lower area. In addition, Clos network provides uniform latency and throughput across various traffic patterns.

2.6 Summary

In this chapter, the first analytical model for an equalizing link over an RC-dominant channel is developed and explained. The model is based on the mathematical formulation that ties together the channel model, the driver model, the equalization algorithms, and

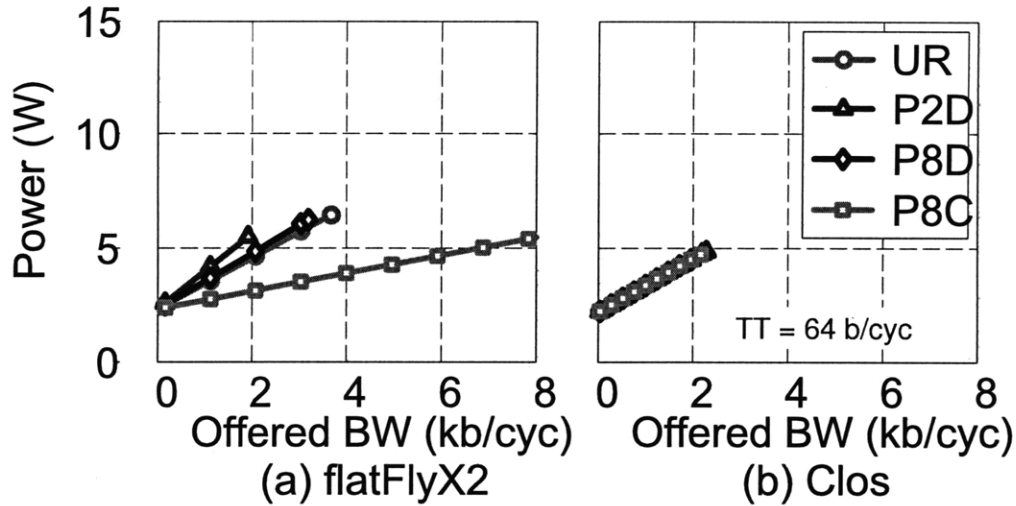


Figure 2-35: Power vs. offered bandwidth - Interconnects are designed using equalization, 4 VCs per router, TT = Throughput per tile (for that row).

the power consumption model. The channel model is derived from a lossy transmission line model and solution of the telegrapher's equation. The transfer function formula with termination impedance guides the designer toward a proper termination strategy in driver and receiver design. The driver model including the power consumption and sensitivity is mathematically explained. According to the model, the proposed CI FFE driver architecture is twice as power efficient as the conventional driver, and is ten times less sensitive to the coefficient error. Based on this model, the fast computation algorithm for the equalization coefficient which improves the computation speed by two hundred times is suggested. An example CAD tool for an LCM-based equalizing link is explained and demonstrated. Using this tool, repeater-based interconnects and equalization-based interconnects in 32nm are compared, and the results show that the equalized interconnects are about 2-10x more energy-efficient than the repeated interconnects at the link level and 2-3x more efficient at the NoCs level.

Chapter 3

Circuit Design

In earlier on-chip link designs, designers used pulse width pre-emphasis to reduce the power and complexity overhead in equalization circuits [18, 19]. However, the high activity factor and narrow pulse width significantly reduced the power efficiency. Additionally, the lack of signal shaping freedom in pulse width modulation limited equalization quality and achievable data rates. Later, improved power efficiency was demonstrated, using capacitive peaking equalization, but with limited throughput of only 2 Gb/s/ch (1 Gb/s/ μm) [21, 22].

In this chapter, based on on-chip link design insight from the previous chapter, we report a pre-distorted charge-injection (CI) FFE transmitter and a trans-impedance-amplifier receiver, which enable data rate increase and further improve both the energy and area efficiency. The CI FFE transmitter eliminates the power wasted in analog subtraction of a conventional FFE, by using digitally pre-computed signaling currents [23, 24, 32, 33, 35, 44]. A full 3-tap FFE implementation enables strong equalization on lossy channels and increase in data rates up to 6 Gb/s/ch (3 Gb/s/ μm). The CI FFE also significantly relieves the relative accuracy requirement for each FFE coefficient. In addition, digital pre-distortion of FFE coefficients allows the use of power-efficient nonlinear drivers. At the receiver, a trans-impedance amplifier (TIA) provides small termination impedance while suppressing the static current [25]. The small termination impedance provides wide bandwidth and large current amplitude, which is mapped to large voltage amplitude after TIA current-voltage conversion.

The rest of this chapter is organized as follows. Section 3.1 gives an overview of the link architecture. Section 3.2 explains the mechanisms of charge-injection and pre-distortion in

this design as well as the micro-architecture and implementation of the transmitter. Section 3.3 describes the advantages of the TIA over purely-resistive termination at receiver, as well as receiver micro-architecture and circuit implementation. Section 3.4 describes the chip layout. Section 3.5 shows the measurement result of the test chip and Section 3.6 summarizes this chapter.

3.1 Link Design Overview

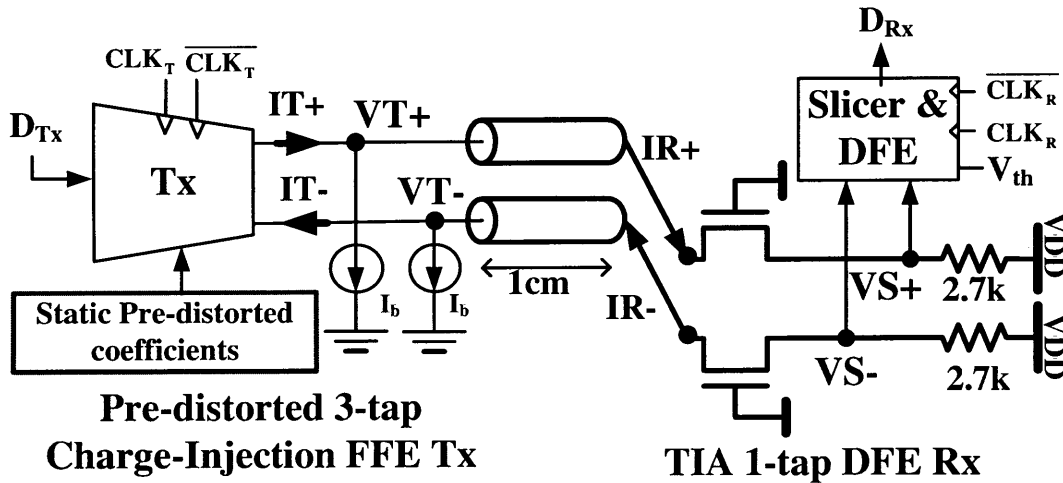


Figure 3-1: A link overview

Figure 3-1 shows the block diagram of the proposed link. The transmitter and receiver are connected through a 10 mm long differential on-chip wire. The receiver is terminated with a TIA. Two current sources attached at the transmitter provide bias current I_b for the TIA through the wire. The bias current I_b and the TIA together set proper common mode voltage levels of nodes V_T^+ , V_T^- , V_S^+ and V_S^- .

On data transmission, the transmitter computes and injects pre-emphasis current I_T^+ and I_T^- into the wire. The pre-emphasis current can be programmed by pre-distorted FFE coefficients. The TIA at the receiver converts the arriving current I_R^+ and I_R^- into voltage V_S^+ and V_S^- , respectively, sampled by the decision feedback equalizer (DFE) module. The DFE extends the data rate by compensating the higher channel loss and mismatches from desired exponential impulse-response roll-off. It has a loop-unrolled architecture [45] with threshold control knobs to match and eliminate one post cursor ISI tap while determining

the received data D_{Rx} .

3.2 Charge Injection Feed Forward Equalization Transmitter

In this section, the circuit implementation of a CI FFE transmitter in the test chip is explained. The circuit described in this section is designed based on the simulation in Section 2.3.2 and Section 2.3.4.

3.2.1 3-tap CI FFE Implementation

Figure 3-2 describes the overall architecture of the 3-tap CI FFE transmitter. A latch-pipelined, double-data-rate (DDR) digital decoding block generates switching signals for driver segments. The driver consists of weak and strong segments to appropriately pull up and down non-transient (I_0) and transient (I_1, I_2) currents, respectively. As explained in Chapter 2, this 3-tap CI FFE is equivalent to a typical 3-tap CS FFE by the mapping in Table 2.1. This 3-tap FFE transmitter provides stronger equalization ability than edge pre-emphasis in [46]. In [46], a digital logic circuit detects data transition and generates a narrow peaking pulse at the data edge with a strong driver while the weak driver provides the non-transient amplitude. This scheme can save the current wasted in analog subtraction too. However, since the peaking pre-emphasis is much narrower than a bit time, the high-frequency compensation is weak due to large channel attenuation. Therefore, this edge-preemphasis scheme is less effective than a 2-tap FFE equalization scheme. In our design, the tap count is three and each peaking pulse is one bit-time-wide, so it is more effective than [46].

The weak driver conducts small current I_0 to set the desired eye opening at the receiver. Although only 10% of the relative accuracy is required to bound the eye change by I_0 error within 10%, the absolute accuracy is high because the nominal value of I_0 is small (about $60\mu\text{A}$). Therefore, we use a current switch for the weak driver as shown in Figure 3-2 (b). The tail current source is adjusted to $2I_0$ instead of I_0 by current mirror because the weak segment only pulls down. Therefore, the current switch provides 0 or $-2I_0$ current into the channel to mimic the operation of $\pm I_0$ current. Combined with the bias current I_b , these two schemes are equivalent.

The design of the strong driver focuses on power-efficient current delivery since the

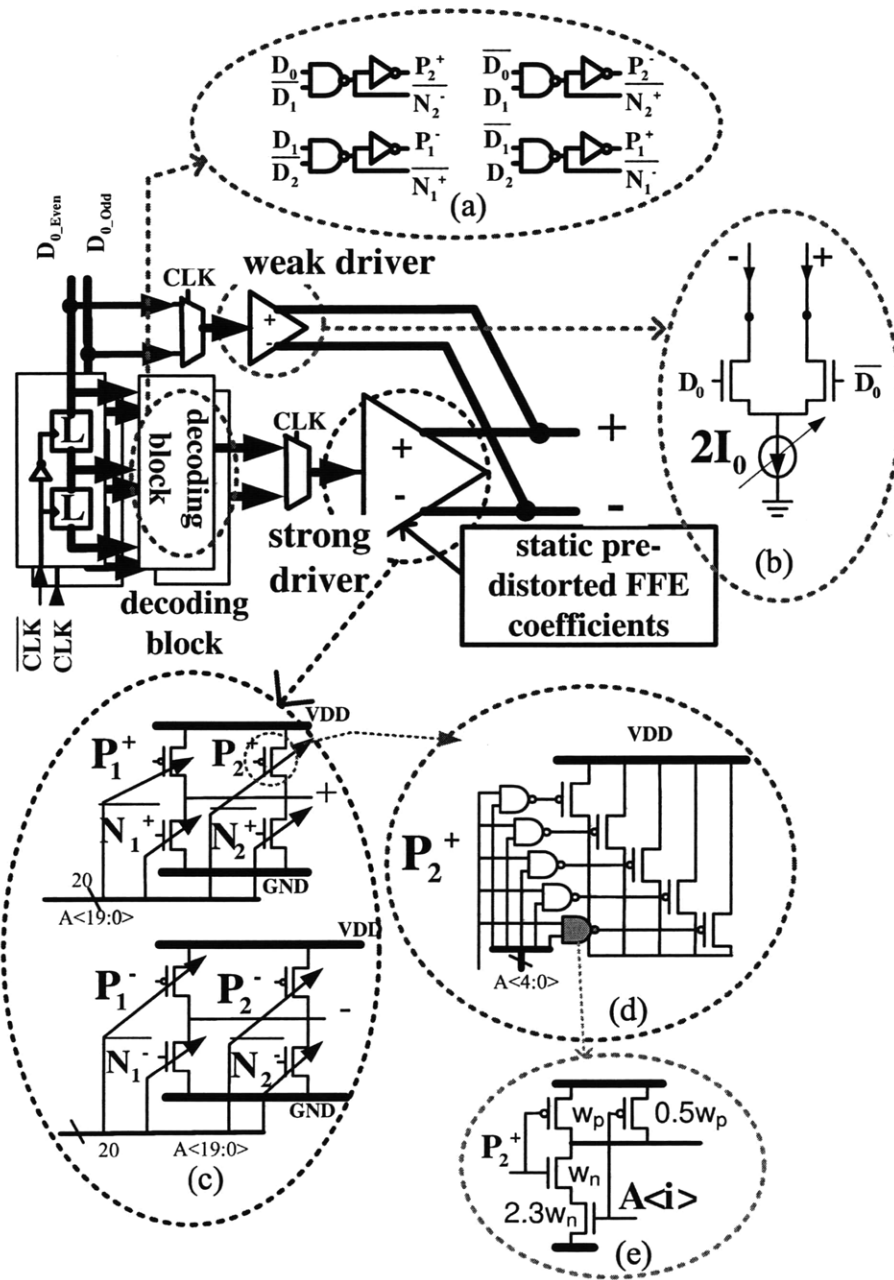


Figure 3-2: CI FFE implementation:(a) decoding block,(b) weak driver circuit, (c) strong driver circuit, (d) P2 DAC transistor, (d) skewed NAND gate.

amplitude of the transient current is large and the accuracy requirements for I_1 and I_2 currents are more relaxed as discussed in Chapter 2. The strong segment consists of four 5-bit digital-to-analog converter (DAC) transistors (P_1 , N_1 , P_2 , and N_2) for each differential terminal as illustrated in Figure 3-2 (c). P_1 and N_1 generate I_1 , and P_2 and N_2 generate I_2 . The maximum sizes of each DAC transistors are adjusted for the I_1 and I_2 currents. The 5-bit accuracy on I_1 and I_2 theoretically bounds the received eye error to less than 10%, because of the channel attenuation. This 5-bit accuracy is slightly overdesigned for testing purposes. In the test, explained in the later section, only 4 bits are used. Strong segment pull-up is necessary to keep a proper common mode voltage level for the driver because of the pull-down receiver TIA bias current. Without strong driver pull-up, the common mode voltage becomes too low almost turning the driver off. Each DAC transistor is an array of binary weighted transistors with enable signal as shown in Figure 3-2 (d). To achieve the proper least significant bit (LSB), the minimum size transistor of N_1 is stacked. However, due to the relaxed accuracies of I_1 and I_2 currents and the non-linearity compensation that will be explained in Section 3.2.2, the accuracy and linearity of DAC transistors are achieved. With DAC transistor gate nodes driven rail-to-rail, this topology delivers the maximum transient current for a given parasitic capacitance, achieving good power efficiency. For example, for the same transistor area, the current switch topology like a weak driver delivers about five to eight times smaller current than this strong segment due to smaller gate overdrive voltage required to keep the tail transistor in saturation. The enabling NAND gate in Figure 11 (e) is skewed for fast response to signal input (P_2), improving the pre-driver energy efficiency. The enable PMOS is only half the size of the signal PMOS minimizing the loading on the signal path while being strong enough to keep the voltage at V_{dd} when disabled. Similarly, an array of NOR gates enables the array of N_1 and N_2 transistor DACs. In a similar manner, the NOR gates are also skewed to achieve high-speed operation for the signal paths. By using skewed sizes, the NAND and NOR gates achieve performance power efficiency slightly worse than inverters with area overhead.

Figure 3-2 (a) shows a simplified circuit implementation of the decoding block. This decoding block is an implementation of the current source selection logic of Table 2.1. Compared to the CS FFE, this decoding block is a design overhead. However, as shown in Figure 3-2 (a), the logic gates do not take too much area and power providing efficient implementation of a 3-tap CI FFE. Since the transmitter compensates nonlinear error by

statically tuning the CI FFE coefficients (i.e. strengths of driver segments) as explained in Subsection 3.2.2, the high-speed decoder logic does not carry any coefficient information and can be implemented with very simple logic gates.

However, the inverter-like strong driver is nonlinear due to output impedance change. The sources of the nonlinearity are 1) data-dependent switching of driver segments with different impedances (from bit-time to bit-time) and 2) impedance fluctuation by output voltage change in a strong driver segment (within a bit-time). For example, in the simulation in Figure 2-14, the output impedance is set by the current source of the weak driver while the transmitter current is I_0 , but the output impedance becomes small and a function of the drain voltage of P_2 when the P_2 transistor is conducting I_2 current. This causes nonlinear behavior of the transmitter that introduces additional signal degradation and is hard to model with linear link equalization performance analysis tools, and hence causes the difference between small signal simulation in Figure 2-7 and the transient simulation in Figure 2-14. However, this nonlinearity can be compensated by static pre-distortion of CI FFE coefficients which will be explained in Subsection 3.2.2.

3.2.2 Nonlinearity and Pre-distortion

In a 3-tap CI FFE, three consecutive bits select the proper current source and the selected I_T^+ deterministically changes V_T^+ . Therefore, each current I_T^+ value has the unique selection of current source and the voltage profile. Table 2.1 summarizes how three consecutive bits determine I_T^+ value and V_T^+ voltage change during a bit time, and Figure 2-14 shows an example of isolated ‘1’ case. The magnitude of nonlinear error is determined by the three consecutive bits, and a digital compensation must cover all eight cases generated by the three binary combinations, in order to fully compensate the nonlinearity. By allowing a small nonlinearity error in $\pm(I_0 + I_1 + I_2)$ case, we can reduce the cost of the compensation block to cover only six cases.

Figure 3-3 is a voltage-transition state diagram for nonlinearity compensation constructed from Table 2.1. The state is represented by two consecutive bits D_0D_{-1} , indicating the transmitter output voltage. Each arrow shows a state transition and current source selected for a new outgoing bit. The two state bits and a new outgoing bit determine the proper I_T^+ value and thus the voltage transition. For example, when the transmitter is sending consecutive ‘0’s as shown in the beginning of the simulation in Figure 2-14, the

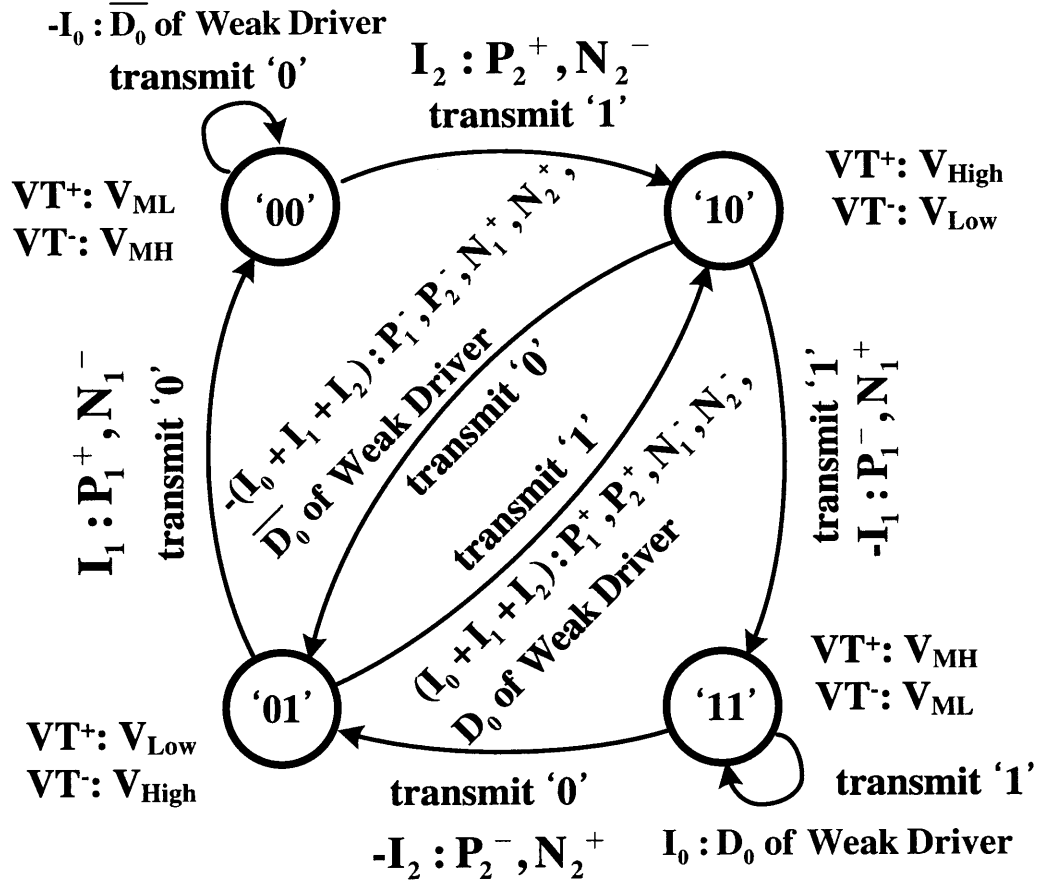


Figure 3-3: State transition diagram for non-linearity compensation. The voltage is associated with the state ' D_0D_{-1} .' The state transition defines proper selection of current source and the non-linearity effect due to voltage change. .

state and V_T^+ stay at '00' and middle low level (V_{ML}), respectively, by steadily conducting $-I_0$ current via weak driver. As the transmitter starts sending the isolated '1' bit, the transmitter turns on P_2^+ (and N_2^- for other differential terminal) DAC transistor to conduct I_2 current, changing the state from '00' to '10' along with V_T^+ voltage change from V_{ML} to V_{High} . The V_T^+ voltage change in this transition weakens the P_2^+ DAC's current, causing current error on I_2 . In the next cycle in Figure 2-14, the state changes from '10' to '01' by turning on all the transmitter segments - the weak driver, N_1^+ , and N_2^+ transistors (P_1^- and P_2^- for the other differential terminal) to conduct $-(I_0 + I_1 + I_2)$. This current also suffers from the nonlinearity error.

According to this diagram, except for two transitions ('10' \rightarrow '01' and '01' \rightarrow '10'), each device has unique voltage profile and thus unique amount of non-linearity error. Therefore,

we can compensate the nonlinear error by statically tuning the size of each device. For example, except in two cases, the weak driver only turns on when the output voltage is V_{ML} or V_{MH} . The difference between V_{ML} and V_{MH} is very small since they are set by small I_0 current. Since the voltage level is in the middle of the supply level, the current source of the weak driver operates in saturation and thus the current error is negligible. When P_2^+ transistor turns on during the transition from ‘00’ to ‘10’, V_T^+ voltage changing from V_{ML} to V_{High} decreases I_2 by a constant amount. Therefore, static adjustment on P_2^+ strength is enough to compensate this non-linear error. During the transition from ‘10’ to ‘01,’ the voltage changes from V_{High} to V_{Low} by conducting a current through the weak driver, N_1^+ , and N_2^+ (P_1^- and P_2^- for the other differential terminal). In this transition, N_1^+ transistor is stronger than in ‘10’ \rightarrow ‘11’ transition because the drain voltage at the end of the transition is V_{MH} , which is higher than V_{Low} in ‘10’ \rightarrow ‘01’ transition. N_2^+ transistor, on the other hand, is weaker during this transition than in ‘11’ \rightarrow ‘01’ transition because the start-transition voltage V_{MH} is lower than V_{High} in ‘10’ \rightarrow ‘01’ transition. In this case, the errors on I_1 and I_2 have opposite polarities, mostly cancelling each other. Note that I_0 current is too small to add significant error in this case.

Partitioning of drive segments in CI FFE allows compact and hardware-efficient static pre-distortion, which is not possible in other analog FFEs (CML, CS, and VD). In CS FFE, three current sources work together to generate all 8 current values as listed in Table 2.1. As a result, each current source is turned on all the time and experiences all cases of voltage changes. Since the nonlinear error is associated with voltage change due to the voltage-dependent impedance change, each current source has more than two distinct values of nonlinear error, preventing static compensation. For example, the pull-down w_2 current source in Table 2.1 is connected to ‘+’ node when $D_0D_{-1}D_{-2}$ is ‘110’, ‘100’, ‘010’, or ‘000’. These four patterns cause four distinct V_T^+ voltage transitions, respectively: $V_{High} \rightarrow V_{MH}$, $V_{ML} \rightarrow V_{High}$, $V_{High} \rightarrow V_{Low}$, and $V_{ML} \rightarrow V_{ML}$. Therefore, four different coefficients are necessary for w_2 since the non-linear error can have four distinct values for each case. The hardware implementation is much more difficult since the pre-distortion requires memory to store four different values of each coefficient, and a decoding block must select and assign the right coefficient value within a bit time.

3.3 Trans-impedance Amplifier Receiver

Further optimizing the signal transfer across the channel, the receiver is terminated with a TIA to leverage the benefits of both the voltage mode (VM) and current mode (CM) receivers. The transfer function and the static power consumption of the overall system significantly depend on the receiver input impedance as discussed in Subsection 2.2.4. In this section, we explain the receiver circuit implementation.

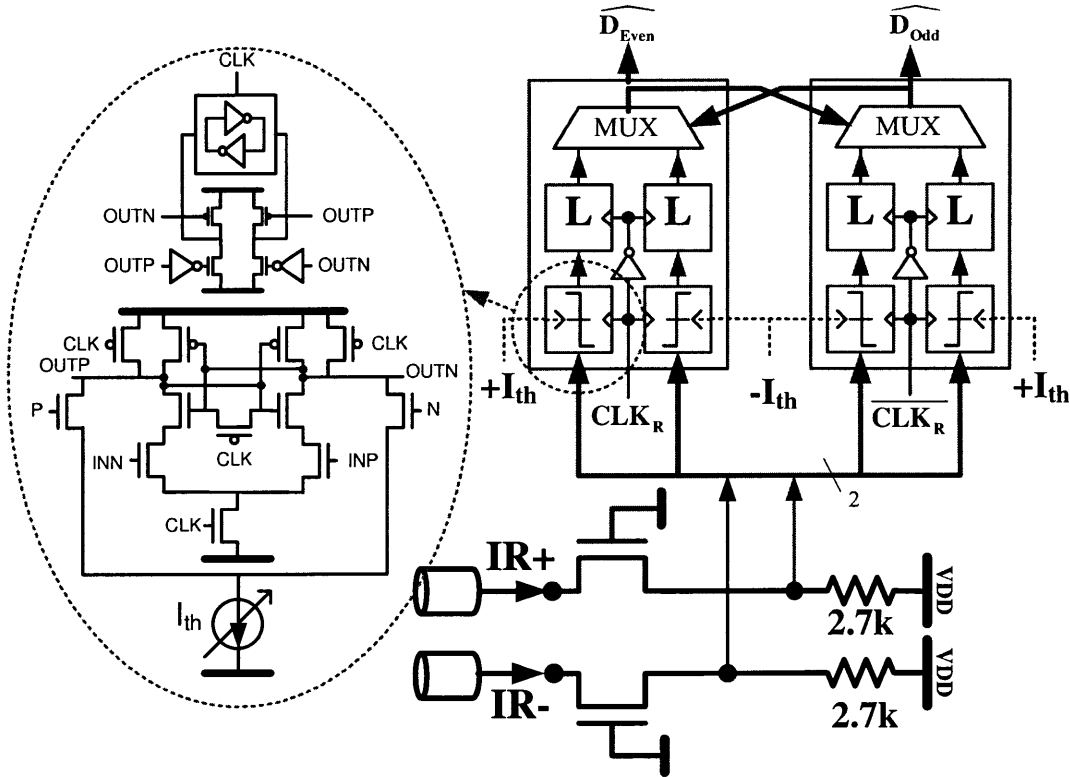


Figure 3-4: Receiver circuit.

Figure 3-4 describes the receiver circuits. The front-end TIA amplifies input current and converts it into voltage. TIA's output voltage is connected to a latch-based DDR loop-unrolling DFE [45, 47, 48] that decides the value of the received bit.

3.3.1 Trans-impedance Amplifier

The TIA is implemented as a simple common gate amplifier as shown in Figure 3-4 since this TIA topology is simple and reliable enough to be implemented with small area cost.

The DC bias current is provided from the transmitter through the wire as shown in Figure 3-1. This bias current determines the TIA's common mode voltage level as well as the small signal input impedance. The bias current is determined considering the wire's DC resistance, supply voltage level, the desired TIA's small signal input impedance, the voltage drop of the TIA's gain resistor, and the strong segment's desired common mode voltage level. The resistor is a silicide-blocked poly resistor which is widely used in modern technology. With a silicide blocked resistor, the area and parasitic capacitance are affordable to implement the TIA. The sizing is based on the trade-off analysis in Subsection 2.2.4. The transistor size is optimized for the best signal amplitude at Nyquist frequency for a given bias current. Larger transistors can reduce the small signal input impedance and thus larger signal amplitude as discussed in Subsection 2.2.4. However, large transistors also increase parasitic capacitance which reduces the signal amplitude. Therefore, the sizing is based on the AC simulation at Nyquist frequency to maximize the received signal amplitude. According to these simulations, the TIA provides 3x larger signal amplitude at 2GHz with only 50% static power consumption for the same bandwidth as shown in Subsection 2.2.4.

3.3.2 Loop-unrolled Decision Feedback Amplifier

The TIA output voltage is connected to a DDR-style [49,50] loop-unrolled decision feedback equalizer (DFE). Figure 3-4 also shows the DFE architecture. In a DDR architecture, the DFE function is time-interleaved on every even/odd phase of the clock to reduce clock frequency and latency requirement, and eventually to improve energy efficiency. In this design, the maximum clock frequency is 3GHz, and thus the DDR architecture is necessary. Depending on the technology and the desired operation frequency, single data rate (SDR) scheme could be more power-area efficient. In this implementation latches are selected over flip-flops to save power and area. Since master-slave type flip-flops require twice area of the latches, latches are more power efficient in a typical high-speed digital design. In a loop-unrolled architecture, two even slicers generate two decision bits by adding or subtracting input-referred post cursor in speculation about the previous bit value: '1' or '0.' The following multiplexer (MUX) selects the right decision bit when the previous bit becomes available.

In this design, the selection signals of the MUXs are delayed by one additional differential-input latch stage to further relax latency requirement. Due to the nature of the regeneration

process of a sense-amplifier, the output amplitude depends on the input amplitude and the regeneration time. If the input amplitude becomes small due to noise, the output signal may not be fully regenerated within a bit time failing the MUX feedback in a normal loop-unrolled DFE. In this design, the additional latch helps fully regenerate the output of sense amplifier within a bit time. For this purpose, the latch is designed with differential input for good sensitivity. This additional regeneration ensures that the following MUX always takes rail-to-rail selection signal during operation. Therefore, this circuit topology works similar to the double regeneration slicers [51].

3.3.3 Slicers

Figure 3-4 also shows the slicer circuit. Modified StrongArm sense amplifiers [52] with additional offset compensation ports are used to add or subtract a post cursor to the TIA output, by setting the offset/threshold current. The threshold polarity is selected by two NMOS switches P and N. A tail current source attached to the output node of the sense amplifier controls the threshold voltage. When CLK is '0,' the nodes OUTP and OUTN are both pulled up by PMOSs while the differential NMOS pair are not working since the tail transistor is turned off. At this moment, the two pull-up transistors work as a linear resistors in triode-region. By conducting small threshold pull-down current I_{th} through the tail threshold transistor, we can add small voltage difference between OUTP and OUTN which causes differential initial voltage condition at the start of the regeneration process when CLK becomes '1.' During regeneration period (i.e. CLK='1'), the tail current of the differential NMOS pair turns on, starting regeneration. The initial voltage difference between OUTP and OUTN as well as continuous conducting threshold current I_{th} form a threshold for the input voltage INP and INN.

Although, this threshold adjustment works fine in this design in general, this threshold adjustment scheme is sensitive to the supply noise. Since the threshold current path is attached to only one output node, the supply noise only affect one output node degrading supply noise rejection. Since the signal amplitude is about 100 mV due to the channel attenuation, large supply noise can significantly degrade the performance. Potentially, offset adjustment circuit with higher supply noise rejection ratio can improve the receiver performance in a larger digital design like a CPU [53].

The SR latch attached to the sense amplifier keeps the previous bit while the sense

amplifier pre-charges nodes OOTP and OUTN when CLK is '0.' During this pre-charge period, both OOTP and OUTN charge up V_{dd} disconnecting the cross-coupled inverter pair. The cross-coupled inverters in the same latch hold the previous bits during this time. In regeneration period, one of the OOTP or OUTN becomes low voltage (although possibly not fully zero), flipping the voltages of the inverter pair. The cross-coupling connection path of the inverters is disconnected during this period to easily flip the data nodes.

3.4 Chip Fabrication

To explore the impact of equalization on efficiency of on-chip interconnects and test the pre-distorted CI FFE and TIA receiver concepts, a proof-of-concept chip in 90 nm bulk CMOS process has been fabricated and tested. The technology is an ASIC oriented process and the M8 metal layer is chosen for the 10-mm link design to emulate semi-global and global processor interconnects. On-chip test support blocks are built to enable direct, *in-situ* characterization of the link performance. Figure 3-5 shows the die photograph overlaid with a design layout to outline the regions of the transceiver and test-support blocks. A 10-mm wire channel is designed as a serpentine in a M8 layer covering most of the die area. The differential wire pair is selected among a bundle of eight wires to add the side-wall capacitance effect. The bottom layer M7 is filled with supply grid to emulate the dense wire environment. The top layer M9 is also filled with dummy metal to satisfy the metal density rules. However, the top layer was the smallest capacitance since distances to M7 and neighbor wires are much smaller than the distances to a M9 dummy layer. The areas of the core transmitter and the receiver are about $16 \mu\text{m} \times 70 \mu\text{m}$ and $16 \mu\text{m} \times 40 \mu\text{m}$, respectively. The test results show that the on-chip link successfully operates up to 6 Gb/s/ch (3 Gb/s/ μm) with energy cost of up to 0.635 pJ/b.

3.5 Experimental Data

3.5.1 Test Setup

This chip presents the first *in-situ* characterization setup for on-chip equalized links. A block diagram of the on-chip test-support circuits is illustrated in Figure 3-6. During test, two pattern generators at the transmitter side feed the transmitter with a desired

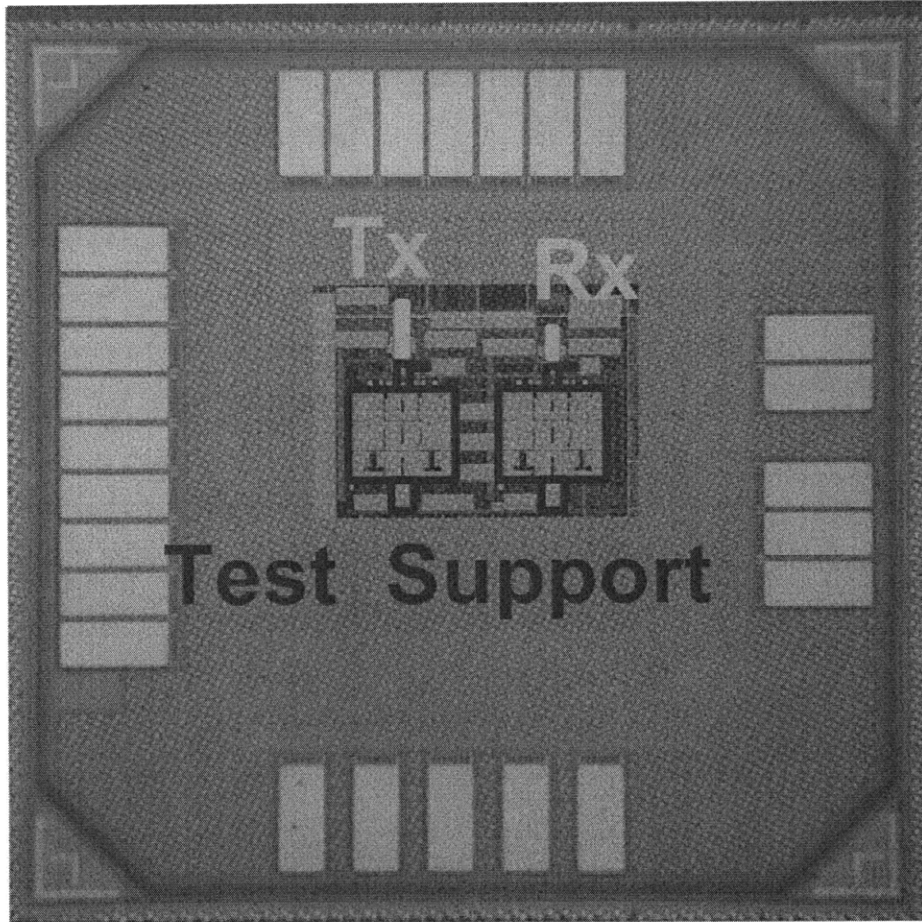


Figure 3-5: Die photo.

test bit sequence. Each pattern generator can be configured either as a 31-bit pseudo random bit sequence (PRBS) generator or a 32-bit pattern rotator through the scan chain. Two 36-bit snapshot units are attached to the pattern generators to record the part of the generated bit sequence. The snapshot units have two modes: track and hold. In a track mode, the snapshot unit works as a shift register at data rates to track the output sequence of the pattern generator. In a hold mode, the snapshot stops tracking and holds the sequence recorded so that the scan chain can read out the sequence at slow speed. By reading out the two snapshot units attached to the pattern generator, we can verify whether the pattern generators work fine or not and examine the delay in the link. The transmitter sends the generated pattern through the 10-mm differential wire under test. The received bit is determined by a DFE unit after the current-voltage conversion at the front-end TIA. The DFE unit can be configured as either a self-DFE or an error-propagation-

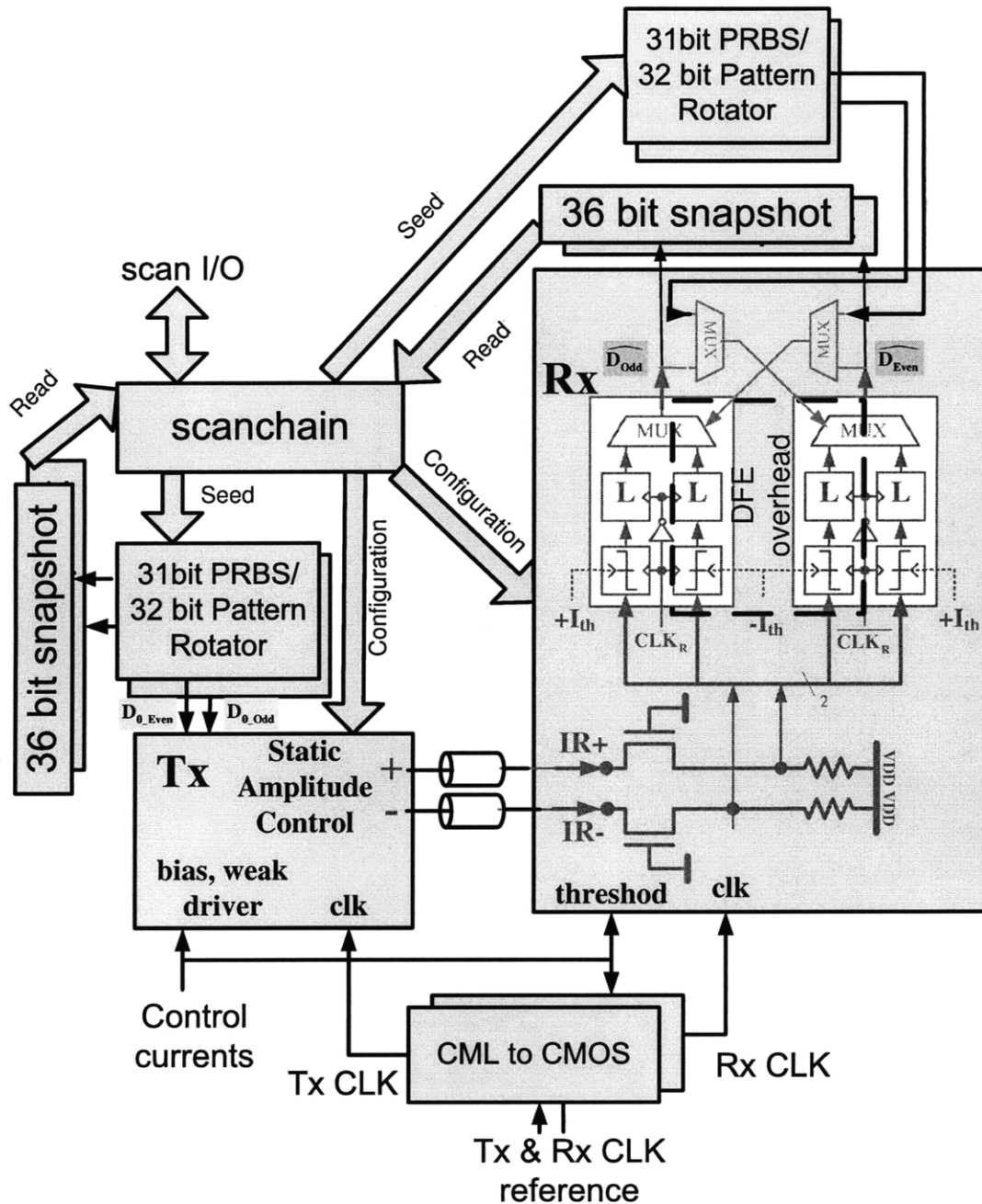


Figure 3-6: On-chip test support block diagram.

free monitoring circuit. In the self-DFE mode, the DFE unit works as a normal DFE circuit generating the decision bits from the slicer outputs. In the error-propagation-free monitoring mode, the decision feedback is fed by the two pattern generators instead of the DFE output. This scheme allows to monitor the front-end bit error rate without the

effect of the error propagation. In normal DFE operation, a decision error may affect the next bit decision through the decision feedback MUX once a decision error occurs. Therefore, a wrong decision can propagate through the bit cycle. This effect is called error propagation. However, error statics without error propagation are often more interesting than the ones with error propagation. For example, monitoring bit error rate without error propagation gives us the noise information at the front-end receiver. For this purpose, the error-propagation-free monitoring circuit always takes the correct sequence from the pattern generators for decision MUX as shown in Figure 3-6. Since the transmit pattern is known at the beginning of the test, the decision pattern can be programmed at the receiver's pattern generators with proper delay to feed the perfect decision bit sequence. Therefore, in this scheme, we can monitor bit error statics of the DFE circuit without error propagation. The output of the DFE unit is monitored by two 36-bit snapshot units. A comparison of the transmit and received snapshots at different transmitter and receiver clock phases and receiver threshold voltages generates the *in-situ* statistical eye diagram and channel pulse response as seen by the receiver.

To reduce cost of high-speed I/Os, all configurations are done through slow I/Os except the reference high-speed clocks. The control and data read/wright of the scan chains are done through the slow I/Os. Two synchronized reference clocks with adjustable phase are provided from an external signal generator. The analog bias currents are adjusted through slow I/Os too.

The scan chain programs the strong driver strength, mode selection, as well as the seed of the pattern generator at the transmitter side. At the receiver, the scan chain also configures the threshold polarities of the slicers. Analog configurations are all done through DC reference current inputs. The weak driver and bias currents of the transmitter, slicer thresholds at the receiver, are configured by external analog DC current reference, to allow testing flexibility and experiment with accuracy and dynamic range requirements. The test chip required this high-level of flexibility since it is designed to explore the power-performance trade-off for large range of channel losses and data-rates (2 Gb/s - 6 Gb/s). For practical application with narrower data-rate range, this configuration overhead could be significantly reduced.

3.5.2 Channel Measurement

Figure 3-7 shows the on-chip measured 64 symbol-time-period square pulse response and transfer function in current-driving and current-receiving mode ($T_{ii}(f)$) as described in Equation 2.24. During the measurement, only the weak segment drives the channel with a step digital pattern at 4 Gb/s: 32 consecutive ‘1’s followed by 32 consecutive ‘0’s. The pulse width is chosen to be large enough to mimic the step response. Only the weak segment is used as a driver during channel measurement since the strong segment has poor accuracy. As discussed in Subsection 2.3.4, the strong segment does not require high absolute accuracy for equalization.

For good channel measurement, the weak segment strength can be directly calibrated by measuring the TIA current at DC since the separate supply is used for the supply of the transceiver core for measurement. The received current is measured by sweeping the threshold current of the slicers and observing received digital bit patterns repetitively at the same timing position. Since the transmitter, the receiver, the pattern generator, and the snapshots are synchronized, the same phase position can be repetitively measured over many test runs. For example, with 2GHz clock and a DDR style architecture, the received sampling rate is 4Gsample/s. By adjusting the transmitter and receiver clock phase

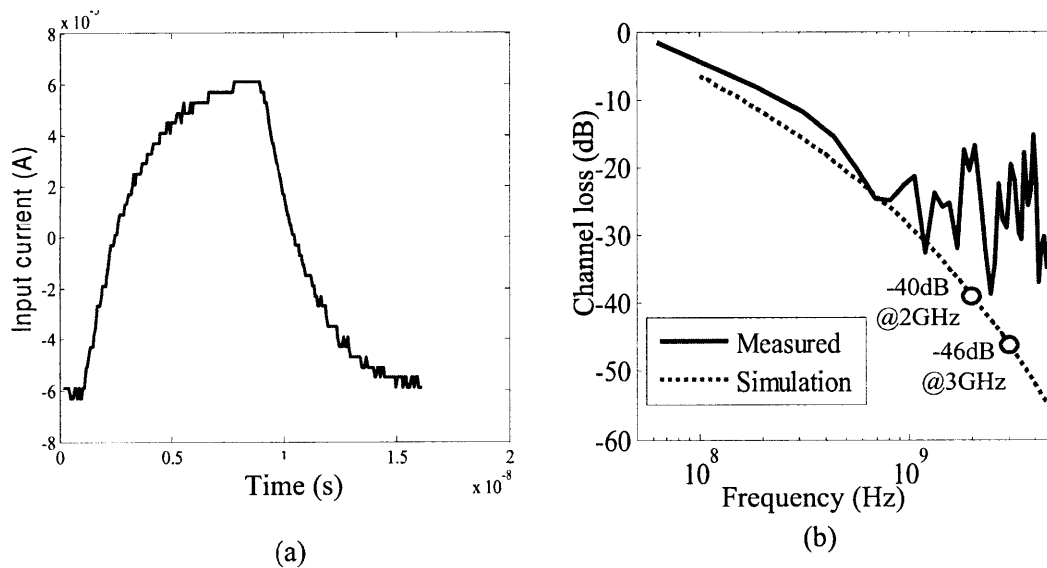


Figure 3-7: Measured (a)64 bit time period square pulse response and (b) transfer function. blue: measured; red: simulation.

difference, the sampling rate can be increased. The probabilities of ‘1’ and ‘0’ are recorded to determine the current level at each time point. The received current is determined by finding the threshold where the probability of bit ‘1’ becomes 0.5 over many test runs. The received current is four times over-sampled by adjusting receiver’s clock phase relative to transmitter’s clock in this measurement. The transfer function is generated by dividing the spectrum of the step response by the transmitted spectrum.

The long tail of the step response in Figure 3-7 (a) reveals significant ISI in unequalized channel. The measured 50% delay and 90% settling times are about 1.4 ns and 5.5 ns, respectively, or 8.6 and 33 bit times at 6 Gb/s/ch. In Figure 3-7 (b), the measured and simulated transfer functions are shown for comparison. The noise dominates the measured signal at high frequency due to large signal attenuation. The noise floor is about 20 dB lower than the weak-segment current magnitude I_0 used in this test indicating the feasibility of low bit error rates for binary transmission equalized to I_0 values at the receiver. This noise is overestimated in the measurement process because of: 1) the finite number of bit counts and 2) the spectrum shape of the square pulse. Since the signal level is achieved by finding the point where the probability of bit ‘1’ becomes 0.5, which is similar to dithering in Δ - Σ modulations. Due to the limited number of averages, the decision noise becomes shaped into the high frequency region similar to the a noise-shaping effect in Δ - Σ modulations. Furthermore, since the transfer function is driven from the transient response to the square pulse in Figure 3-7 (a), the high-frequency noise is amplified. Because the spectrum of the source sinc function (Fourier transform of the square pulse) has small amplitude at high frequencies, the high frequency noise is amplified in dividing the received spectrum by the transmitted sinc function. Therefore, both effects amplify the high-frequency noise. The channel transfer function measurement and simulation show reasonably good match within the measured frequency range. The difference comes from the modeling error such as ground plane approximation for top and bottom metal layers in Figure 2-3. The measured channel loss at 690 MHz is about 24.6 dB, implying much higher loss at 3 GHz (Nyquist frequency for 6 Gb/s/ch operation), which is 46 dB in simulation. This channel loss is significantly larger than the one in the previous equalized links [29,32] implying the superior equalization performance due to good sensitivity and robustness to the coefficient errors.

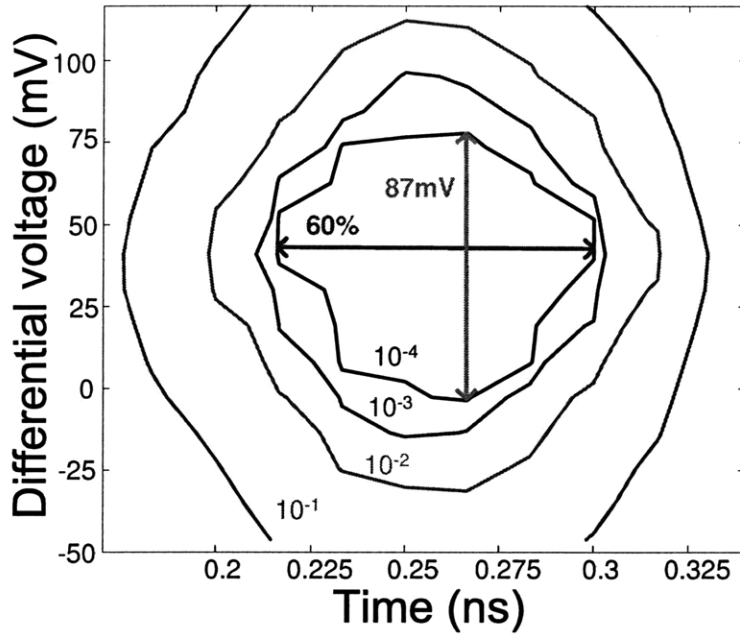


Figure 3-8: Measured eye diagram at 6Gb/s with 1.2V supply voltage and DFE enabled.

3.5.3 Eye Measurement

Figure 3-8, 3-9, and 3-10 present measured eye diagrams for various settings. To obtain power-performance trade-off for the same eye quality, the FFE coefficients are adjusted to achieve close to 100 mV vertical receiver eye. The eye diagram in Figure 3-8 is measured at 6 Gb/s with 1.2 V supply voltage. During the measurement, the DFE was fully functional. The eye was closed without DFE. The measured eye height is 87 mV after the TIA conversion and the eye width is 60% of the bit time. Considering the large channel loss (> 40dB), 60% eye width verifies the quality of the equalization.

Due to the scan-interface speed limitations, the probability of each of the voltage-time points on the eye diagram was collected from 10^4 transmissions. The good quality of horizontal eye opening (60% bit-time (UI)) in comparison with a typical bathtub curve in other literature [44] supports that the link would work at much lower bit error rate. In a similar measurement in [25], 50% UI horizontal eye at $BER < 10^{-4}$ was verified error free at the center of the eye up to 10^{-6} which was able to be measured within measurable testing time. The eye in Figure 3-9 is measured at 4 Gb/s with 1.1 V supply, with disabled DFE to save power. In a loop-unrolled architecture, the DFE overhead is half of the receiver

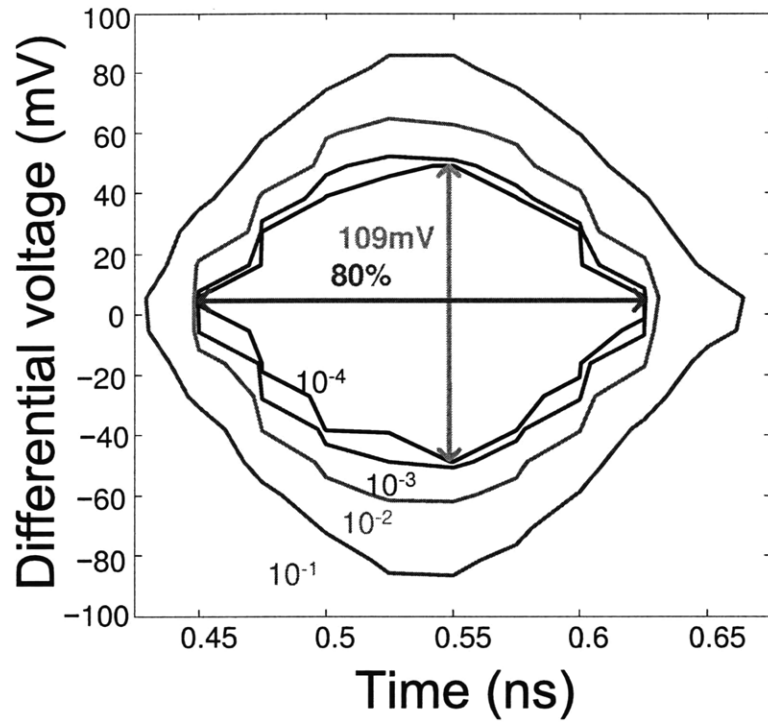


Figure 3-9: Measured eye diagram at 4Gb/s with 1.1V supply voltage and DFE disabled.

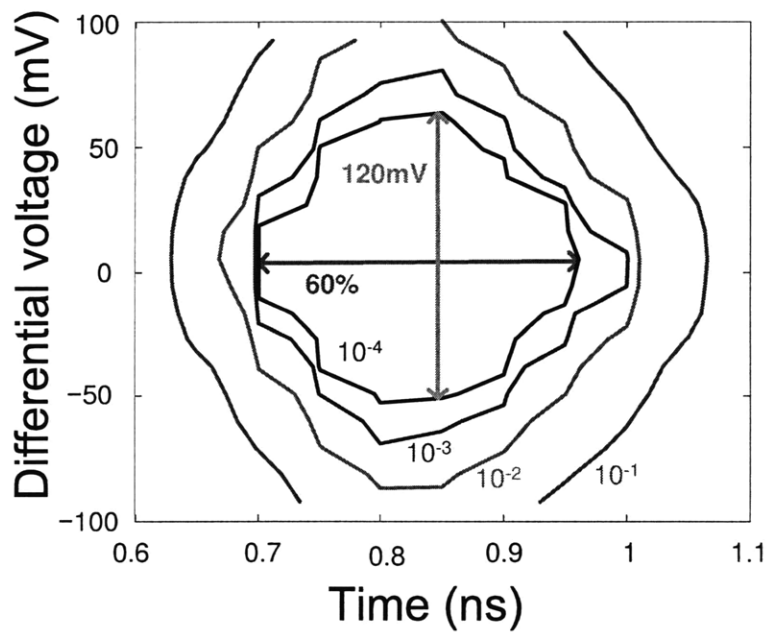


Figure 3-10: Measured eye diagram at 2Gb/s with 1.1V supply voltage and DFE disabled.

power. Therefore, if the DFE is not necessary, it is better to disable the DFE part. The measured vertical eye was 109 mV, and the horizontal eye was 80% UI (BER < 10⁻⁴). Considering the large channel loss, 80% UI is typically considered hardly achievable. The eye in Figure 3-10 is measured at 2 Gb/s with 1.1 V supply and disabled DFE. At 2 Gb/s, we also disabled one CI FFE tap (N_1 and P_1 transistor DACs) to demonstrate that further hardware cost reduction is possible at low data rate operation. The vertical eye is 120 mV and horizontal eye is 60% of the unit interval (UI). This eye size and the vertical eye could have been larger if N_1 and P_1 segments are enabled.

3.5.4 Eye Sensitivity Measurement

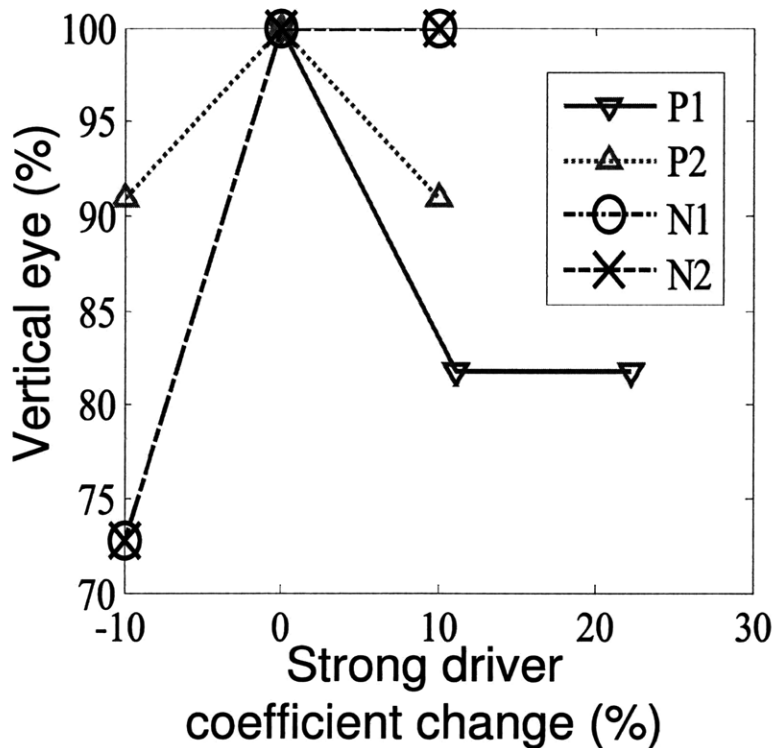


Figure 3-11: Vertical eye versus strong driver coefficient change at 6Gb/s with 1.2V supply voltage and DFE enabled. The nominal values of 5-bit strong driver coefficients are $P_1=9$, $P_2=10$, $N_1=10$, and $N_2=10$.

Figure 3-11, 3-12, and 3-13 show vertical eye versus perturbation of strong segment coefficient measured at 6 Gb/s, 4 Gb/s, and 2 Gb/s with 1.2V, 1.1V, and 1.1V supply, respectively. To capture the eye sensitivity to coefficient errors, coefficients are perturbed

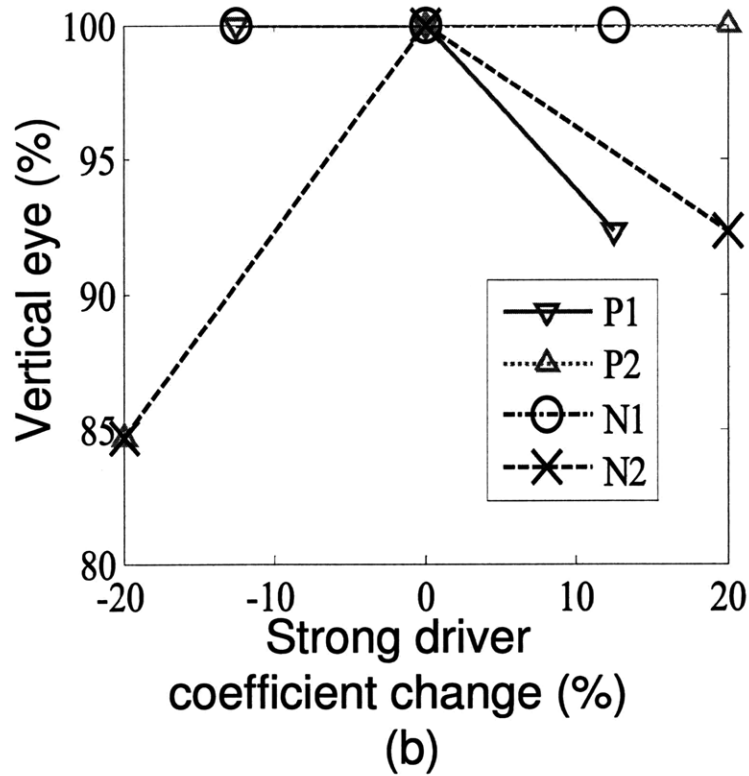


Figure 3-12: Vertical eye versus strong driver coefficient change at 4Gb/s with 1.1V supply voltage and DFE disabled. The nominal values of 5-bit strong driver coefficients are $P_1=9$, $P_2=5$, $N_1=9$, and $N_2=5$.

one at a time. To save measurement time, the eye-measurement statistics were taken down to 10^{-3} probability, which is enough to capture the errors due to coefficient perturbations.

Figure 3-11 confirms the small sensitivity of the eye to strong segment coefficients. At 6 Gb/s, the vertical eye changes by about 30% at most for 10% coefficient change giving us the eye sensitivity about 3. According to the Table 2.3, the eye sensitivity is slightly larger than 2. This small mismatch to the mathematical derivation is due to the approximation in the analysis, but the values are roughly correct within our range of interest. Figures 3-12 and 3-13 further illustrate higher sensitivity to I_2 (generated from P_2 and N_2) than I_1 (generated from P_1 and N_1), as discussed in Subsection 2.3.4. At 4 Gb/s, the peak sensitivity is about 16 for 20% coefficient change. At 2 Gb/s, the eye is not very sensitive to P_1 and N_1 showing that the channel can be equalized only with 2-taps. Since P_2 and N_2 is the main tap, eye still shows stronger dependency on P_2 and N_2 .

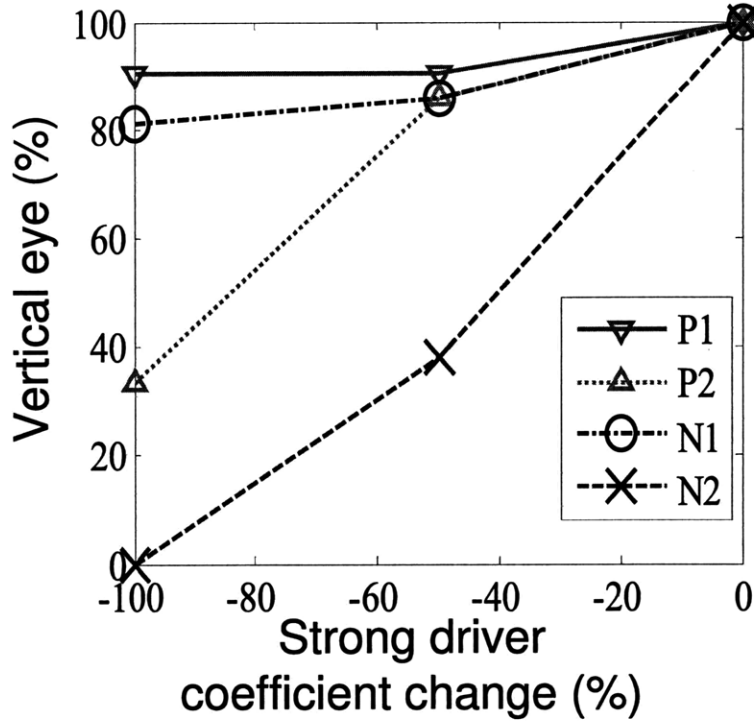


Figure 3-13: Vertical eye versus strong driver coefficient change at 2G/ps with 1.1V supply voltage and DFE disabled. The nominal values of 5-bit strong driver coefficients are $P_1=2$, $P_2=2$, $N_1=2$, and $N_2=2$.

3.5.5 Energy Measurement

Figure 3-14 presents the measured link energy/bit breakdown at different data rates, measured at the same conditions as in Figure 3-14. Detailed energy breakdown is obtained by measuring supply currents at different conditions such as Tx/Rx clocks, enabling/disabling strong driver, data pattern and etc.. The Rx energy is estimated from the current difference when the receiver clock is enabled and disabled. Therefore, the local receiver clock energy is also counted in the Rx energy. Since the DFE overhead hardware is identically the half of the receiver energy, we can simply compute DFE energy by dividing the receiver energy by two. Similarly, the transmitter energy is acquired, and the transmitter clock energy is counted in $TxOther$. The $TxStr$ is the energy difference when strong driver is enabled and disabled. The TIA energy is simply counted from the bias current setup in Figure 3-1. The only non-distinguishable current is the leakage current via dummy decoupling capacitors. The leakage current values are $72 \mu\bar{A}$, $120 \mu\bar{A}$, and $192 \mu\bar{A}$ at 1 V, 1.1 V, and 1.2 V, re-

spectively in simulation, and are subtracted from the measurements. However, the leakage is insignificant since it is less than 10% of the total current. The energy that cannot be contributed to any of the main blocks is shown as *Misc* energy. This portion of energy could be aggregated error during energy break down such as DC current of transmitter, receiver, leakage simulation error, and etc..

The measurements show that operation at 4 Gb/s with 1 V supply is the most energy efficient. For a random data transmission, the energy efficiency is relatively flat up to 4 Gb/s because DC energy, switching energy, and channel-related energy change differently as data rate increases. For example, the TIA draws DC current so its energy consumption per bit decreases as the data rate increases. The receiver energy-cost stays relatively flat up to 4 Gb/s following the CV^2 rule and doubles at 6 Gb/s due to activated DFE overhead. Transmitter energy cost, especially the strong driver energy, increases with data rate increase. Since the channel loss becomes larger at higher data rate, the driver must be sized

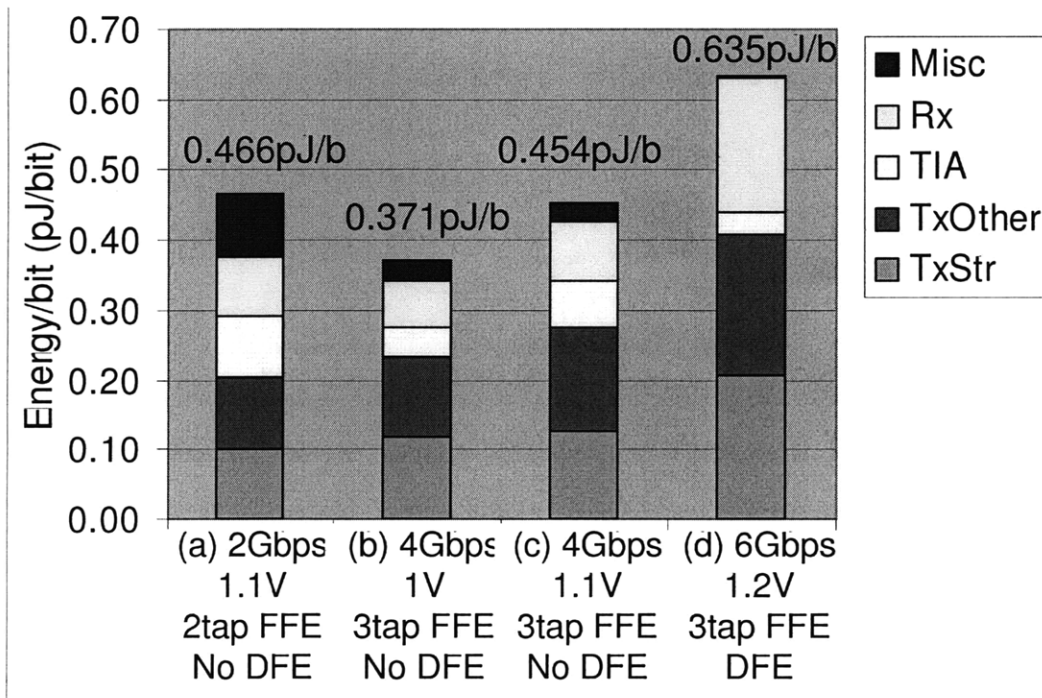


Figure 3-14: Measured energy breakdown at different data rates. *TxOhter*: Tx decoder and clock energy. *TxStr*: strong driver energy. *Rx*: sense amplifier and DFE logic energy. *TIA*: TIA bias energy. *Misc*: energy not included in above list. The decoupling capacitor's leakage currents were found by simulation ($72 \mu\bar{A}$, $120 \mu\bar{A}$, and $192 \mu\bar{A}$ at 1 V, 1.1 V, and 1.2 V, respectively) and subtracted from the measurements.

up to inject more energy into the channel and compensate the loss. For high performance, the measurement shows that increase in data rate from 4 Gb/s to 6 Gb/s requires approx 70% more transceiver energy. For lower and fixed data-rate target, the link might be further resized for lower energy cost. Note that at 4Gb/s target, the current link can be even more energy efficient than designed here, since the parasitic junction capacitance of the driver segments sized up for 6Gb/s resulting significant overhead.

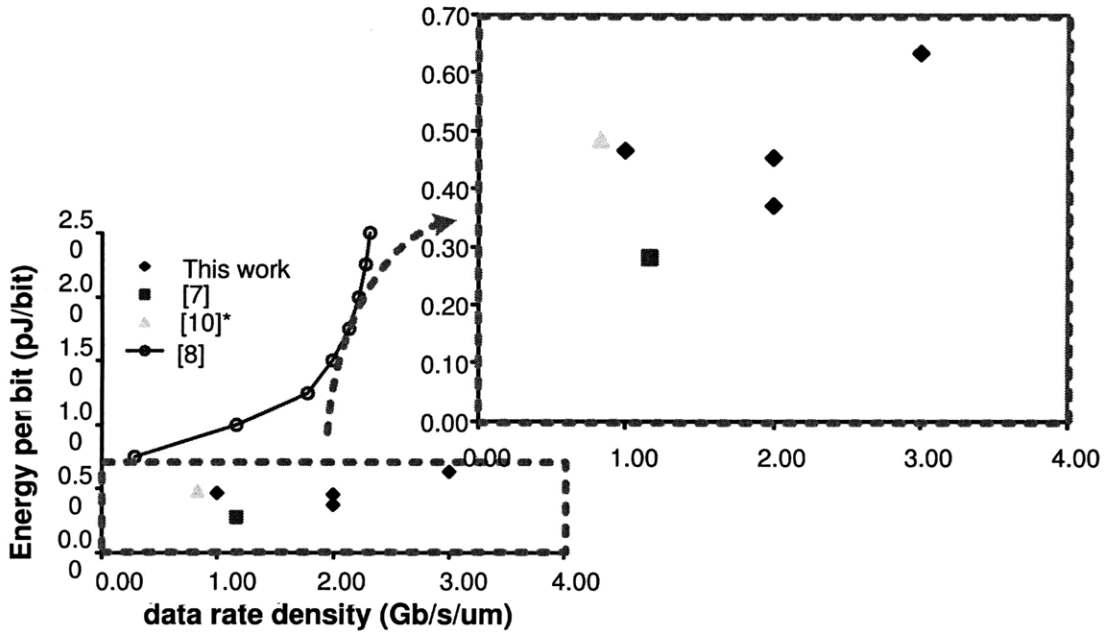


Figure 3-15: Comparison to the most relevant work. * 5mm link.

Figure 3-15 shows the energy cost versus data rate density plot compared to the most efficient previously reported designs [15,22] and repeated interconnect schemes [23] in 90-nm CMOS technology. The closest performance and efficiency is reported in [22] which uses a capacitive peaking pre-emphasis transmitter and a DFE-IIR receiving filter. The capacitive peaking provides pre-emphasis or equivalently modifies the transfer function of the channel [22]. However, the simple capacitive peaking could not provide enough equalization ability and therefore, the performance is limited. Compared to [22], the maximum achievable data-rate is improved by 3x to 3 Gb/s/ μm (6 Gb/s/ch) with up to 2x energy cost. In [15], multi-band of communication is used. Equalization is used in base-band and two RF carrier signals provides extended bandwidth. However, the on-chip's low pass filter characteristic attenuates RF signals too much. Therefore, in [15], wide-pitched wires are used to provide

large bandwidth. As a result the achieved data rate density is small as shown in Figure 3-15. The repeated interconnect power data rate density number is estimated from the modified formula for energy-performance equation [24] when the latency is designed in similar number of the equalized interconnect. Compared to the repeaters, Figure 3-15 shows that all three schemes ([15,22] and this thesis work) have better energy efficiency. Note that this thesis work is the only one that provides higher data rate density than [22] and the eye diagram *in situ*. The eye quality stays above 60% UI for all data rate scenarios (maximum 80% UI), which is larger than 44% UI in [22]. Compared to the estimated repeater [23] power consumption, the repeater has to burn about 4x more energy.

3.6 Summary

In this chapter, a pre-distorted charge-injection FFE transmitter and a TIA-terminated receiver are reported for RC-dominant on-chip interconnects. Charge-Injection FFE consumes 3x less power compared to the conventional voltage divider FFE architectures. Static pre-distortion technique utilizes a power-efficient non-linear driver for equalization to further improve the power efficiency. At the receiver end, a TIA-termination is implemented, simultaneously achieving wide bandwidth, high amplitude, and small static power by decoupling the input small signal impedance from the output trans-impedance gain. Measurements indicate operation up to 6 Gb/s data rates at channel losses up to 46 dB with energy cost around 0.63pJ/b, and 0.37pJ/b at 4Gb/s. The eye is measured *in-situ*, with eye sensitivity tests illustrating significantly relaxed tap accuracy requirements when compared to traditional analog FFE by leveraging channel attenuation to minimize the errors.

Chapter 4

Conclusion

In this thesis, the modeling and design methods for the on-chip equalized interconnect over an RC-dominant wire are explained. The modeling framework and infrastructure proposed in this thesis guide a designer in circuit-wire codesign. This is the first comprehensive on-chip equalized link design-space exploration framework that connects the circuit, wire, and equalization parameters to compute the interconnect metrics (eye quality, power, data rate density).

Based on the insights from the design-space exploration, this thesis also proposed new circuit techniques. The new CI FFE driver burns only half power compared to the conventional CS or VD FFE drivers. It also improves eye sensitivity to the coefficient errors about ten times. A static pre-distortion technique enables the use of the cheap CMOS-inverter-style non-linear drivers for the CI FFE, improving the energy-efficiency while still preserving linear operation for existing performance analysis. A TIA at the receiver improves the trade-off between bandwidth and static power as well as signal amplitude.

4.1 Modeling and Analysis

Chapter 2 suggests the first analytical model for an RC-dominant equalized interconnect. The analytical model is based on the lossy transmission line model expressed with driver/receiver's termination impedances and *RLGC* matrices of the wire. The transfer function provided a more accurate closed form solution compared to the traditional π -model or RC ladder model. The formula also suggests the proper design strategies and provides good intuition of the RC-dominant link behavior.

Drivers are analyzed and characterized in Chapter 2. The analytical results show that the CI FFE driver is twice more power efficient than CS or VD FFE drivers in an RC-dominant interconnect. For an off-chip matched transmission line applications, the CI FFE is three times more power efficient than the VD FFE driver.

Eye sensitivity to coefficient error is also analyzed for different driver types. According to the analysis, a CI FFE driver is about ten times less sensitive to coefficient errors than a conventional CS FFE. Due to the small eye sensitivity, the CI FFE can utilize a power-and-area efficient CMOS style driver.

To determine optimal equalization coefficients, fast computation algorithm is demonstrated. Test run time was about two hundred times improved compared to the conventional method. Swing constrained least mean square error solution improves run time about ten times and gives a very close solution to the worst-case-eye-maximization method. Analysis for the sampling time in frequency domain improves the run time by twenty times. With the two improvements, a test run shows that about 400,000 design space can be computed within 45 minutes.

An example analysis on 32nm technology nodes reveals that equalized interconnects provide 2x-10x improved power efficiency than repeaters. This CAD tool can be used stand alone or combined with other design layers such as a NoC layer tool [1]. For example, in [1], the equalized CAD tool is combined with the NoC simulation tool showing that the NoC with equalized interconnects improve energy-efficiency by 2-3x compared to the NoC with repeated interconnects and enable the use of NoCs like Clos and flatten butterfly that depend on an efficient design of long-global interconnects.

4.2 Circuit and Measurement

A test chip was fabricated to demonstrate new circuit techniques.

A 3-tap CI FFE transmitter is designed and the performance is measured. The CI FFE architecture utilizes an inverter-like CMOS-style non-linear driver by a cheap pre-distortion. The inverter-like non-linear driver shows about five-ten times higher current driving ability compared to the conventional linear current source type driver.

The performance and power measurements confirm the power and area efficiency of the CI FFE architecture. The first *in-situ* channel measurement for an on-chip interconnect

revealed a very large channel loss (about 40dB) at the Nyquist frequency confirming that the proposed CI FFE can operate on channels with extremely large loss.

The eye measurement shows that the horizontal eye diagram has good quality even though there is a very high channel loss. This good equalization ability of the CI FFE is in part proved by the eye sensitivity measurement and the eye sensitivity analysis described in Chapter 2. The measurement and analytical model match, and verify that the CI FFE requires ten times relaxed hardware accuracy.

At the receiver, a TIA changes the impact of the termination impedance on bandwidth, signal amplitude, and static power. A TIA provides the small signal impedance for the channel sides which improves bandwidth and the current signal amplitude. The large gain resistance of the TIA suppresses the static current and improves the signal amplitude. As a result, the TIA can achieve 1.5 times amplitude with only the half static power consumption for the same bandwidth compared to the pure-resistive termination. This performance improvement of the design implementation can be predicted from the analytical model developed in Chapter 2.

4.3 Future Work and Projections

The model and the circuit techniques developed in this thesis are not only applicable to on-chip interconnects but also to other RC-dominant channels such as narrow PCB wires, emerging silicon-carrier based packages, and interconnects in large LCD display panels [29, 54, 55]. These interconnects fit in the same model developed in this thesis work but with different scale. Therefore, the circuit techniques and the CAD methods can be directly leveraged to these applications. Since the demand for the high-speed RC-dominant interconnects is increasing due to high integration density and low power consumption requirements, the application scope of this thesis work will keep increasing.

The TIA circuit can be extended with variations for different applications. Depending on the trade-off between static power and dynamic power, the TIA size, type, and the circuit topologies can have lot of variations and optimization. For example, TIA circuitry with inductive peaking might improve the channel's bandwidth as well as the signaling energy. As expected in Equation 2.24, the non-resistive impedance termination may improve the channel. However, the justification of the usefulness depends on the technology, target data

rate, channel length and many other trade-offs.

The CAD tool developed in this thesis can be extended with different types of drivers and receivers. The tool was demonstrated an LCM driver model. However, to cover the range of transceiver topologies, the CAD library must include pulse-width-preemphasis, CI, CS, and SST drivers too. The only part needed to be replaced is the driver's RC switch model (i.e. Thevenin equivalent model) for each driver type.

For the reliability study, the supply noise must be included. The supply noise, especially in a CPU, is one of the key missing pieces of information to justify the reliability of the on-chip equalizing link. Since the received signal is weak, the supply noise plays a critical role. Previous research only covers the limited supply noises since circuits in a test-chip are much smaller and less noisy than a CPU environment. Therefore, extensive measurement from the supply noise in the real CPU environment is necessary.

The study on repeated equalized interconnect is another interesting part remains. Since the benefit of the equalized interconnect strongly depends on the length, there must be an optimal length of the equalized interconnect. By studying the trade-off of the link power/performance of equalized interconnects for various lengths, the efficiency can be improved. Since the optimal length and the target length may be different, placing repeater stages for equalized interconnects is a promising solution for this approach. We have already utilized this technique for very long (15mm) NoC channels in [1] but more detail needs to be done at circuit level to further develop this concept.

For the architectural point of view, the multi-drop and bus type equalizing interconnects study might be interesting. In the hyper-cube type topologies, the multi-drop interconnects are known to improve the NoC performance. Equalized interconnects are easily re-configured to tap out signal at multiple points which may potentially improve the overall NoC performance, but each tap point must have different coefficients for the attached DFE.

4.4 Summary

In this thesis, the first on-chip equalized interconnect model is suggested and explained. By a CAD example, the usefulness of the model is demonstrated and the algorithm in CAD computation shows a significant improvement in run time. Based on the modeling and analysis, the CI FFE transmitter and the TIA receiver are the first proposed and

improves the power/performance efficiency over the previous transceiver architectures. The experimental results confirm 4Gb/s/2 μ m data transmission over 10-mm on-chip wire with only 0.4pJ/b energy cost. At maximum performance, 6Gb/s/2 μ m speed is achieved with only about 0.6pJ/b energy cost.

Bibliography

- [1] A. Joshi, B. Kim, and V. Stojanović, “Designing energy-efficient low-diameter on-chip networks with equalized interconnects,” in *IEEE Symp. on High-Performance Interconnects*, Aug. 2009, pp. 3–12.
- [2] M. B. Taylor and et al., “The raw microprocessor: a computational fabric for software circuits and general-purpose programs,” vol. 22, no. 2, 2002.
- [3] S. Vangal, J. Howard, G. Ruhl, S. Dighe, H. Wilson, J. Tschanz, D. Finan, P. Iyer, A. Singh, T. Jacob, S. Jain, S. Venkataraman, Y. Hoskote, and N. Borkar, “An 80 Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS,” in *IEEE International Solid-State Circuits Conference*, 2007, pp. 98–99, 589.
- [4] S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung, J. Mackay, M. Reif, L. Bao, J. Brown, M. Mattina, C. Miao, C. Ramey, D. Wentzlaff, W. Anderson, E. Berger, N. Fairbanks, D. Khan, F. Montenegro, and J. Z. J. Stickney, “TILE64TM Processor: A 64-Core SoC with Mesh Interconnect,” in *IEEE Int. Solid-State Circuits Conference*, 2008, pp. 88–89, 598.
- [5] U. G. Nawathe, M. Hassan, K. C. Yen, A. Kumar, A. Ramachandran, and D. Greenhil, “Implementation of an 8-core, 64-thread, power-efficient sparc server on a chip,” *IEEE Journal of Solid-States Circuits*, vol. 43, no. 1, pp. 6–20, 2008.
- [6] M. Horowitz and W. Dally, “How scaling will change processor architecture,” in *International Solid-Sate Circuits Conferenece*, Feb. 2004.
- [7] J. Balfour and W. J. Dally, “Design tradeoffs for tiled cmp on-chip networks,” in *International Conference on Supercomputing*, 2006.
- [8] J. Kim, J. Balfour, and W. J. Dally, “Flattened butterfly topology for on-chip networks,” *IEEE Computer Architecture Letters*, vol. 6, pp. 37–40, July 2007.
- [9] —, “Flattened butterfly topology for on-chip networks,” in *Proc. 40th Annual IEEE/ACM International Symposium on Microarchitecture*, Dec. 2007, pp. 172–182.
- [10] C. Clos, “A study of non-blocking switching networks,” vol. 32, p. 406424, 1953.
- [11] B. Grot, J. Hestness, S. W. Keckler, and O. Mutlu, “Express cube topologies for on-chip interconnects,” in *IEEE Int. Symp. on High-Performance Computer Architecture*, Feb. 2009, pp. 163–174.
- [12] H. B. Bakoglu and J. D. Meindl, “Optimal interconnection circuits for vlsi,” vol. ED-32, no. 5, pp. 903–909, May 1985.

- [13] R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," vol. 89, no. 4, 2001.
- [14] R. T. Chang, C. P. Yue, and S. S. Wong, "Near speed-of-light on-chip electrical interconnect," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2002, pp. 18–21.
- [15] S. Tam, e. Socher, A. Wong, , and M. F. Chang, "Simultaneous tri-band on-chip rf-interconnect for future network-on-chip," in *IEEE Int. Symp. VLSI Circuits Dig. Tech. Papers*, June 2009, pp. 90–91.
- [16] A. P. Jose and K. L. Shepard, "Distributed loss-compensation techniques for energy-efficient low-latency on-chip communication," vol. 42, no. 6, pp. 1415–1424, June 2007.
- [17] D. S. et al., "A 3gb/s/ch transceiver for rc-limited on-chip interconnects," in *International Solid-State Circuits Conference*, Feb. 2005.
- [18] D. Shinkel, E. Mensink, E. A. M. Klumperink, E. Tuijl, and B. Nauta, "A 3-gb/s/ch transceiver for 10-mm uninterrupted rc-limited global on-chip interconnects," vol. 41, no. 1, pp. 297–306, Jan. 2006.
- [19] A. P. Jose, G. Patounakis, and K. L. Shepard, "Near speed-of-light on-chip interconnects using pulsed current-mode signaling," pp. 108–111, 2005.
- [20] R. Ho and et al., "High-speed and low-energy capacitive-driven on-chip wires," in *IEEE International Solid-State Circuits Conference*, 2007.
- [21] R. Ho, T. Ono, F. Liu, R. D. Hopkins, A. Chow, J. Schauer, F. Y. Liu, and R. Drost, "High-speed and low-energy capacitively-driven on-chip wires," vol. 43, no. 1, pp. 52–60, Jan. 2008.
- [22] E. Mensink, D. Shinkel, E. Klumperink, E. Tuijl, and B. Nauta, "A 0.28pj/b 2gb/s/ch transceiver in 90nm cmos for 10mm on-chip interconnects," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 414–415, 612.
- [23] B. Kim and V. Stojanović, "Equalized interconnect for on-chip networks: Modeling and optimization framework," in *in Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, 2007, pp. 552–559.
- [24] ———, "Characterization of equalized and repeated interconnects for noc applications," vol. 25, pp. 430–439, Sept. 2008.
- [25] ———, "A 4 Gb/s/ch 356 fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmitter Filter and Transimpedance Receiver in 90 nm CMOS Technology," in *IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, Feb. 2009, pp. 66–67, 978.
- [26] W. Dally and J. Poulton, "Transmitter equalization for 4-gbps signaling," vol. 17, pp. 48–56, Jan/Feb 1997.
- [27] B. S. Landman and R. L. Russo, "On a pin versus block relationship for partitions of logic graphs," vol. vol. C-20, pp. 1469–1479, 1971.
- [28] P. Christie and D. Stroobandt, "The interpretation and application of rent's rule," vol. 8, no. 6, pp. 639–648, Dec. 2000.

- [29] Y. Liu, B. Kim, T. Dickson, J. Bulzacchelli, and D. Friedman, "A 10 gb/s compact low-power serial i/o with dfe-iiir equalization in 65 nm cmos," in *IEEE Int. Solid-State Circuits Dig. Tech. Papers*, Feb. 2009, pp. 182–183.
- [30] R. B. et al., "A 16gb/s adaptive bandwidth on-chip bus based on hybrid current/voltage mode signaling," in *IEEE VLSI*, 2004.
- [31] N. T. et al., "Differential current-mode sensing for efficient on-chip global signaling," 2005.
- [32] H. Hatamkhani, K. J. Wong, R. Drost, and C. K. Yang, "A 10-mw 3.6-gbps i/o transmitter," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2003, pp. 97–98.
- [33] H. Hatamkhani and C. K. Yang, "Power analysis for high-speed i/o transmitters," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2004, pp. 142–145.
- [34] K. W. H. H. M. Mansuri and C. Yang, "A 27-mw 3.6gb/s i/o transceiver," vol. 39, 2004.
- [35] C. Menolfi, T. Toiff, P. Buchmann, M. Kossel, T. Morf, J. Weiss, and M. Schmatz, "A 16gb/s source-series terminated transmitter in 65nm cmos soi," in *IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, Feb. 2007, pp. 446–447, 614.
- [36] J. Ren and M. Greenstreet, "A unified optimization framework for equalization filter synthesis," in *IEEE Design Automation Conference*, 2005, pp. 638–643.
- [37] <http://www.rle.mit.edu/isg/technology.htm>.
- [38] R. Ho, *On-chip Wires: Scaling and Efficiency*. Stanford, 2003.
- [39] T. Lin and L. T. Pileggi, "Throughput-driven ic communication fabric synthesis," in *International Conference on Computer Aided Design*, 2002, pp. 279–284.
- [40] R. Ho, K. Mai, and M. Horowitz, "Efficient on-chip global interconnects," in *Symposium on VLSI Circuits, Digest of Technical Papers*, 2003, pp. 271–274.
- [41] A. Joshi, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanović, "Silicon-photonics networks for global on-chip communication," in *in Proc. ACM/IEEE International Symposium on Networks-on-Chip*, May 2009.
- [42] W. J. Dally and B. P. Towles, *Principles and Practices of Interconnection Networks*. Elsevier, 2004.
- [43] H. Wang, L.-S. Peh, and S. Malik, "A technologyaware and energy-oriented topology exploration for on-chip networks," in *Design, Automation and Test in Europe, Proceeding*, vol. 2, March 2005, pp. 1238–1243.
- [44] J. F. Bulzacchelli, M. Meghelli, S. V. Rylov, W. Rhee, A. V. Rylyakov, H. A. Ainspan, B. D. Parker, M. P. Beakes, A. Chung, T. J. Beukema, P. K. Pepljugoski, L. Shan, Y. H. Kwark, S. Gowda, and D. J. Friedman, "A 10-gb/s 5-tap dfe/4-tap ffe transceiver in 90-nm cmos technology," vol. 41, no. 12, Dec. 2006.
- [45] S. Kasturia and J. H. Winters, "Techniques for high-speed implementation of nonlinear cancellation," vol. 9, no. 6, pp. 711–717, June 1991.

- [46] L. Zhang, J. Wilson, R. Bashirullah, L. Lei, X. Jian, and P. Franzon, "A 32gb/s on-chip bus with driver pre-emphasis signaling," in *Custom Integrated Circuits Conference*, Sept. 2006.
- [47] Y.-S. Sohn, S.-J. Bae, H.-J. Park, C.-H. Kim, and S.-I. Cho, "A 2.2 gbps cmos look-ahead dfe receiver for multidrop channel with pin-to-pin time skew compensation," in *IEEE Custom Integrated Circuits Conf.*, Sep. 2003, pp. 473–476.
- [48] V. Stojanović, A. Ho, B. W. Garlepp, F. Chen, G. T. J. Wei, E. Alon, R. T. Kollipara, C. W. Werner, J. L. Zerbe, and M. A. Horowitz, "Autonomous dual-model (pam2/4) serial link transceiver with adaptive equalization and data recovery," in *IEEE J. Solid-State Circuits*, vol. 40, no. 4, Apr. 2005, pp. 1012–1026.
- [49] A. Rylyakov, "An 11gb/s 2.4mw half-rate sampling 2-tap dfe receiver in 65nm cmos," in *Dig. Symp. VLSI Circuits*, June 2007.
- [50] M. Park, J. Bulzacchelli, and D. Friedman, "A 7 gb/s 9.3 mw 2-tap current-integrating dfe receiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007.
- [51] B. Kim, Y. Liu, T. O. Dickson, J. F. Bulzacchelli, and D. J. Friedman, "A 10-gb/s compact low-power serial i/o with dfe-iir equalization in 65-nm cmos," vol. 44, pp. 3526–3538, December 2009.
- [52] B. Nikolić, V. Stojanović, V. G. Oklobdzija, W. Jia, J. Chju, and M. Leung, "Sense amplifier-based flip-flop," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1999, pp. 282–283, 468.
- [53] K.-L. J. Wong and C.-K. K. Yang, "Offset compensation in comparators with minimum input-referred supply noise," vol. 30, no. 5, May 2004.
- [54] C. S. Patal, "Silicon carrier for computer systems," in *Proc. IEEE/ACM Design Automation Conference*, July 2006, pp. 857–862.
- [55] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, C. S. Patel, R. J. Polastre, K. Sakuma, E. S. Sprogis, C. K. Tsang, B. C. Webb, and S. L. Wright, "3d silicon integration," in *IEEE Proc. the 58th Electronic Components and Technology Conference*, May 2008, pp. 538–543.