Chapter 3. Epitaxial Growth and Processing of Compound Semiconductors

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3.1 Introduction

The emphasis of the research program involves primarily the epitaxial growth and processing of a wide variety of compound semiconductors (both II-VI and III-V), as well as multilayered structures composed of II-VI/III-V and III-V/III-V heterostructures. The epitaxial growth of the heterostructures is performed in the chemical beam epitaxy laboratory which consists of two gaseous source epitaxy reactors (II-VI-dedicated and III-V-dedicated) interconnected to several smaller chambers which are used for sample introduction, and *in-situ* surface analysis. Such a multichamber epitaxy system allows the fabrication of the aforementioned heterostructures to be accomplished within a continuous ultrahigh vacuum environment. The interconnected reactors enable an additional degree of freedom in device design by providing the ability to integrate the II-VI and III-V material families into a single device. For example, structures containing only III-V epilayers or only II-VI epilayers are grown in a single reactor, or in the case of II-VI/III-V heterostructures and quantum wells both reactors are used. The III-V gas source molecular beam epitaxy (GSMBE) reactor uses solid elemental sources of Ga, In, Al, Si and Be and gaseous hydride sources of arsenic and phosphorus. The III-V reactor also has an atomic hydrogen source that is used to remove the native surface oxide from the samples prior to growth as well as an *in-situ* spectroscopic ellipsometer to characterize the epilayer during growth. The II-VI reactor currently uses solid elemental sources of Zn and Se, in addition to a nitrogen plasma source and a solid $ZnCl_2$ source to achieve p- and n-type doping, respectively.

In the next sections, we will describe our progress in the various II-VI and III-V based projects. One of the II-VI based projects investigated the ways to reduce the non-radiative defects in ZnSe by examining the role of the surface chemistry at the II-VI/III-V interface and the lattice mismatch between the ZnSe and the III-V buffer layer. An additional II-VI/III-V effort involves the fabrication of ZnSe/GaAs quantum well structures, focusing on the formation of and resultant properties of the ZnSe/III-V heterovalent structure. The III-V GSMBE system is also utilized for the fabrication of (In,Ga)(As,P) waveguide-based devices and light emitters that operate at a wavelength of 1.55 μm, the wavelength used for optical fiber communication. Additional III-V-based projects include the fabrication of optoelectronic devices on premetalized GaAs MESFET integrated circuits for optoelectronic integrated circuits, and the fabrication of photonic bandgap crystals utilizing an air bridge microcavity structure. The fabrication of 3-D photonic bandgap crystals is also under investigation.

3.2 Reducing the Defect Density in MBE-ZnSe/III-V Heterostructures

Sponsors

Defense Advanced Research Projects Agency/
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Subcontract N00014-92-J-1893
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The need for compact, long-lived, blue-green semiconductor laser diodes is driven by the advantages gained by implementing a short wavelength laser in technologies that are dependent on the wavelength such as high density optical recording. Currently, the two wide-bandgap material systems that promise to meet the aforementioned challenge are Zn chalcogenide-based II-VI materials and GaN-based III-V materials. In both cases, defect generation and control are at the forefront of the issues requiring investigation. The use of III-V phosphide-based (In,Ga,Al)P buffer layers, placed between the wide-bandgap ZnSe layer and the GaAs substrate is being investigated. The phosphorus-containing III-V alloy enables both the gradation of the energy bandgap and the lattice constant, suggesting that the large 1 eV valence band discontinuity present between the ZnSe and the GaAs substrate can be greatly reduced, thus facilitating hole injection.[1] A lattice-matched ohmic contact composed of p-type III-V materials on a III-V substrate offers an alternative to the use of a highly lattice-mismatched Zn(Se,Te) graded-layer ohmic contact.[2] Such a III-V ohmic contact requires the proper nucleation of the II-VI layer on the III-V surface to minimize defect generation, subsequently increasing both the luminescence efficiency and the optical device lifetime.[3]

A variety of III-V buffer layers were grown by gas source molecular beam epitaxy (GSMBE) on GaAs substrates. These III-V layers were then used as epitaxial substrates for the 1-μm thick ZnSe epilayers in a study of both the nucleation and the effect of lattice-match on defect density in the ZnSe layer. First, a set of experiments was carried out to study the nucleation of ZnSe on c(4X4)- and (2X4)-reconstructed GaAs surfaces. The different surface reconstructions reflect varying amounts of arsenic coverage with a (2X4)-reconstructed surface having an As surface coverage of 75 percent and a c(4X4)-reconstructed surface being completely covered by arsenic. A second set of experiments utilized lattice-matched 4-μm thick (In,Ga)P buffer layers to study the effect of lattice-match. Such a lattice-matched II-VI/III-V interface was created by varying the alloy fraction of the phosphide-based buffer layer to grade the in-plane lattice constant from that of the GaAs substrate to that of the ZnSe device layer.[4] ZnSe has a lattice constant that is 0.27 percent larger than GaAs. Finally, to isolate the effect of lattice-match from that of the interfacial chemistry, the phosphide surface was capped with eight monolayers of the previously studied c(4X4)- or (2X4)-reconstructed GaAs prior to the ZnSe nucleation. The structures were monitored *in-situ* using reflection high energy electron diffraction (RHEED), both before and after transferring the sample in vacuum from the III-V-dedicated reactor to the II-VI-dedicated reactor. The ZnSe cathodoluminescence (CL) was evaluated at room temperature by employing a JEOL JSM 6400 scanning electron microscope with an Oxford Instrument's MonoCL collection system. The electron beam energy was 20 keV to insure the full excitation of the 1 μm ZnSe epilayer.[5] The surface morphology was characterized in air by atomic force microscopy (AFM) using a Digital 3000 Nanoscope in the tapping mode. An estimate of the threading dislocation density was determined by room temperature etch pit density (EPD) measurements using a solution of 1 percent bromine-in-methanol to etch 250 nm of the ZnSe in order to elucidate extended defects that intersect the surface. X-ray diffraction double crystal rocking curves were used to determine the in-plane and the out-of-plane lattice constants of the epilayer.

Since the initial CL characterization of the ZnSe on lattice-matched (In,Ga,Al)P surfaces indicated the presence of an unexpectedly high density of dislocations, the role of the surface chemistry was examined by using GaAs buffer layers that exhibited a c(4X4)- or a (2X4)-surface reconstruction along with various ZnSe nucleation procedures. The origin of such a high density of defects in the ZnSe/(In,Ga,Al)P structures was speculated to be

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1 K. Iwata, H. Asashi, J.H. Kim, X.F. Liu, S. Gonda, Y. Kawaguchi, A. Ohki, and T. Matsuoka, "Gas Source Molecular Beam Epitaxy Growth of InAlP Band Offset Reduction Layers on p-type ZnSe," *J. Cryst. Growth* 150(1-4): 833-837 (1995).

2 Y. Fan, J. Han, L. He, J. Saraie, R.L. Gunshor, M. Hagerott, H. Jeon, A.V. Nurmikko, G.C. Hua, and N. Otsuka, "Graded Band Gap Ohmic Contact to p-ZnSe," *Appl. Phys. Lett.* 61(26): 3160-3162 (1992).

3 A. Ishibashi, "II-VI Blue-green Laser Diodes," *IEEE J. Select. Topics Quantum Electron.* 1(2): 741-748 (1995).

4 K. Lu, J.L. House, P.A. Fisher, C.A. Coronado, E. Ho, G.S. Petrich, L.A. Kolodziejski, "(In,Ga)P Buffer Layers for ZnSe-based Visible Emitters," *J. Cryst. Growth* 138 (1-4): 1-7 (1994).

5 K. Kanaya and S. Okayama, "Penetration and Energy-Loss Theory of Electrons in Solid Targets," *J. Phys. D* 5(1): 43-58 (1972).

due to the surface chemistry and the ZnSe nucleation conditions. Using atomic force microscopy, a mean roughness R_a of 9 Å and 7 Å was measured from the sample that exhibited the c(4X4)-reconstructed surface and from the sample that exhibited the (2X4)-reconstructed GaAs surface, respectively. In other sets of similar films, the R_a values from the ZnSe epilayers grown on c(4X4)-reconstructed GaAs were consistently larger than the values measured from the ZnSe epilayers grown on (2X4)-reconstructed GaAs. Utilizing migration-enhanced epitaxy (MEE) during the initial stage of heteroepitaxy resulted in the same conclusion that a (2X4)-reconstructed GaAs surface gives rise to a smoother ZnSe layer.

A dramatic difference between the CL images of the ZnSe films grown on the c(4X4)- and the (2X4)-reconstructed GaAs buffer layers was observed, as shown in figure 1. The contrast in the CL images is due to variations in the amount of non-radiative recombination and hence, yields information about the density of threading dislocations which act as non-radiative recombination sites.[6] From the CL images, the defect densities were estimated to be $7x10^6\,cm^{-2}$ and $9x10^5\,cm^{-2}$ for the ZnSe that was grown on a c(4X4)-reconstructed GaAs buffer layer and the ZnSe that grown on a (2X4)-reconstructed GaAs buffer layer, respectively. These defect densities were correlated to the EPD values of $10^7\,cm^{-2}$ and $10^6\,cm^{-2}$ for these structures. Characterization of the set of MEE-initiated samples did not demonstrate a noticeable difference in defect densities between the MBE and the MEE growth of ZnSe on (2X4)- reconstructed GaAs.

The growth of fully relaxed ZnSe nucleated with a Zn pre-exposure on a (2X4)-reconstructed GaAs surface seems to result in a lower threading dislocation density and a smoother surface than ZnSe grown on a c(4X4)-reconstructed GaAs surface. The observation of reduced defect densities in ZnSe epilayers grown on (2X4)-reconstructed GaAs agrees with another recent study.[7] The complexity of the ZnSe/GaAs intefacial layer makes it difficult to isolate the reason for the reduced defect density in ZnSe grown on (2X4)-reconstructed GaAs surfaces compared to ZnSe grown on c(4X4)-reconstructed GaAs surfaces. A contributing factor for the difference is that a more charge neutral interface is formed on a (2X4)-reconstructed GaAs surface as opposed to a c(4X4)-reconstructed GaAs surface. A completely charge neutral interface can be formed if the anion plane is 50 percent As and 50 percent Se. (2X4)-reconstructed GaAs has, on average, a 75 percent As surface coverage,

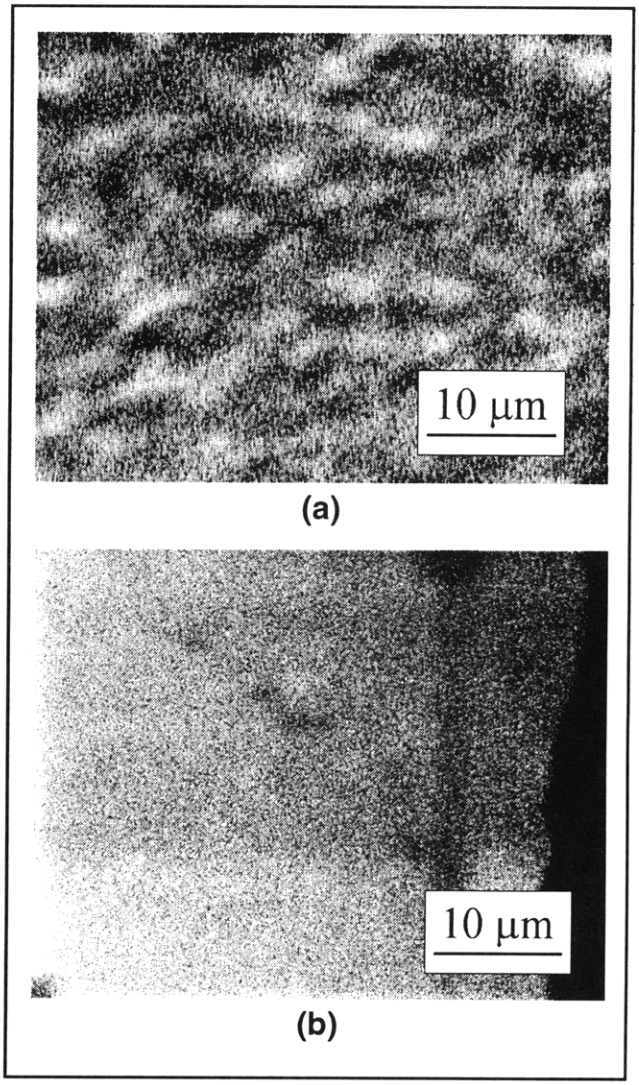

Figure 1. The room temperature cathodoluminescence of 1 μm ZnSe films grown by MBE on (a) a Zn-exposed c(4X4)-reconstructed GaAs buffer layer and (b) a Zn-exposed (2X4)-reconstructed GaAs buffer layer. The defect density was estimated to be 7 X $10^6\,cm^{-2}$ and 9 X $10^5\,cm^{-2}$, respectively. The electron probe parameters were: 30 nA, 20 keV. The magnification was 1700 times.

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6 B.G. Yacobi and D.B. Holt, "Cathodoluminescence Scanning Electron Microscopy of Semiconductors," *J. Appl. Phys.* 59(4): R1-R24 (1986).

7 Z. Yu, S.L. Buczkowski, N.C. Giles, and T.H. Myers, "Defect Reduction in ZnSe Grown by Molecular Beam Epitaxy on GaAs Substrates Cleaned by Atomic Hydrogen," *Appl. Phys. Lett.* 69(1): 82-84 (1996).

which is lower than the 100 percent surface coverage of c(4X4)-reconstructed GaAs.[8]

The second set of samples incorporated a 4 μm thick (In,Ga)P buffer layer placed between the ZnSe epilayer and the GaAs substrate, which allowed the in-plane lattice constant to be modified in order to minimize the lattice-mismatch at the II-VI/III-V interface. Figure 2 shows the CL images from these samples. The dark spots seen in figures 2a and 2b are due to threading dislocations, while the dark lines seen in figure 2c are due to misfit dislocations. The CL images show, in figure 2a, ZnSe grown on InGaP, and figure 2b, ZnSe grown on a c(4X4)-reconstructed GaAs cap on InGaP, appear to be nearly identical to those shown in figure 1a. This suggests that the high dislocation density in these samples are due to poor nucleation and that the reduction of the lattice-mismatch does not have a noticeable effect. The density of threading dislocations in these samples is estimated to be approximately 10^7 cm^{-2}, both from the CL images and from EPD measurements.

In contrast, the CL image shown in figure 2c, ZnSe grown on a (2X4)-reconstructed GaAs cap on InGaP, primarily exhibits misfit dislocations with faint features due to various types of irregularities in the crystal lattice. Since CL imaging shows enhanced contrast at misfit dislocations, these represent the dominant form of dislocations in this film. This suggests that the growth of ZnSe on (2X4)-reconstructed GaAs minimizes threading dislocations arising from the II-VI/III-V nucleation such that the slight lattice-mismatch in the sample, as shown in figure 2c, plays the primary role in the dislocation process in this sample. The average spacing of the misfit lines is approximately 3 μm, indicative of the close lattice-match[9] which was confirmed by x-ray diffraction measurements. CL and EPD measurements both suggest a threading dislocation density of less than 10^5 cm^{-2} in this sample. The remaining dislocations are speculated to arise either from the fully-strained pseudomorphic GaAs cap layer or from the relaxed III-V/III-V buffer layer.

The 1-μm ZnSe layers on various lattice-matched III-V epitaxial substrates were also characterized by AFM. The AFM results obtained on the ZnSe, that was grown directly on the InGaP buffer layer, are very encouraging as the measured R_a value is roughly 4 Å, indicative of a very smooth growth front. The AFM result is not completely unexpected as reflection high energy electron diffraction intensity oscillations are routinely observed during the nucleation of ZnSe on phosphorus-containing III-V surfaces. AFM also showed that ZnSe grown on the (2X4)-reconstructed GaAs surface on lattice-matched InGaP results in a much smoother ZnSe layer (R_a ~3 Å) as compared to ZnSe grown on the c(4X4)-reconstructed GaAs surface on InGaP (R_a ~ 7 Å).

The nucleation study of ZnSe on c(4X4)- and (2X4)-reconstructed GaAs surfaces identified the (2X4)-reconstructed surface as contributing to a lower density of extended defects and to a smoother overall surface. However, a 0.27 percent in-plane lattice constant mismatch was present, and also contributed to the generation of defects due to plastic strain relief. To examine the role of lattice-matching, the surface chemistry, i.e., ZnSe on GaAs, was maintained, while the underlying in-plane lattice constant was graded. This was accomplished by the deposition of eight monolayers of GaAs on graded (In,Ga)P buffer layers. With a (2X4)-reconstructed GaAs cap, the elimination of the lattice-mismatch by the use of a (In,Ga)P buffer layer results in a dislocation density of less than 10^5 cm^{-2}, with the residual dislocations most likely originating in the relaxed, but lattice-mismatched III-V/III-V structure.

3.2.1 Publications

Ho, E., G.S. Petrich and L.A. Kolodziejski. "Comparison of Hydrogen Passivation of ZnSe:N using Gas Source and Conventional Molecular Beam Epitaxy." *J. Cryst. Growth* 159(1-4): pp. 266-70 (1996).

Warlick, E.L., E. Ho, G.S. Petrich, and L.A. Kolodziejski. "Reducing the Defect Density in MBE- ZnSe/III-V Heterostructures." Paper presented at the Ninth International Conference on Molecular Beam Epitaxy, Malibu, Calfornia, August 4-9, 1996; *J. Cryst. Growth.* Forthcoming.

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8 D.K. Biegelsen, R.D. Bringans, J.E. Northrup, and L.-E. Swartz, "Surface Reconstructions of GaAs(100) Observed by Scanning Tunneling Microscopy," *Phys. Rev. B.* 41(9): 5701-5706 (1990).

9 C.H. Simpson and W.A. Jesser, "On the Use of Low Energy Misfit Dislocation Structures to Filter Threading Dislocations in Epitaxial Heterostructures," *Phys. Stat. Sol. A* 149(1): 9-20 (1995).

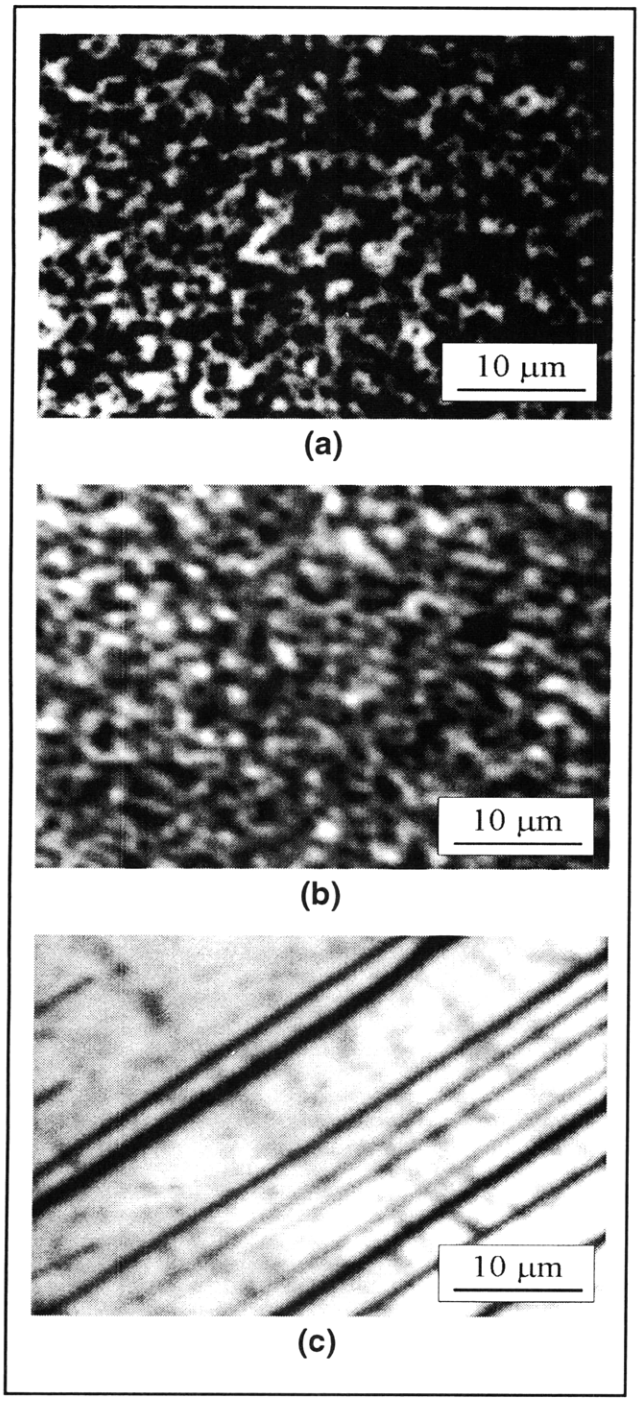

Figure 2. The room temperature cathodoluminescence of 1 μm ZnSe films grown by MBE on 4 μm linearly graded (In,Ga)P buffer layers (a) without a GaAs layer between the (In,Ga)P and ZnSe, (b) with a Zn-exposed, 8-monolayer-thick, c(4X4)-reconstructed GaAs layer between the (In,Ga)P and the ZnSe, and (c) with a Zn-exposed, 8-monolayer-thick, (2X4)-reconstructed GaAs layer between the (In,Ga)P and the ZnSe. The (In,Ga)P lattice constant was graded from that of GaAs to that of ZnSe. The electron probe parameters were: 30 nA, 20 keV. The magnification was 1700 times.

3.3 Microstructural Analysis of ZnSe/GaAs Heterostructures

Sponsors

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University Research Initiative
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Project Staff

Professor Erich P. Ippen, Professor Leslie A. Kolodziejski, Dr. Gale S. Petrich, David J. Dougherty, Jody L. House, Emily L. Warlick

The integration of II-VI and III-V semiconductors into a single II-VI/III-V heterojunction device enables the exploitation of the many similarities, as well as the many differences, in material properties (energy bandgap, lattice constant, dielectric constant, etc.) to create new devices exhibiting unique optical and electronic properties. In this project, epitaxially-grown dielectric GaAs quantum wells (QWs) with ZnSe barriers are under investigation.

An assessment of the microstructural properties of the ZnSe/GaAs heterostructure contributes to the understanding of the relationship between the epitaxial growth parameters and the resultant optical and electronic properties. Microstructural analysis can be achieved from a combination of cross-sectional transmission electron microscopy (TEM) and atomic force microscopy (AFM). Cross-sectional TEM can reveal information about the origin and orientation of the defect-structure of a material with defect densities greater than 10^5 cm^{-2}. AFM allows the surface roughness to be measured on regions up to 10 μm X 10 μm in size. When used in conjunction with one another, TEM and AFM analyses provide an insight into the microstructural properties of a material.

A heterostructure, intended for device purposes, needs to have well-defined characteristics; this includes the electronic properties of the heterointerfacial regions. In ZnSe/GaAs heterostructures, ZnSe and GaAs are composed of elements with different valences which allows the four different elements to bond at the interface with different configurations. For example, an abrupt interface can be formed theoretically, where there are no interfacial layers of Ga, Zn, Se, and As. In this

instance, an electronic imbalance results from the dangling bonds, and an associated electric field creates a region depleted of carriers for stability. When a few transitional monolayers occur, the heterostructure is no longer entirely ZnSe and GaAs. One of the goals of this study is to determine which of these two extremes is the best from a device perspective. There has been a great deal of work to date in defining the electronic structure of the ZnSe on GaAs heterostructure. Theoretically, the valence band-offset has been shown to vary from 0.7 eV to 1.59 eV, depending on the ZnSe/GaAs interface formation.[10] However, little is known about the far-reaching effects of these different interfaces.

One of the critical factors affecting the properties of the ZnSe/GaAs QW structure is the formation of the heterovalent interfaces, particularly the formation of the inverted interface that is formed when GaAs is nucleated onto a ZnSe epitaxial surface. The stoichiometry of each interface is engineered by using various growth techniques. Due to the severe mismatch in the optimal growth temperatures for the two material systems (600 degrees C) for GaAs and 300 degrees C for ZnSe), additional emphasis has been placed on the reduced temperature growth of GaAs on ZnSe. The nucleation of GaAs on ZnSe has been optimized with a reduced-temperature (250 degrees C) deposition of the first few monolayers (MLs).[11] Cross-sectional TEM analysis has shown that a minimum of three monolayers of the reduced-temperature GaAs is desirable for achieving a subsequently defect-free heterostructure. Figure 3 compares the microstructure of a 6 nm GaAs single QW with and without three monolayers of reduced-temperature GaAs nucleated at the start of the quantum well. Furthermore, using AFM, the ZnSe surface roughness of a GaAs single QW structure grown with three monolayers of reduced-temperature GaAs is less than the surface roughness of a GaAs single QW structure grown without the three monolayers of reduced-temperature GaAs.

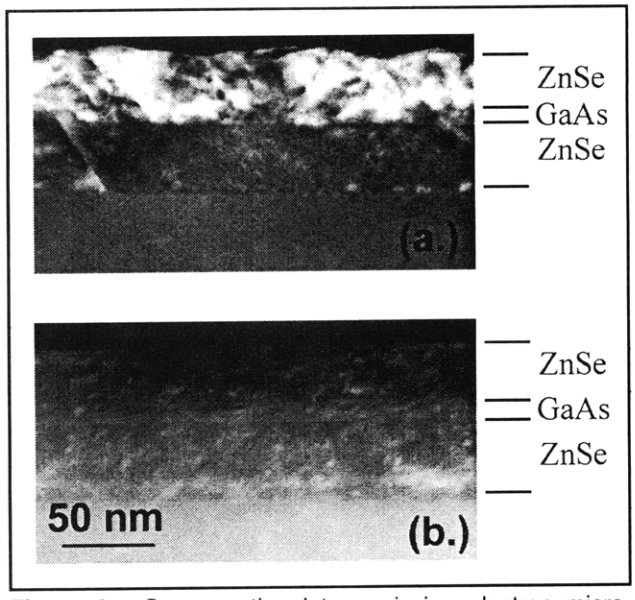

Figure 3. Cross-sectional transmission electron micrographs of GaAs nucleated on an epitaxial ZnSe surface. In (a) the GaAs layer was nucleated without an initial deposition of reduced-temperature GaAs. In (b) the GaAs was initially nucleated with three monolayers of reduced-temperature GaAs.

The combination of time and substrate temperature appears to be crucial to the growth of a defect-free GaAs layer on ZnSe. After the initial deposition of the reduced-temperature GaAs, the rest of the quantum well layer has been epitaxially-grown using a variety of conditions. The initial reduced-temperature GaAs layer (3 MLs) is not sufficient to ensure the subsequent two-dimensional crystal growth of a GaAs quantum well. It must be followed by at least 3 additional monolayers of GaAs that are deposited one monolayer at a time and at a substrate temperature between 300 degrees C and 350 degrees C.

Optimization of the epitaxial growth of a ZnSe/GaAs single quantum well has been attempted and characterized via microstructural analysis. However, although the resultant optimized heterostructure is defect-free within the sensitivity of the characterization methods employed, optical and electrical con-

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[10] G. Bratina, R. Nicolini, L. Sorba, L. Vanzetti, G. Mula, X. Yu, and A. Franciosi, "ZnSe-GaAs Heterojunction Parameters," *J. Cryst. Growth* 127(1-4): 387-391 (1993); G. Bratina, L. Vanzetti, R. Nicolini, L. Sorba, X. Yu, A. Franciosi, G. Mula, and A. Mura, "Microscopic Control of ZnSe-GaAs Heterojunction Band Offsets," *Physica B* 185(1-4): 557-565 (1993); G. Bratina, L. Vanzetti, L. Sorba, G. Biasiol, A. Franciosi, M. Peressi, and S. Baroni, "Lack of Band-Offset Transitivity for Semiconductor Heterojunctions with Polar Orientation: ZnSe-Ge(001), Ge-GaAs(001), and ZnSe-GaAs(001)," *Phys. Rev. B* 50(16): 11,723-11,729 (1994); A. Kley and J. Neugebauer, "Atomic and Electronic Structure of the GaAs/ZnSe(001) Interface," *Phys. Rev. B* 50(12): 8616-8628 (1994); R. Nicolini, L. Vanzetti, G. Mula, G. Bratina, L. Sorba, A. Mura, J.E. Angelo, W. W. Gerberich, and A. Franciosi, "Local Interface Composition and Band Offset Tuning in ZnSe-GaAs(001) Heterostructures," *Phys. Rev. Lett.* 72(2): 294-297 (1994).

[11] J.L. House, D.J. Dougherty, G.S. Petrich, L.A. Kolodziejski, E.P. Ippen, and G.-C. Hua, "Growth and Characterization of ZnSe/GaAs Single Quantum Well Structures," *Appl. Surf. Sci.* 104-105: 472-478 (1996).

finement in the GaAs quantum well has yet to be demonstrated. Optical characterization, using pump-probe analysis, has shown that the carrier lifetimes in the GaAs are sufficiently long to measure the emission from the well using a standard optical detection system, such as a photodetector or photomultiplier. Another possible cause for the limitations in the optical quality of the GaAs well material, results from the energy band alignment in the conduction band between the GaAs and ZnSe material. Single-heterostructures are under investigation to determine the extent of electron carrier confinement for GaAs wells with ZnSe barriers. See chapter "Optics and Quantum Electronics."

3.3.1 Publications

House, J.L., D.J. Dougherty, G.S. Petrich, L.A. Kolodziejski, E.P. Ippen, and G.-C. Hua, "Growth and Characterization of ZnSe/GaAs Single Quantum Well Structures." *Appl. Surf. Sci.* 104/105: 472-478 (1996).

3.4 Growth of (In,Ga)P/GaAs LEDs for Optoelectronic-VLSI

Sponsor

National Center for Integrated Photonics Technology
Contract 542-381

Project Staff

Professor Clifton G. Fonstad, Jr., Professor Leslie A. Kolodziejski, Dr. Sheila Prasad,[12] Dr. Gale S. Petrich, Joseph F. Ahadian, Steven G. Patterson, Praveen T. Viadyananthan

Work in the past year has led to the successful integration of (In,Ga)P/GaAs light emitting diodes (LEDs) onto Vitesse-processed GaAs VLSI circuits (figure 4). In order to prevent circuit performance degradation, we have employed gas source molecular beam epitaxy (GSMBE) to deposit the LEDs at temperatures below 475 degrees C. This was possible due to the use of an atomic hydrogen source within the GSMBE system that allowed the native GaAs oxide to be removed from the surface at temperatures below 475 degrees C without resorting to the usual method of thermally desorbing the oxide at 580 degrees C. Several fabrication issues related to preparing the VLSI chips for growth were mastered in order to successfully integrate the LEDs onto the VLSI chips.

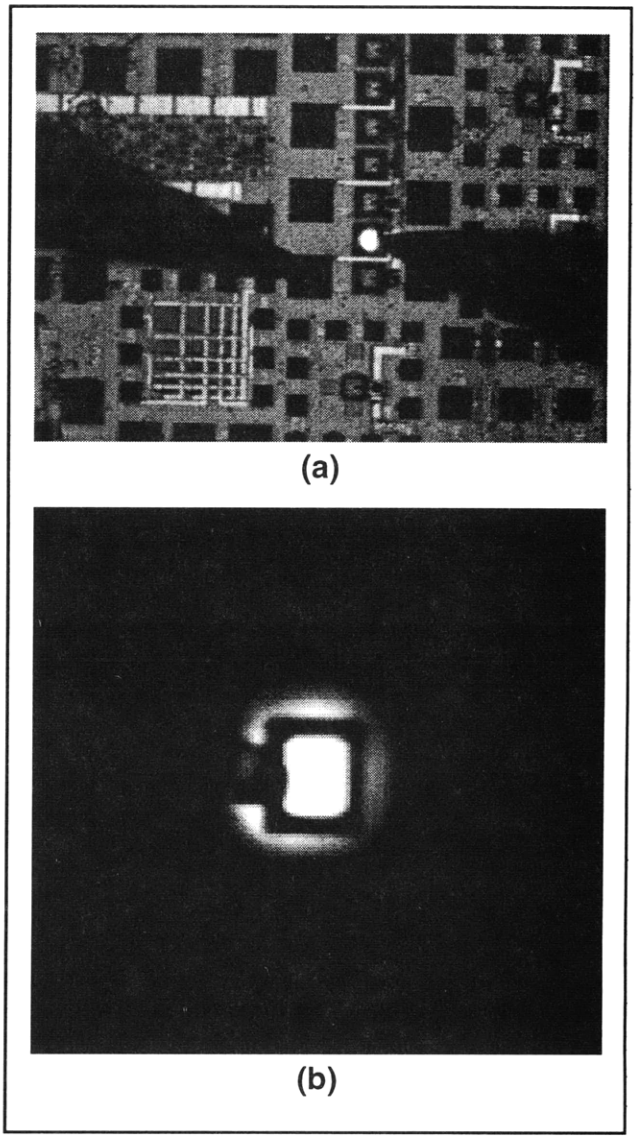

Figure 4. (a) An operating integrated light emitting diode on a GaAs VLSI integrated ciruit. (b) An enlargement of the LED.

Following the design of the VLSI MESFET circuits, Vitesse Semiconductor Corporation fabricates the electronic portion of the circuit using their HGaAs-III process.[13] One of the last processing steps performed by Vitesse, involves the partial removal of

[12] Northeastern University, Boston, Massachusetts.

[13] Vitesse Semiconductor Corporation, Camarillo, California.

the various layers of dielectric material from the areas that are designated for the optical emitters. Within these areas, known as dielectric growth windows (DGW), resides a layer of aluminum with a tungsten nitride cladding (the first metal interconnect layer) a 0.5-μm layer of silicon dioxide and below this, a 300 Å layer of silicon nitride. After the VLSI chips arrive at MIT, the metal and dielectric material remaining in the dielectric growth window are removed to exposed the GaAs substrate. The first step in this cleaning process involves the deposition of a high quality layer of silicon dioxide over the bond pad metal (as a means of protecting the bond pad metal from damage during subsequent processing). Although the aluminum layer capping the dielectric growth well is easily removed, the underlying oxide and nitride layers (most likely due to the high temperature annealing steps involved in the VLSI process) have proven to be more difficult to remove. Due to the thickness of the dielectric material and the inability of the photoresist to withstand the etching process, these layers are removed by repeating the process of photolithographically defining the wells and etching the exposed dielectric material in a buffered oxide etch solution.

DGW cleaning has also been accomplished through the use of an oxygen plasma etch. Subsequent examination of the epilayers that were grown on the oxygen-plasma-cleaned chips and bulk wafers, however, has indicated the presence of jagged, protruding defects by scanning electron microscopy. Although, the origin of these defects is now known to be the result of the plasma etching step, the exact mechanism leading to their formation is still unknown. The photoresist is currently being removed by using 1-methyl 2-pyrrolidinone and acetone in conjunction with the standard degreasing procedure. Using this method, high quality GaAs can be deposited within the DGWs. Once the DGWs are cleaned and the LED deposition performed, the polycrystalline material that was deposited onto the dielectric stack, is removed. Parallel efforts have been undertaken to remove the polycrystalline material using wet chemical etching or reactive ion etching. Finally, the use of titanium/-platinum ohmic contacts allows the LEDs to be connected to the VLSI circuitry using Al wires.

During the past year, the first ever OPTOCHIP offering was made. This multi-university project chip includes nine designs which include light emitting and detecting devices, from various educational institutions along with MIT. The chips are fabricated by Vitesse (via MOSIS) and the optical emitters have been grown in the DGW at MIT. The chips are currently in the final processing stages. Upon the completion of the devices, each participating educational institution will receive at least two chips for testing. Applications being investigated by these groups include Viterbi decoders, image and parallel processing, remote sensing, and neural networks. Such a robust initial response and the breadth of applications indicate the desirability of aggressively developing opto-electronic integrated circuits.

The following year looks to be quite exciting, with efforts now turning toward the development of vertical cavity and in-plane surface emitting lasers, optical waveguides, and possibly the initial investigation of optical interconnect architectures.

3.5 InP-Based Devices for Optical Communication Networks

Sponsors

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Project Staff

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As communication networks continue to increase in speed and bandwidth, the semiconductor industry must continue to strive to provide network designers with devices that will meet their needs. Among the more critical requirements are the need for optical devices that operate with little or no drive current so that they may function, or cause another optical source to function, at extremely high pulse rates, as well as the need for single mode optical sources. The latter devices at the low loss (1.55 μm) and dispersion zero (1.3 μm) wavelengths of standard optical fiber are the backbone of future all-

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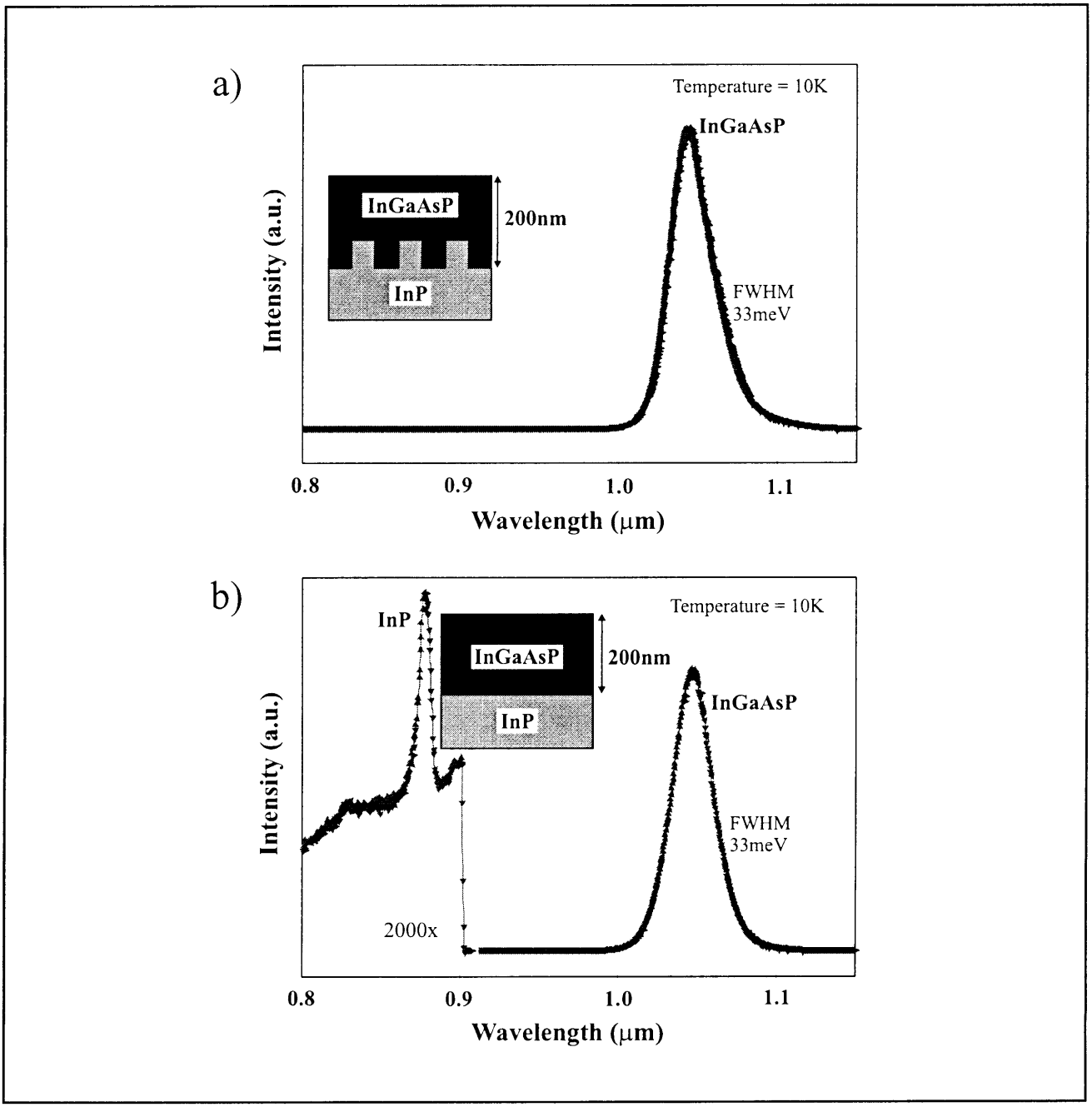

Figure 5. Photoluminescence spectra of a patterned surface overgrowth (a) and a bulk material growth (b), grown simultaneously, are comparable indicating the high quality of the InGaAsP deposited on the patterned InP surface.

optical communication networks. These devices and wavelength requirements can be met using InP-based materials, specifically the (In,Ga)(As,P) material system. The crystal growth technique that is employed to fabricate these devices is gas source molecular beam epitaxy (GSMBE). GSMBE combines the controllability of gaseous group V hydrides (AsH_3, PH_3) with the benefits of conventional MBE. This combination lends itself to the growth of multilayered structures, such as multiple quantum well (MQW) lasers and saturable Bragg reflectors (SBRs). In addition, GSMBE can be utilized for overgrowth of patterned surfaces to realize devices such as distributed feedback (DFB) lasers.

Periodic perturbations of the refractive index are a foundation for realizing single mode optical sources. In order to achieve the strongest possible refractive index perturbation, such as that required by DFB lasers and Bragg grating resonators, the periodic structure must reside within the device, necessitating epitaxial overgrowth. New oxide removal

techniques combined with GSMBE overgrowth of rectangular-patterned gratings are being investigated. Gratings, having a period of 240 nm, are patterned in both InP substrates and InGaAsP epilayers via x-ray lithography and reactive ion etching, achieving vertical sidewalls to depths of 80-110 nm. An atomic hydrogen source, residing within the epitaxial reactor, is employed to remove the oxide from the patterned surfaces. The atomic hydrogen-assisted oxide removal is performed below the growth temperature thereby reducing the amount of time that the patterned surface is at elevated temperatures in the absence of material deposition.

Techniques employed for characterizing the grating profile and epilayer include scanning and transmission electron microscopy, Nomarski interference-contrast microscopy, double crystal and triple axis x-ray diffraction, and photoluminescence. Triple axis x-ray results confirm the grating period and depth prior to overgrowth and also indicate the fidelity of the overgrown grating. X-ray measurements of an annealed InP grating (cycled through the growth process under a phosphorus overpressure) have also been performed. The comparison of the annealed grating with an overgrown InP grating indicates minimal grating degradation in the overgrown sample. In addition, the photoluminescence spectra, as shown in figure 5, indicate the high quality of the overgrown epilayer material.

A key component for the generation of ultrashort pulses in solid-state and fiber lasers is a saturable Bragg reflector (SBR). SBRs are passive devices comprised of a saturable absorption region integrated with a highly reflective mirror (a distributed Bragg reflector or DBR). The saturable absorption region of a SBR is typically one or two quantum wells placed within a quarter-wave layer of the DBR or within a half-wave layer on top of the DBR. The reflected intensity of this device, at the quantum well emission wavelength, can be varied based on the position of the quantum well within the DBR structure, e.g., the reflected intensity is highest if the quantum well is placed in the first quarter-wave layer, and decreases as the quantum well is placed further into the device. The quantum well should have an emission wavelength within the DBR reflectivity bandwidth in order to maximize the nonlinear reflectivity of the SBR that results from the nonlinear absorption of the quantum well. By placing the SBR in a low-gain solid-state laser cavity, its nonlinear reflectivity will mode-lock the laser with the result being self-starting, stable, ultrashort optical pulses.[15]

SBRs have been demonstrated in the 0.85 μm wavelength range by Tsuda, et al.,[15] and more recently in the 1.5 μm wavelength regime by Collings, et al.[16] and Hayduk, et al.[17] The devices operating in the 1.5 μm regime are inherently more difficult to produce. The least desirable method is to place an InGaAs saturable absorption region on an InGaAsP/InP mirror. While this design is desirable simply because it is InP-based, the complication resides in the large number of layers (~ 40 pairs) necessary for the highly reflective mirror. An alternative approach, as has been demonstrated by both Collings, et al. and Hayduk, et al. is to place the InGaAs saturable absorption region on a GaAs/AlAs mirror.[18] However, while this design requires a fewer number of layers for the highly reflective mirror, the mirror and the saturable absorption region are significantly lattice-mismatched.

The SBR design currently being developed is similar to that used by Collings, et al.[16] and is shown in figure 6. The GaAs/AlAs mirrors are first developed and optimized. The InP-based saturable absorption region is then integrated with an optimized GaAs/AlAs mirror via GSMBE regrowth techniques. Upon completion, the SBRs will be placed in both Cr^{4+}:YAG and fiber laser cavities.

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[15] S. Tsuda, W.H. Knox, E.A. de Souza, W.Y. Jan, and J.E. Cunningham, "Low-Loss Intracavity AlAs/AlGaAs Saturable Bragg Reflector for Femtosecond Mode Locking in Solid-State Lasers," *Opt. Lett.* 20(12): 1406-1408 (1995).

[16] B.C. Collings, J.B. Stark, S. Tsuda, W.H. Knox, J.E. Cunningham, W.Y. Jan, R. Pathak, and K. Bergman, "Saturable Bragg Reflector Self-Starting Passive Mode Locking of a Cr^{4+}:YAG Laser Pumped with a Diode-Pumped Nd:YVO_4 Laser," *Opt. Lett.* 21(15): 1171-1173 (1996).

[17] M.J. Hayduk, S.T. Johns, M.F. Krol, C.R. Pollock, and R.P. Leavitt, "Broadly Tunable Saturable Absorber Mode-Locked Cr^{4+}:YAG Femtosecond Laser," *Proceedings of the IEEE Lasers and Electro-Optics Society 1996 Annual Meeting*, Boston, Massachusetts, November 18, 1996.

[18] B.C. Collings, J.B. Stark, S. Tsuda, W.H. Knox, J.E. Cunningham, W.Y. Jan, R. Pathak, and K. Bergman, "Saturable Bragg Reflector Self-Starting Passive Mode Locking of a Cr^{4+}:YAG Laser Pumped with a Diode-Pumped Nd:YVO_4 Laser," *Opt. Lett.* 21(15): 1171-1173 (1996); M.J. Hayduk, S.T. Johns, M.F. Krol, C.R. Pollock, and R.P. Leavitt, "Broadly Tunable Saturable Absorber Mode-Locked Cr^{4+}:YAG Femtosecond Laser," *Proceedings of the IEEE Lasers and Electro-Optics Society 1996 Annual Meeting*, Boston, Massachusetts, November 18, 1996.

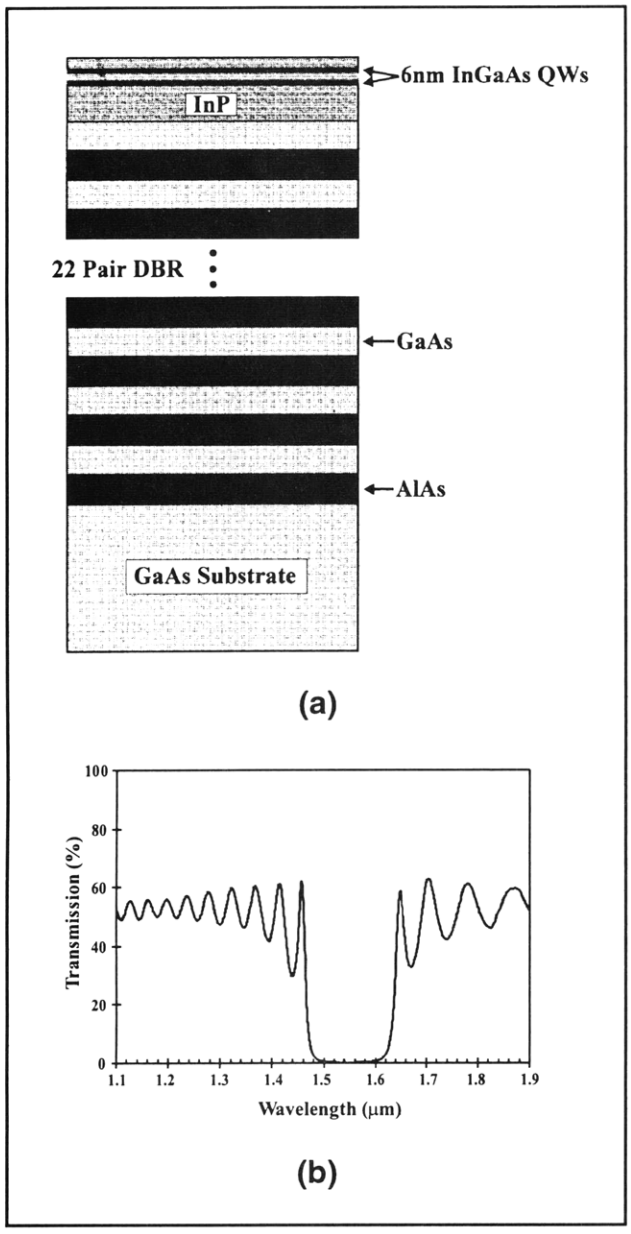

Figure 6. (a) A schematic of the saturable Bragg reflector (SBR), for operation at a wavelength of 1.55 μm, currently under investigation. (b) The transmission spectrum of the GaAs/AlAs distributed Bragg reflector centered at 1.55 μm. The DBR reflectivity is 99.85 percent at 1.55 μm.

3.6 (In,Ga)(As,P) Composition Control and Characterization

Sponsors

MIT Lincoln Laboratory
Contract BX-6085
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Project Staff

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The development of (In,Ga)(As,P) optoelectronic devices requires precise control of the material composition, the thickness, and the impurity doping levels for each layer. Typically, reflection high energy electron diffraction and optical pyrometry are used *in-situ* to monitor the material composition as well as the thickness of the deposited material, while techniques such as Hall Effect measurements are used *ex-situ* to characterize the carrier concentration within doped epitaxial layers. Currently, the use of a relatively new *in-situ* characterization method, spectroscopic ellipsometry, is being developed. In addition, Hall Effect measurements are being performed in order to calibrate the dopant cells in the gas source molecular beam epitaxy (GSMBE) system.

Inherent in the development of spectroscopic ellipsometry as an *in-situ* characterization technique is the promise of using spectroscopic ellipsometry as a real-time *in-situ* feedback control mechanism during the GSMBE growth of (In,Ga)(As,P) materials and devices. The use of spectroscopic ellipsometry as a feedback control mechanism for GSMBE growth will provide a means of minimizing the effects of growth uncertainties such as flux variations. Spectroscopic ellipsometry has been successfully used as an *in-situ* feedback control mechanism for metal organic chemical vapor deposition (MOCVD) of AlGaAs.[19] However, in addition to the challenge of applying this technique to the GSMBE growth method, the optical properties of $In_{1-x}Ga_xAs_yP_{1-y}$ are not well known at the temperatures required for GSMBE growth. Moreover, the possible variations in composition of the $In_{1-x}Ga_xAs_yP_{1-y}$ materials further complicate the

[19] S.C. Warnick, "Feedback Control of Organmetallic Vapor Phase Epitaxial Growth of Aluminum Gallium Arsenide Devices," S.M. thesis, *Dept. of Electr. Eng. And Comput. Sci.*, MIT, 1995.

real-time feedback control over that previously implemented for MOCVD of AlGaAs.[19]

In order to properly characterize the (In,Ga)(As,P) materials, spectroscopic ellipsometry measurements are being performed at various growth temperatures. Upon the completion of the extensive database, control theory algorithms that are currently being developed, will be employed to implement real-time feedback control. Future work will involve exploring methods of meeting device performance specifications in the presence of typical GSMBE growth uncertainties.

Also of importance to the performance of optoelectronic devices is the quality of the epitaxial material. The carrier mobility is often used as a figure of merit for gauging the material quality. In many devices, accurate carrier concentrations are needed to meet a particular design specification. Both the carrier concentration and mobility can be obtained *ex-situ* by Hall Effect measurements. To examine the quality of materials grown via GSMBE, sets of p-type, n-type, and undoped InP structures were grown. All of the structures grown thus far consist of 1.5 μm doped and unintentionally-doped InP epilayers deposited on semi-insulating, Fe-doped, InP substrates. Samples are prepared for Hall Effect measurements by first etching a clover leaf pattern into the epilayer with bromine:methanol (1:99). Metal contacts are then placed on the samples (In for n-type samples and InZn for p-type samples) and alloyed. Measurements are performed at room temperature. Electrical properties are then correlated to optical and microstructural properties via photoluminescence and x-ray diffraction.

3.7 Photonic Bandgap Structures

Sponsor

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This project represents the combined effort of the research groups led by Professors John D. Joannopoulos, Leslie A. Kolodziejski, Erich P. Ippen, and L. Rafael Reif. Professor Joannopoulos' group designs the structures and theoretically calculates the optical properties. Professor Kolodziejski's research group fabricates the one-dimensional structures in III-V compound semiconductors and the three-dimensional structures in Si/SiO_2 with Professor Reif providing expertise with the Si processing. Finally, the optical properties of the devices are measured by Professor Ippen's research group. The complexity of the design, fabrication and measurement of these structures necessitates a strong interaction between the various research groups.

A photonic crystal is a periodic dielectric structure that prevents photons within a certain range of frequencies from propagating. This forbidden band of frequencies translates into a photonic bandgap (PBG) analogous to an electronic bandgap in a semiconductor crystal. A defect state can also be introduced in the photonic bandgap when the dielectric periodicity of a photonic crystal is broken by the selective removal or addition of dielectric material. This defect results in the spatial localization of the defect mode into a volume of approximately one cubic wavelength, yielding a high-Q electromagnetic microcavity. The realization of such a microcavity holds the promise of vastly reducing the spontaneous emission and zero point fluctuations within an energy band.

A three-dimensional (3-D) photonic crystal requires a sophisticated geometry and an intricate arrangement of holes and rods to create a full bandgap. The complex structure does not easily lend itself to fabrication at submicron length scales. For example, the 3-D PBG structure that is under investigation, is constructed of three materials (Si, SiO_2, and air) and consists essentially of a layered structure in which a series of cylindrical air holes are etched at normal incidence through the top surface of the structure. Furthermore, most applications for photonic bandgap structures require bandgaps larger than 10 percent which, in turn, require the use of materials with a large index contrast such as in the case of Si and SiO_2. In the structure under fabrication, the photonic bandgap is as large as 14 percent of the midgap frequency using Si, SO_2 and air; and 23 percent using Si and air (after the SiO_2 is etched away). The structures that are being fabricated are designed to have a midgap frequency of 4.3 μm, 4.5 μm and 4.7 μm in both the Si/air system and the Si/SiO_2/air system. In order to allow for fabrication variations, the trench widths are varied from 90 percent to 110 percent of the optimum width, leading to a total of 18 different crystals being fabricated simultaneously onto a single Si wafer. Previously, three-dimensional PBG crystals have been constructed for operation in the

millimeter wave region,[20] and the fabrication of a two-dimensional PBG nanostructure has been reported.[21]

The fabrication process of three-dimensional photonic crystals consists of sequentially defining trenches in poly Si, filling the trenches with boron phosphide silicate glass (BPSG) and planarizing the surface using chemical-mechanical polishing (CMP). Prior to the etching of the poly Si trenches, a thin layer of Si_3N_4 and a layer of low temperature oxide (LTO) is deposited. The Si_3N_4 is used as an etch stop for the CMP, while the LTO is used as a hard mask for the trench definition. Figure 7 shows the poly Si trenches after being etched using Cl_2/HBr. Further refinements in the etching process are necessary to obtain a trench with a smoother bottom. After the BPSG deposition is used to fill the poly Si trenches with SiO_2, the surface is planarized. Figure 8 shows the completed first layer of a 3-D structure. The second layer is aligned to the first layer using alignment marks and Moire patterns. Figure 9a shows the second layer trenches aligned to the first layer; a schematic is shown in figure 9b.

Future work includes the completion of the seven layers that are needed in the three-dimensional photonic crystal using the existing contact masks and the verification of the photonic bandgap. When the deep-UV aligner in the Microsystems Technology Laboratory becomes operational, a new mask set for the deep-UV aligner will be designed and used for the next process run. Potential problems include the distortion of the crystal due to the stress in the multilayer poly-Si lines and the profile of the "final" holes that are etched through the structure.

The photonic bandgap air-bridge microcavity is essentially a one-dimensional photonic crystal made of III-V compound semiconductor material (refractive index, n ~ 2.9-3.3) surrounded by air (n = 1.0). The one-dimensional crystal comprises a semiconductor bridge that is punctuated with holes. These holes are situated periodically along the length of the bridge. A defect is introduced into the crystal by removing one of the holes. We have previously reported the successful fabrication of these structures using both silicon-based and III-V semiconductor material.[22] Since that report, we have proceeded to design and fabricate devices coupled with single-mode waveguides for measurement purposes. These photonic bandgap air-bridge devices have been designed to exhibit a photonic bandgap centered at a wavelength of 4.5 μm.

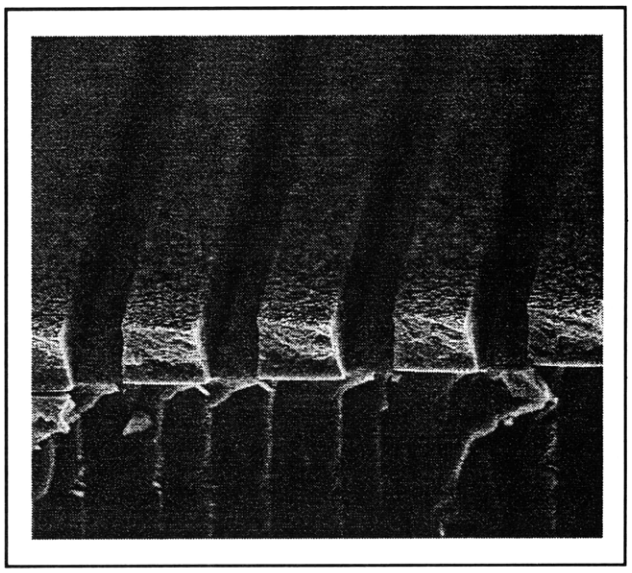

Figure 7. A scanning electron micrograph of the first layer trenches in poly silicon. The center-to-center distance between the trenches is 2.8 μm. The width and depth of the trenches are 1 μm and 0.8 μm respectively.

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[20] E. Özbay, E. Michel, G. Tuttle, R. Biswas, K.M. Ho, J. Bostak, and D.B. Bloom, "Double-Etch Geometry for Millimeter-Wave Photonic Band-Gap Crystals," *Appl. Phys. Lett.* 65(13): 1617-1619 (1994).

[21] P.L. Gourley, J.R. Wendt, G.A. Vawter, T.M. Brennan, and B.E. Hammons, "Optical Properties of Two-Dimensional Photonic Lattices Fabricated as Honeycomb Nanostructures in Compound Semiconductors," *Appl. Phys. Lett.* 64(6): 687-689 (1994).

[22] P.R. Villeneuve, S. Fan, J.D. Joannopoulos, K.Y. Lim, G.S. Petrich, L.A. Kolodziejski, and R. Reif, "Air-Bridge Microcavities," *Appl. Phys. Lett.* 67(2): 167-169 (1995).

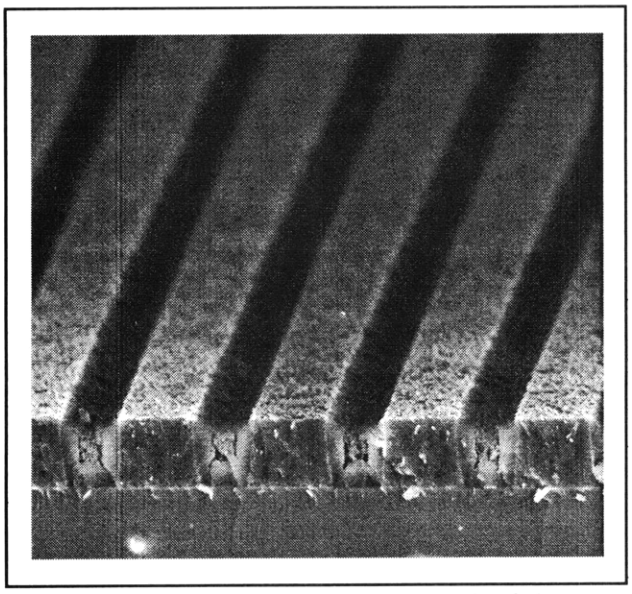

Figure 8. A scanning electron micrograph of the completed first layer of a three-dimensional photonic bandgap structure. The center-to-center distance between the trenches is 2.8 μm.

A typical one-dimensional device consists of a photonic bandgap air-bridge with waveguides feeding into and leading out of the air-bridge. The air-bridge material is GaAs and the structure is typically 14 μm long, 1.8 μm wide and 0.4 μm thick. The holes are 1.0 μm in diameter and are separated by 0.8 μm, yielding a period of 1.8 μm. The defect is 2.6 μm wide (measured center-to-center of the two holes bordering the defect). The waveguide material is also GaAs, but it has an upper cladding layer of $Al_{0.3}Ga_{0.7}As$ and a lower cladding layer of $Al_{0.7}Ga_{0.3}As$. The material configuration is designed to enhance the coupling of both the input beam from free space into the input waveguide, and from the input waveguide into the photonic bandgap air-bridge. Typically, both the upper and lower cladding layers are 0.2 μm-thick, and the tri-layer waveguide structure resides on a 4 μm $Al_{0.9}Ga_{0.1}As$ layer on a GaAs substrate.

The initial compound semiconductor material for the photonic bandgap air-bridge structure is grown by gas-source molecular beam epitaxy in the Chemical Beam Epitaxy Laboratory. A series of high-resolution photolithography, reactive ion etching, and wet chemical etching steps are then performed to fabricate the bridge and waveguide structures. These processing steps utilize the facilities in both the Microsystems Technology Laboratory and the

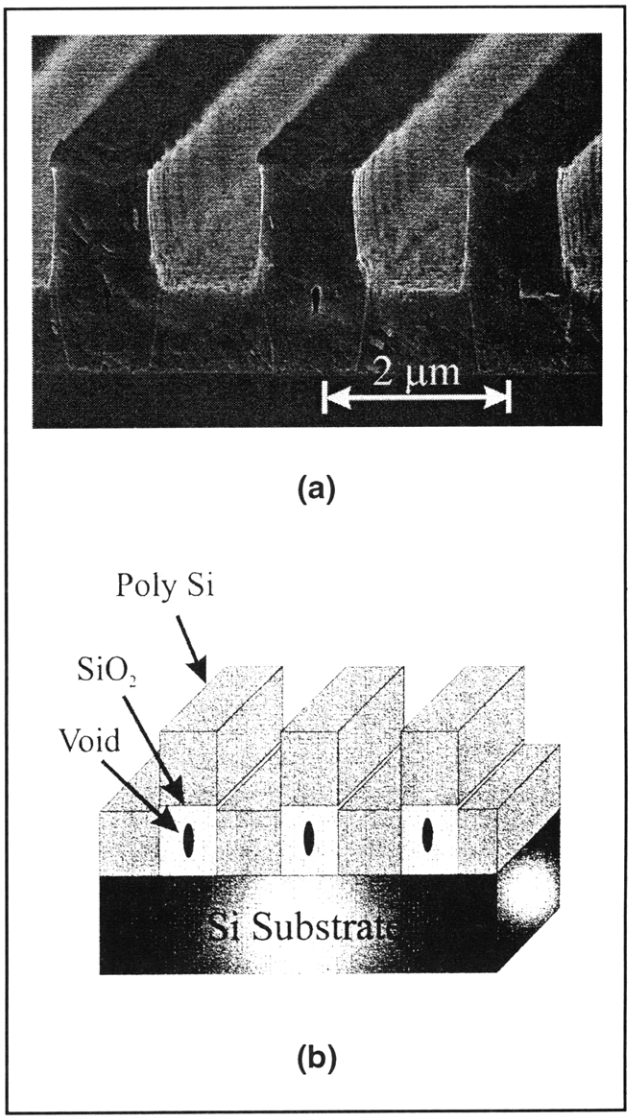

Figure 9. (a) A scanning electron micrograph of the second layer trenches aligned to the first layer of a three-dimensional photonic bandgap structure. The center-to-center distance between the trenches is 2 μm. The holes are in the first layer of SiO_2. (b) a schematic of the structure shown in (a).

Microelectronics Fabrication Laboratory in Building 13. We have successfully fabricated these devices and a scanning electron micrograph of such a device is shown in figure 10.

An experimental optical setup to measure and characterize the photonic bandgap air-bridge structure is under construction, and measurements will be performed in the near future in conjunction with Professor Erich P. Ippen's group.

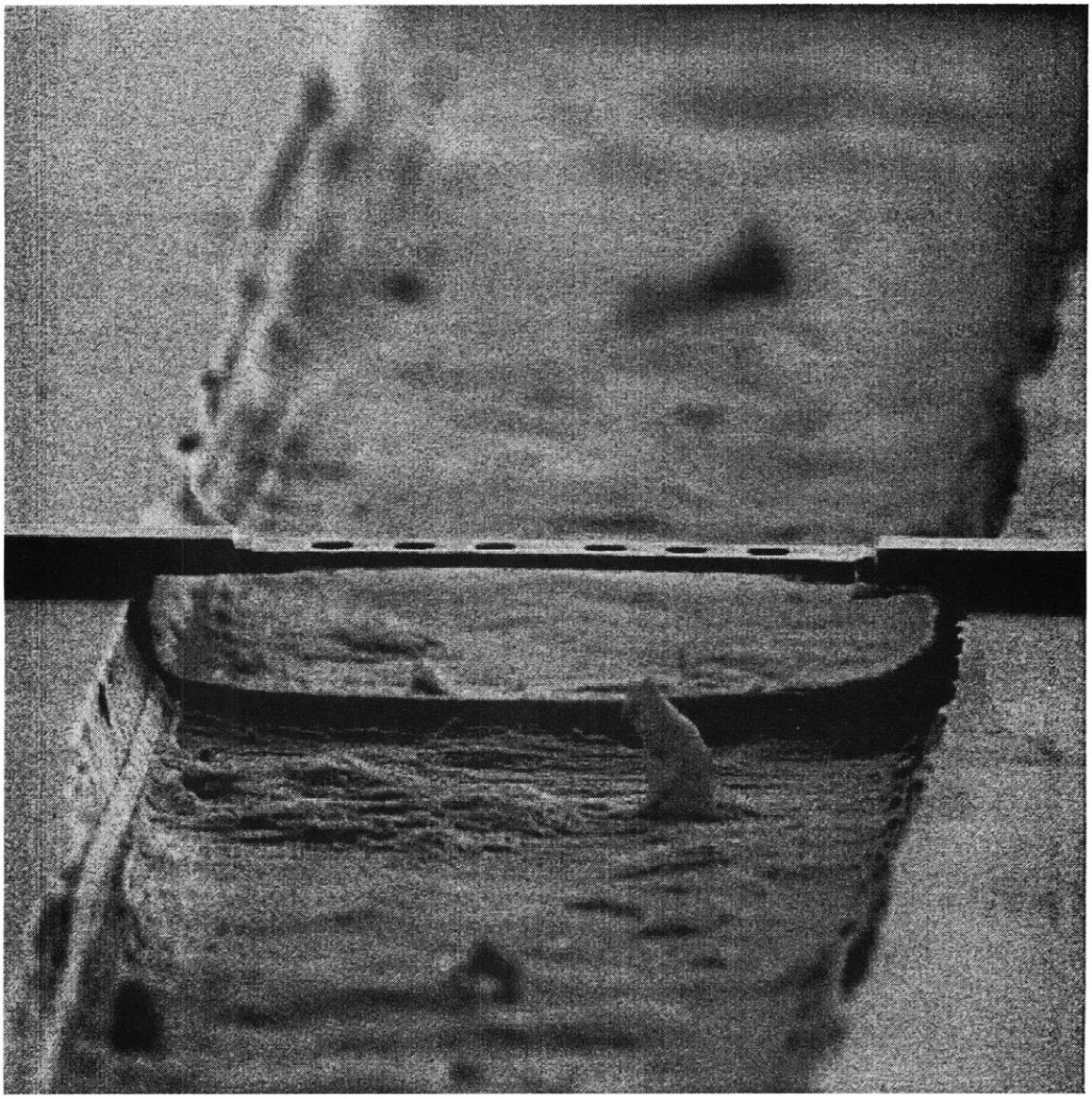

Figure 10. Scanning electron micrograph of a photonic bandgap air-bridge device coupled with input and output waveguides. The air-bridge is 1.8 μm wide, 0.4 μm thick and approximately 14 μm long. The holes are 1.0 μm in diameter and are separated by 0.8 μm. The defect region, in the middle of the air-bridge, is 2.6 μm wide (center-to-center). The 0.2 μm-thick upper cladding layer of the waveguide (absent from the bridge) is clearly visible.