Chapter 2. Physics of InAlAs/InGaAs Heterostructure Field-Effect Transistors

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2.1 Introduction

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The goal of this project is to develop InAlAs/InGaAs heterostructure field-effect transistors suitable for millimeter-wave high-power applications. The suitability of this material system for low-noise amplification is now unquestionable. Obtaining a high breakdown voltage is, however, still rather difficult, and it usually comes with severe trade offs. This fact seriously limits the suitability of this material system for high-power millimeter-wave applications.

Over the last few years, we have been engaged in research on how to improve the breakdown voltage of InAlAs/InGaAs HFETs, that is, the maximum voltage that the device can handle. Our work has provided technological design criteria that are now widely used in industry, such as employing AlAs-rich InAlAs pseudoinsulators[1] and carrying out selective recessed-mesa sidewall isolation.[2] We also recently identified the detailed physical mechanisms responsible for breakdown in InAlAs/n^+-InGaAs HFETs fabricated at MIT.[3] We found that the breakdown path involves two different processes in series. First, electron thermionic field emission takes place from the gate over the InAlAs barrier into the InGaAs channel. This is followed by hot electron relaxation in the channel with impact ionization of electron-hole pairs. More recently, in collaboration with Daimler-Benz in Ulm, Germany, we identified the same mechanisms in action in state-of-the-art InAlAs/InGaAs Modulation-Doped Field-Effect Transistors (MODFETs).[4] Finally, last year we identified the existence of substantial impact ionization in the channel of our own InAlAs/InGaAs HFETs under regular operating conditions. This is important for understanding noise in these devices.

In the last period of performance, we have developed S-passivation technology for InAlAs/InGaAs MODFETs, and we have integrated it into a complete 0.8 μm gate length device process. S passivation is claimed to reduce Fermi level pinning

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1 S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 38(9): 1986-1992 (1991).

2 S.R. Bahl and J.A. del Alamo, "Elimination of Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing," *IEEE Electron Dev. Lett.* 13(4): 195-197 (1992).

3 S.R. Bahl and J.A. del Alamo, "Physics of Breakdown in InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 41(12): 2268-2275 (1994).

4 S.R. Bahl, J.A. del Alamo, J. Dickmann, and S. Schildberg, "Off-State Breakdown in InAlAs/InGaAs MODFETs," *IEEE Trans. Electron Dev.* 42(1): 15-22 (1995).

at the surface of III-V compound semiconductors. There are two ways in which this could be exploited to improve the power handling capability of InAlAs/InGaAs MODFETs. First, if the Fermi level can be unpinned, S passivation at the exposed gap between the gate and the drain should smooth the electric field at the drain end of the channel. This ought to result in an improvement of the breakdown voltage. Furthermore, if S passivation is applied to the interface between an appropriate gate metal and the semiconductor, the Schottky barrier height of the gate could be improved. This should result in a reduction of gate leakage and an improvement of the breakdown voltage. Our first experimental results indicate modest improvements in the expected direction but it is yet unclear the physics that are at play. The following sections describe in more detail our technical findings and our key conclusions.

2.2 An Integratable S-passivation Process for the InAlAs/InGaAs System

For several years, the use of sulfur-containing compounds for the passivation of the surfaces of both GaAs and InP has received considerable attention. It has been demonstrated that treatment with sulfur-containing compounds prior to evaporation can yield substantial shifts in Schottky barrier height towards the ideal value dictated by the metal work function.[5] Recently, similar results were reported for Au Schottky barriers on InAlAs.[6] While these results offer great promise, it is unclear whether the improvement in Schottky barrier height on InAlAs is due to reduction in pinning, or to a shift in the position of the pinned Fermi level. Furthermore, the work reported previously has utilized aggressive surface cleans prior to sulfur treatment. An effective S passivation process that is suitable to integration with a complete HFET fabrication process has yet to be developed.

Based on a literature search, we selected $(NH_4)_2S_x$ as the most likely candidate for an integratable S treatment of the InAlAs surface. We first carried out two process compatibility tests that any integratable process had to meet:

- We measured the etch rate of $(NH_4)_2S_x$ on InAlAs, InGaAs and GaAs. InGaAs and GaAs exhibited minimal etch rates (less than 10 Å/hr). InAlAs was etched at a rate of about 100 Å/hr. These results are adequate for process integration.
- We established that the S treatment is compatible with conventional photolithography. No pattern degradation or adhesion difficulties were observed after $(NH_4)_2S_x$ treatment of a photoresist patterned wafer.

Following these process compatibility tests, we carried out an additional test to select the proper chemical treatment prior to $(NH_4)_2S_x$ application. We fabricated Van der Pauw structures in typical InAlAs/InGaAs MODFET heterostructures. These structures were subject to several pretreatments as summarized in table 1. In all cases, a selective succinic-acid based gate recess was performed just prior to S treatment as this is a key constrain in the process. In addition to a reference sample without S treatment, four different pretreatment processes were examined, as listed in table 1. The sheet carrier concentration before and after S passivation was measured for all samples.

The results summarized in table 1 indicate that the omission of a pretreatment before $(NH_4)_2S_x$ application resulted in the maximum change in the sheet carrier concentration (with respect to the reference sample) as a result of S passivation. The other approaches were much less effective. From a process integration point of view, this is also a favorable alternative because of its simplicity. In consequence we decided not to perform any pretreatment between succinic acid selective etching and $(NH_4)_2S_x$ application.

2.3 S-passivated InAlAs/InGaAs MODFETs

Having selected the process parameters of the S treatment, we proceeded to carry out a complete fabrication run of InAlAs/InGaAs MODFETs. The starting heterostructure is shown in figure 1. This heterostructure was designed in collaboration with Raytheon Research Division, and it was MBE-grown at Raytheon by Bill Hoke. This design incorporates a number of features that are targeted for power applications. First, it is a double-

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5 M.S. Carpenter, M.R. Melloch, and T.E. Dungan, "Schottky Barrier Formation on NH_4S-treated N- and P-type (100) GaAs," *App. Phys. Lett.* 53(1): 66-68 (1988); J. Fan, H. Oigawa, and Y. Nannichi, "Metal-dependent S-barrier Height with the $(NH_4)_2S_x$-treated GaAs," *Jap. J. App. Phys.* 27(11): L2125-2127 (1988).

6 N. Yoshida, M. Totsuka, J. Ino, and S. Matsumoto, "Surface Passivation of InAlAs using $(NH_4)_2S_x$ and P_2S_5/NH_4S," *Jap. J. App. Phys.* 33(3A) part 1: 1248 (1994).

Sample ID	*E*	*F*	*G*	*H*	*I*
Gate Recess	Succinic	Succinic	Succinic	Succinic	Succinic
Pre-Treatment	-	-	Semico Clean	5% NH_4OH	Dilute H_2SO_4:H_2O_2
$(NH_4)_2S_x$ Treatment	-	10 min.	10 min.	10 min.	10 min.
Relative change in sheet concentration ($\Delta n_s/n_s$)	- 2%	- 16%	- 6%	- 5%	- 3%

Table 1. Summary of process and sheet charge concentration results in five samples as a function of the chemical treatment applied prior to S passivation.

heterostructure with doping above and below the channel. Second, we used delta-doping on both layers. Third, we incorporated a thin undoped cap that is to be selectively etched. Our insulator is thicker than usual, 300 Å, in order to obtain a high breakdown voltage. The channel is thick so as to get high transconductance and low output conductance and therefore high gain.

Our process is standard. We use SiN_x-assisted liftoff for all our metal layers with the exception of the pads which are performed using chlorobenzene. The ohmic contacts are made by rapid-thermally annealing a AuGe bilayer. Before S treatment and gate evaporation, we perform selective mesa sidewall recessing to eliminate a very deleterious

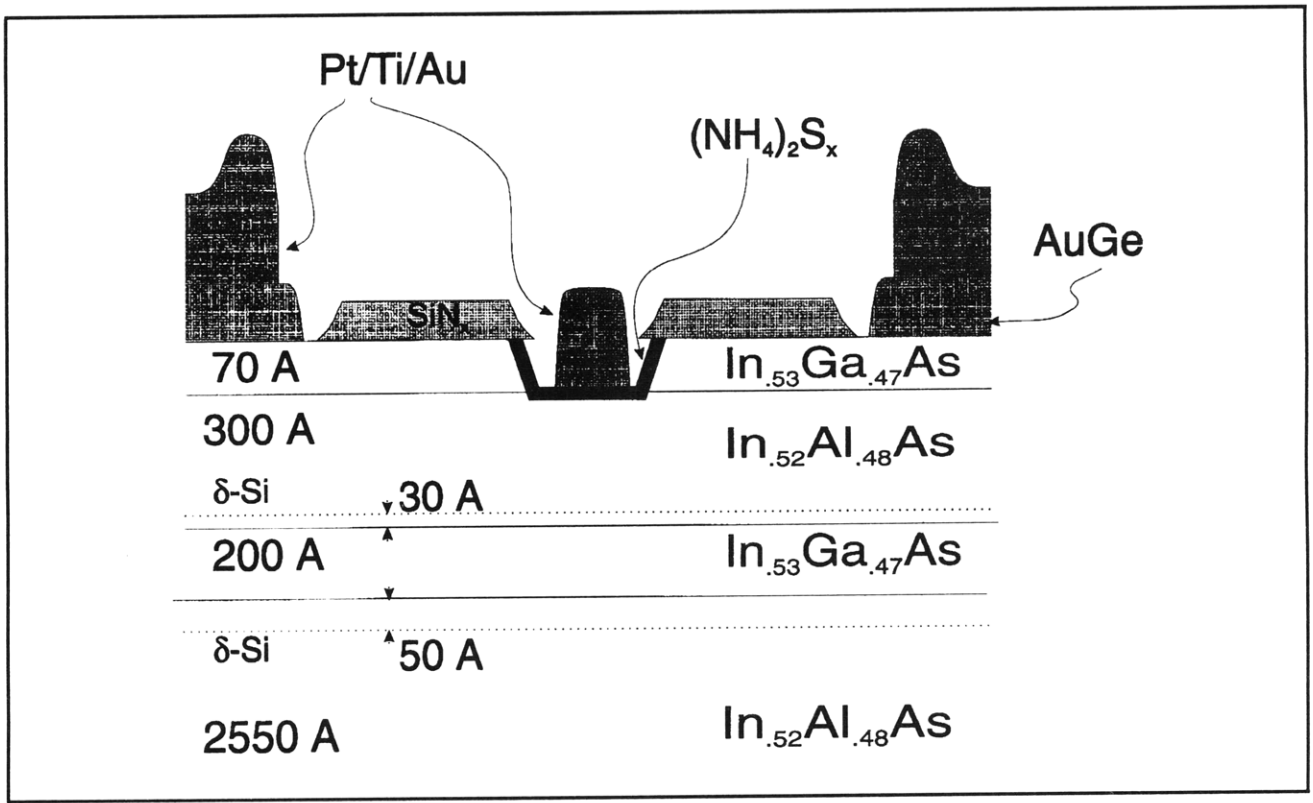


Figure 1. Schematic cross-section of fabricated modulation-doped field-effect transistor. The heterostructure was grown at Raytheon Research Division by Bill Hoke.

leakage path between the gate and the channel.[7] For this we use a succinic acid solution. This simultaneously etches in a selective way the InGaAs cap in the intrinsic portion of the device exposing the InAlAs insulator. The sample was cleaved at this point into two pieces. One half underwent the S treatment presented in the previous section. The second half was a reference sample that followed a conventional 5 percent NH_4OH pre-gate treatment. Both halves were joined again for gate evaporation. This consisted of a Pt/Ti/Au stack. The process finished with the evaporation and lift-off of Ti/Au pads.

Devices with gate lengths 0.8 μm long and 50 μm wide have been tested. Typical output characteristics of a S-treated device are shown in figure 2. Qualitatively, they do not differ much from the untreated devices. A summary of average values of important figures of merit for both technologies is listed in table 2. Mean values for the maximum current that these devices can handle are 450 and 475 mA/mm, for the S-treated and untreated devices respectively. A plot of transconductance and drain current versus V_{GS} is shown in figure 3 for different values of V_{DS}. The average peak transconductance of the S-treated devices is 440 mS/mm. This contrasts with an average value of 380 mS/mm for the reference devices. This significant improvement in g_m could be explained by a slight etching of the InAlAs insulator or by the elimination of a surface oxide that is unavoidably present between the gate and the InAlAs insulator in conventional processing. In fact, the threshold voltage has shifted slightly from -0.7 V to -0.55 V as a result of the treatment.

Sample ID	*No Sulfur*	*Sulfur*
$\langle V_T \rangle$	-0.7 V	-0.55 V
$\langle g_{m\text{-}peak} \rangle$	380 mS/mm	440 mS/mm
$\langle I_{DSS} \rangle$	475 mA/mm	450 mA/mm
$\langle BV_{DS} \rangle$	7.5 V	8.3 V

Table 2. Summary of MODFET results for S-treated and reference devices with L_g = 0.8 μm and W_g = 50 μm.

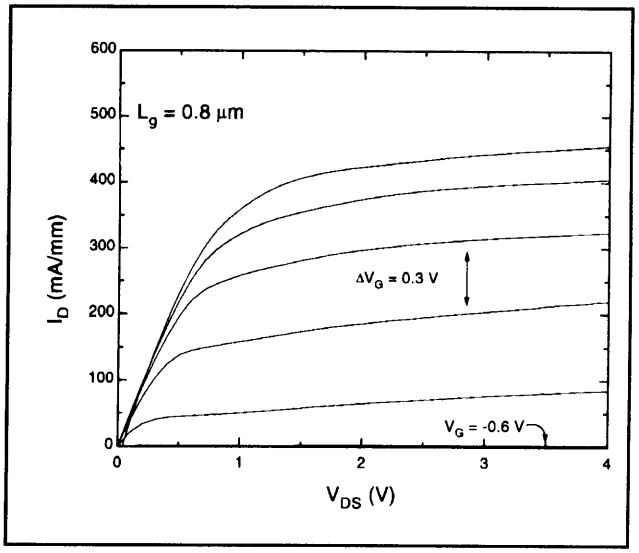


Figure 2. Output characteristics of a S-treated L_g = 0.8 μm, W_g = 50 μm MODFET.

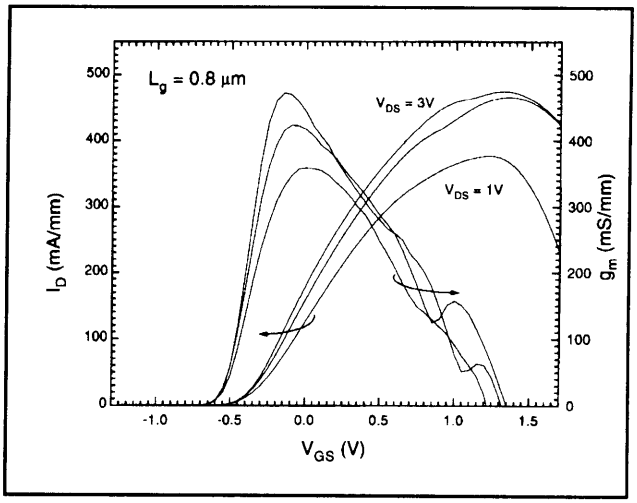


Figure 3. Plot of transconductance and drain current vs. V_{GS} for a S-treated L_g = 0.8 μm, W_g = 50 μm MODFET for three values of V_{DS}.

In spite of this, the breakdown voltage of these devices is excellent. We have measured an average off-state three-terminal breakdown voltage of 7.5 V in the conventional device (defined at a current of 1 mA/mm). For the S-treated device, this value improved to 8.3 V. Figure 4 shows a plot of the drain-current injection technique[8] applied to a S-treated device. A three-terminal breakdown voltage in excess of 8 V is obtained.

[7] S.R. Bahl and J.A. del Alamo, "Elimination of Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing," *IEEE Electron Dev. Lett.* 13(4): 195-197 (1992).

[8] S.R. Bahl and J.A. del Alamo, "A New Drain-Current Injection Technique for the Measurement of Breakdown Voltage in FETs," *IEEE Trans. Electron Dev.* 40(8): 1558-1560 (1993).

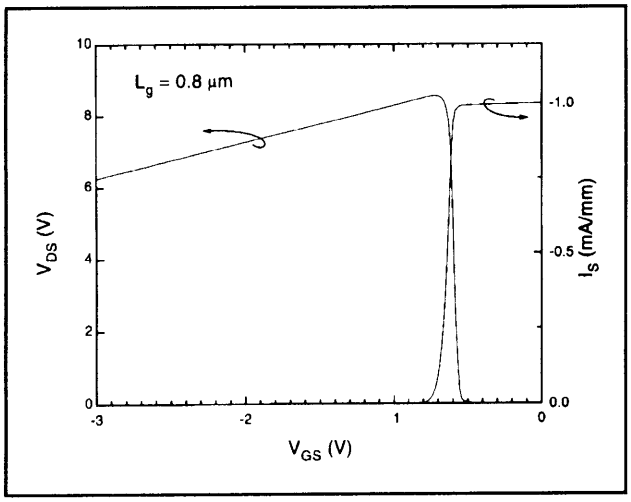


Figure 4. Plot of V_{DS} and I_S versus V_{GS} for I_D = 1 mA/mm for a S-treated L_g = 0.8 μm, W_g = 50 μm MODFET showing a three-terminal breakdown voltage in excess of 8 V.

A detailed analysis of the impact of S passivation is currently under way. Our preliminary results indicate that S passivation improves the transconductance and the breakdown voltage of the device while it slightly degrades the maximum current drivability. In the near future, we will carry out detailed C-V characteristics of gate diodes so as to understand the charge control in the intrinsic portion of the device. We will also measure high-frequency S-parameters.

2.4 Publications and Conference Papers

Bahl, S.R., and J.A. del Alamo. "Physics of Breakdown in InAlAs/n$^+$-InGaAs Heterostructure Field-Effect Transistors." *IEEE Trans. Electron Dev.* 41(12): 2268-2275 (1994).

Berthold, G., M. Mastrapasqua, C. Canali, M. Manfredi, E. Zanoni, S.R. Bahl, and J.A. del Alamo. "Electron and Hole Real Space Transfer in InAlAs/InGaAs Heterostructure Device." *Proceedings of the 24th European Solid State Device Research Conference.* Eds. C. Hill and P. Ashburn. Editions Frontieres. Edinburgh, United Kingdom, September 11-15, 1994. pp. 631-634.

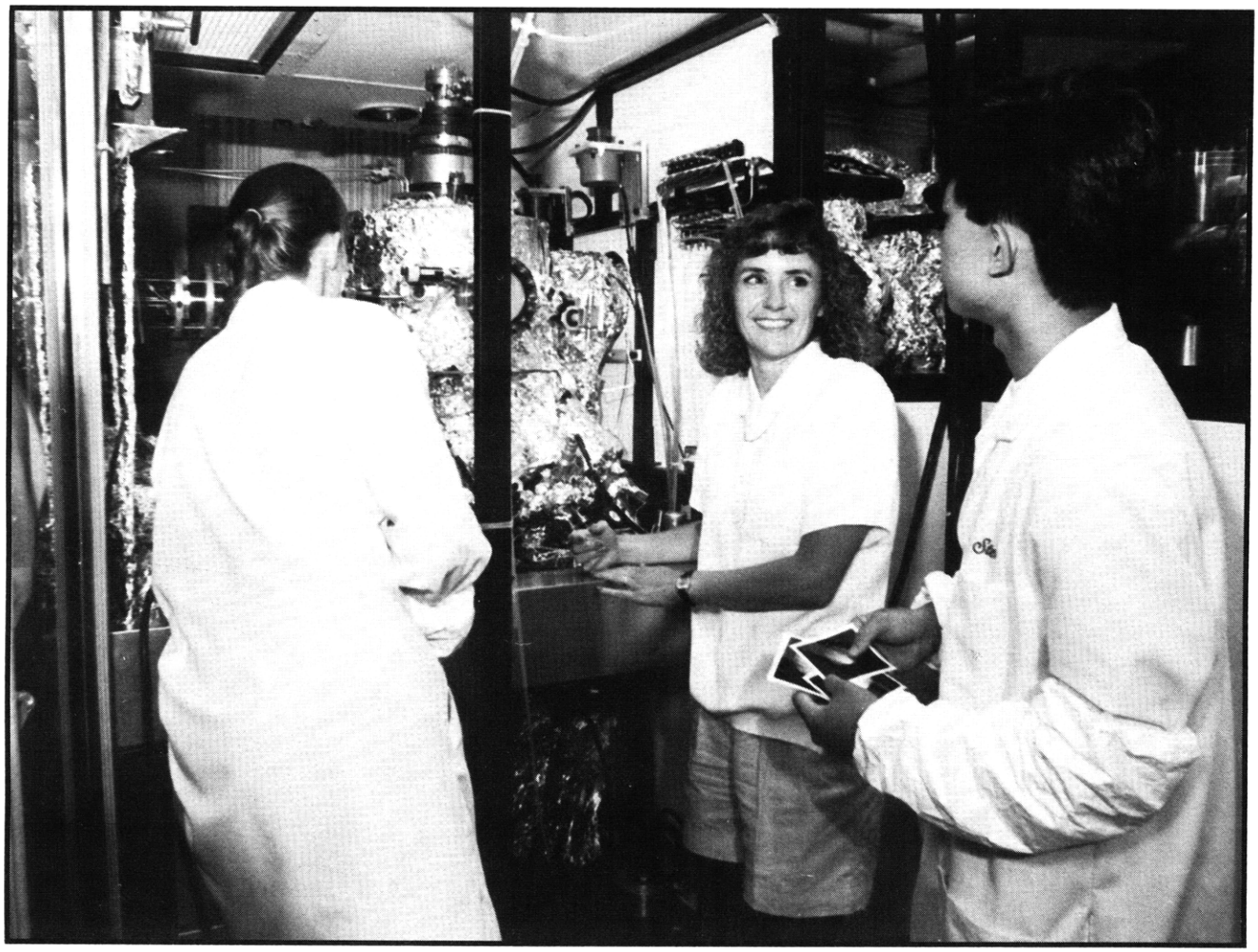
Berthold, G., E. Zanoni, M. Manfredi, M. Pavesi, C. Canali, J.A. del Alamo, and S.R. Bahl. "Electroluminescence and Gate Current Components of InAlAs/InGaAs HFETs." 52nd Annual Device Research Conference, Boulder, Colorado, June 20-22, 1994.

Moolji, A.A., S.R. Bahl, and J.A. del Alamo. "Impact Ionization in InAlAs/InGaAs HFETs." *IEEE Electron Dev. Lett.* 15(8): 313-315 (1994).

Theses

Adams, T. *Gate Delay in InP Heterostructure Field-Effect Transistors.* B.S. thesis. Dept. of Electr. Eng. and Comput. Sci., MIT, 1994.

Reiner, J.W. *A Small-Signal Model for Surface Effects in InAlAs/InGaAs HFETs.* B.S. thesis. Dept. of Electr. Eng. and Comput. Sci., MIT, 1994.



From left: graduate student Jody L. House, Professor Leslie A. Kolodziejski, and graduate student Kuo-Yi Lim (Photo by John F. Cook)