Chapter 2. Physics of InAlAs/InGaAs Heterostructure Field-Effect Transistors

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2.1 Introduction

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The goal of this project is to explore the suitability of InAlAs/InGaAs heterostructure field-effect transistors for power applications at very high frequencies. This material system has recently emerged as a promising candidate for low-noise applications at ultra-high frequencies where world record results have been demonstrated.[1] Unfortunately, before InAlAs/InGaAs HFETs can also be used for high-frequency *power* applications, the physics of the breakdown voltage of these devices needs to be better understood. This has been the objective of our project for the last few years.

Over the last few years, we have been studying ways to improve the breakdown voltage of InAlAs/InGaAs HFETs, that is, the maximum voltage that the device can handle. Our work has resulted in technological design criteria such as employing AlAs-rich InAlAs pseudoinsulators[2] and carrying out selective recessed-mesa sidewall isolation[3] that are now widely used in industry. Two years ago we identified the detailed physical mechanisms responsible for breakdown in InAlAs/n^+-InGaAs HFETs fabricated at MIT.[4] We found that the breakdown path involves two different processes in series. First, electron thermionic field emission takes place from the gate over the InAlAs barrier into the InGaAs channel. This is followed by hot electron relaxation in the channel with impact ionization of electron-hole pairs.

Over the last year, in collaboration with the Daimler-Benz Research Center in Ulm, Germany, we have been studying the physics of breakdown in state-of-the-art quarter-micron gate length InAlAs/InGaAs modulation-doped field-effect transistors (MODFETs) fabricated at Daimler Benz. To our surprise, we found that the physics of breakdown in these devices is qualitatively identical to that of MIT's InAlAs/n^+-InGaAs HFETs in spite of the radically different geometries and layer structure. There were important *quantitative* differences which help us trace the origin of the chronically low break-

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[1] L.D. Nguyen, L.E. Larson, and U.K. Mishra, "Ultra-High-Speed Modulation-Doped Field-Effect Transistors: A Tutorial Review," *Proc. IEEE* 80(4): 494-518 (1992).

[2] S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+-In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Devices* 38(9): 1986-1992 (1991).

[3] S.R. Bahl and J.A. del Alamo, "Elimination of Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing," *IEEE Electron Device Lett.* 13(4): 195-197 (1992).

[4] S.R. Bahl and J.A. del Alamo, "Physics of Breakdown in InAlAs/n^+-InGaAs HFETs," *Proceedings of the Fifth International Conference on Indium Phosphide and Related Materials,* Paris, France, April 18-22, 1993.

down voltage of MODFETs in this material system. In a separate effort, we have also studied the occurrence of impact ionization in InAlAs/n^+-InGaAs HFETs under regular operating conditions, that is, with the channel on and away from breakdown. We indeed found that substantial impact ionization is taking place in these devices at typical operating biases. This is important for low-noise microwave and photonic applications where excess gate current due to hole generation in the channel is a serious noise contribution. The following sections describe in more detail our technical findings and conclusions.

2.2 Physics of Breakdown in InAlAs/InGaAs MODFETs

In collaboration with Daimler-Benz Research Center, we have performed the first comprehensive experimental study of off-state breakdown in InAlAs/InGaAs MODFETs. The heterostructure of these devices is shown in figure 1. The cap was designed to be surface-depleted for higher breakdown voltage. Three different heterostructures were characterized in this study, with different InAs mole-fractions of x=0.53 (lattice-matched), x=0.62, and x=0.70 in the channel. For the device with x=0.70, the lower 250 Å of the channel was grown with a lattice-matching composition of x=0.53 to avoid excessive strain. Processing was carried out according to the sequence described in Dickmann et al.[5] The cap was etched selectively, and mesa-sidewall isolation was used in all heterostructures as we originally proposed in 1992.[6]

MODFETs with L_G =0.28 μm and W_G=80 μm were characterized. For reference, the lattice-matched device had I_D(max)=275 mA/mm, g_m(peak)=400 mS/mm, f_t =83 GHz, and f_{max} =140 GHz. These are excellent values for devices with high BV. In this study, both drain-source breakdown voltage, BV_{DS}, and drain-gate breakdown voltage, BV_{DG}, were measured at several temperatures using the drain-current injection technique we have innovated.[7] The test current was 1 mA/mm.

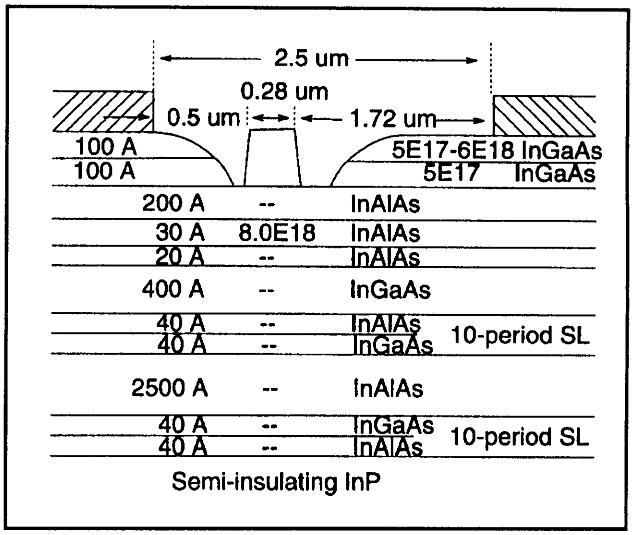

Figure 1. Schematic cross-section of heterostructure. Three structures were grown with InAs-mole fraction, x=0.53, 0.62, and 0.70 in the channel.

A plot of BV_{DS} and BV_{DG} versus T is presented in figure 2. At 300 K, BV_{DS} was 8.9 V, 6.3 V, and 5.1 V for x=0.53, 0.60, and 0.70 respectively. These are very high values for InAlAs/InGaAs MODFETs. In all devices, BV_{DS} and BV_{DG} show a negative temperature coefficient. The drain-current injection technique indicated that V_{DS} is limited by gate breakdown for the entire range of temperatures in all devices. BV_{DS} and BV_{DG} track each other with a difference of about V_T, consistent with the above finding. BV_{DS} increases from 7.9 V at 340K to 14.4 V at 220 K for x=0.53. Since impact-ionization has a positive temperature coefficient, it follows that breakdown cannot be a simple impact-ionization phenomenon, as might be expected for a narrow bandgap channel with long mean-free path.

We also investigated the temperature dependence of the gate current approaching breakdown. I_G was found to be thermally activated around room-temperature. Figure 3 shows an Arrhenius plot of I_G/T^2 at V_{DG}=4 V for the three devices. It is clear that as x is increased in the channel, I_G increases and E_A is reduced. For V_{DG}=4 V, E_A is 0.17 eV, 0.09 eV, and 0.06 eV for x=0.53, 0.62, and 0.70 respectively.

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[5] J. Dickmann, K. Riepe, H. Haspeklo, B. Maile, H. Daembkes, H. Nickel, R. Losch, W. Schlapp, "Novel Fabrication Process for Si_3N_4 passivated InAlAs/InGaAs/InP HFETs," *Electron. Lett.* 12: 1849 (1992).

[6] S.R. Bahl and J.A. del Alamo, "Elimination of Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing," *IEEE Electron Device Lett.* 13(4): 195-197 (1992).

[7] S.R. Bahl and J.A. del Alamo, "A New Drain-Current Injection Technique for the Measurement of Breakdown Voltage in FETs," *IEEE Trans. Electron Devices* 40(8): 1558-1560 (1993).

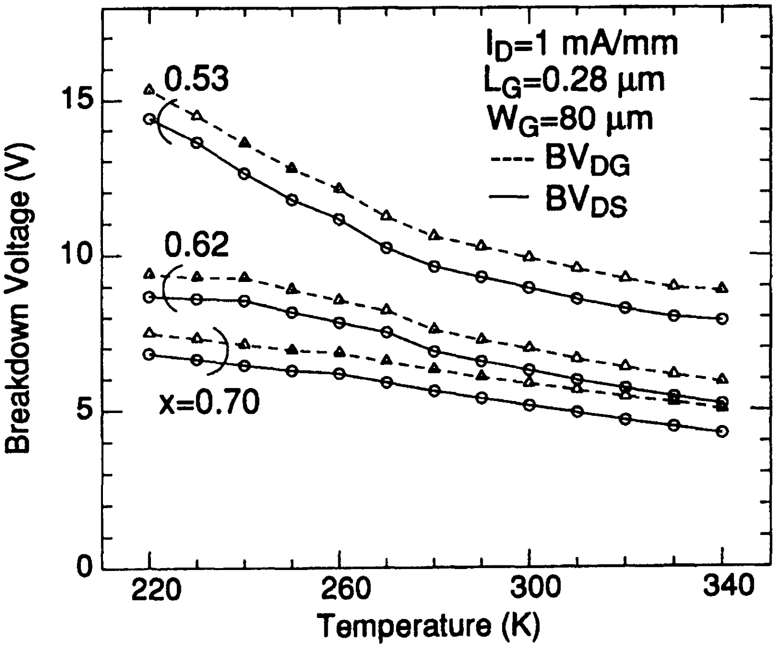

Figure 2. Drain-source and drain-gate breakdown voltages BV_{DS} and BV_{DG} vs. temperature as a function of InAs mole fraction, x, in the channel.

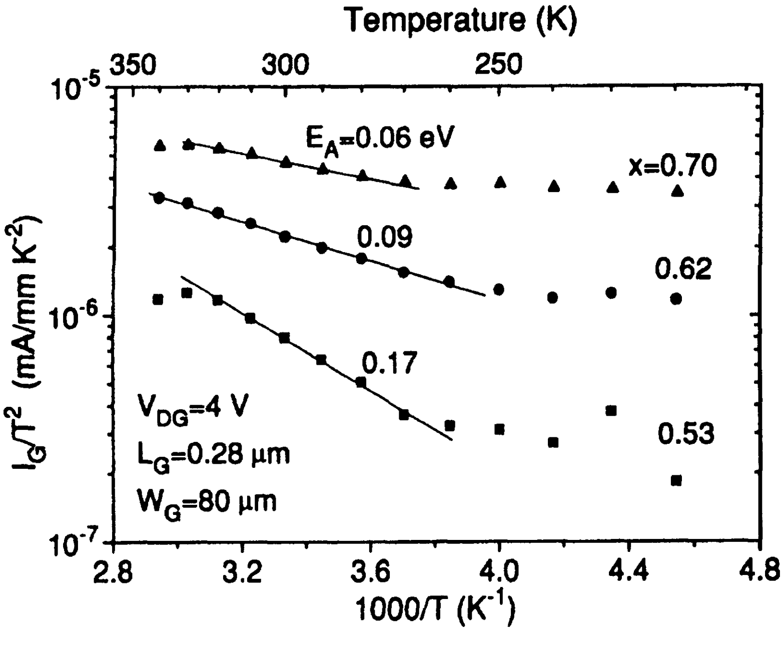

Figure 3. An Arrhenius plot of log(I_G/T^2) vs. 1000/T for V_{DG}= 4 V, as a function of x.

In a side-gate measurement, we verified that holes are produced in the channel at breakdown. Since specially designed sidegate structures did not exist in this wafer, this measurement was carried out by positioning a probe very close to the drain of the device and applying a reverse voltage of -80 V. In this manner, the probe was able to capture a few holes generated in the channel.

All these findings are qualitatively identical to those that we previously obtained on InAlAs/n^+-InGaAs HFETs.[8] This is rather remarkable since the present devices differ considerably from those in Bahl and del Alamo[8] in their much shorter gate-length, different cap design, the presence of dopants in the insulator, the absence of dopants in the channel, Si_3N_4 passivation, incorporation of gate-recessing, and different buffer-layer. The similitude of experimental observations regarding off-state breakdown in such dissimilar devices reveals how fundamentally the breakdown process is associated with the materials involved.

The thermionic-field emission/Auger-generation hypothesis we proposed for the InAlAs/n^+-InGaAs HFET[8] can explain all the findings for the MODFET. Essentially, electrons going from the InAlAs insulator to the InGaAs channel suddenly gain a kinetic energy equal to ΔE_c from the conduction-band step. This is in addition to the energy they already acquired from the electric-field in the insulator. For $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$, $\Delta Ec = 0.5$ eV, which is a substantial fraction of the bandgap of $In_{0.53}Ga_{0.47}As$ (0.73 eV). In this case, even the presence of a low electric-field in the insulator can give rise to impact-ionization in the channel.

The combined thermionic emission/-Auger-generation process, shown schematically in figure 4a, is a two-step process. First, electrons are injected from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, and immediately relax their energy through impact-ionization. The electrons flow towards the drain, and the holes can either be extracted by the gate or flow towards the source, where they recombine with electrons. This process actually occurs in two-dimensions, with electron injection likely to take place sideways from the gate into the drain-gate gap, as illustrated in a two-dimensional sketch in figure 4b.

The physical understanding gained in the course of this work provides for design criteria for future improvements in the off-state breakdown voltage of InAlAs/InGaAs MODFETs for the first time. Specifically, our findings now explain the need for an insulator that has the largest possible Schottky barrier. This barrier suppresses electron thermionic-field emission and improves breakdown. Second, the bandgap in the channel must not be too narrow since it facilitates Auger generation of electrons and holes. As a third conclusion, correct engineering of the cap also impacts breakdown because it affects

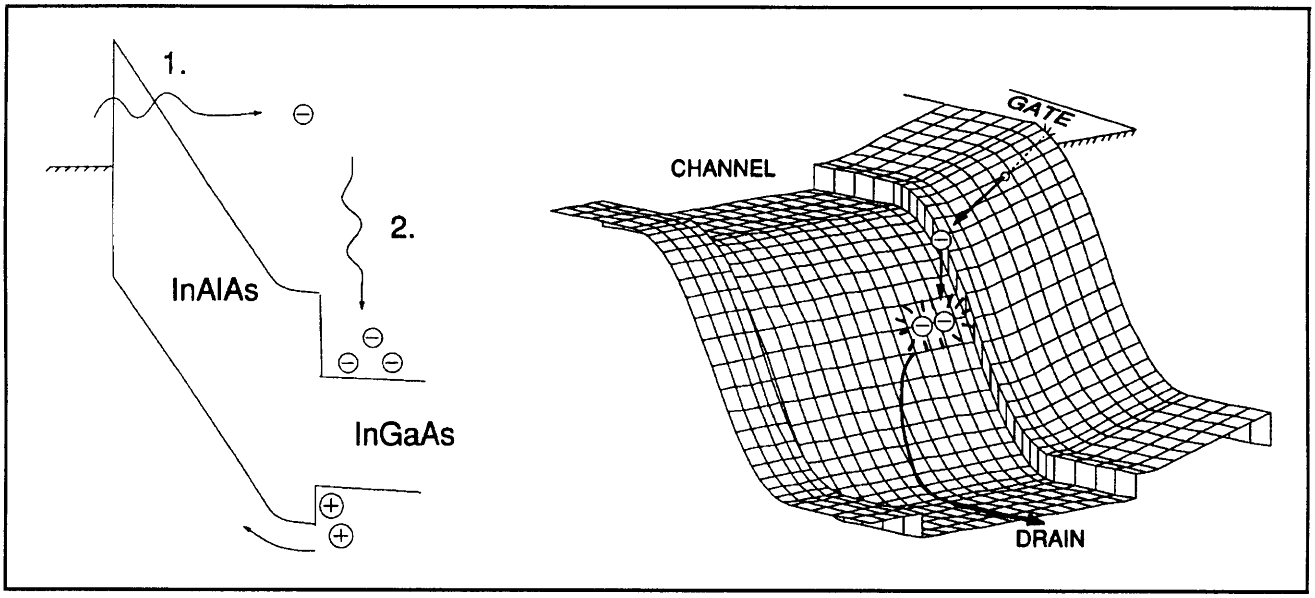

Figure 4. A schematic diagram showing the combined effect of electron thermionic-field emission and Auger generation. (a) Basic mechanism, (b) two-dimensional drawing. Electrons are injected sideways through thermionic-field emission from the gate into the high-field drain-gate region of the insulator (step 1). They then enter the channel hot and impact-ionize by Auger generation (step 2).

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[8] S.R. Bahl and J.A. del Alamo, "Physics of Breakdown in InAlAs/n^+-InGaAs HFETs," *Proceedings of the Fifth International Conference on Indium Phosphide and Related Materials,* Paris, France, April 18-22, 1993.

the electric field distribution directly underneath the gate edge on the drain-end of the channel where electron injection from the gate to the channel takes place.

We now understand the reason for the superior breakdown voltage characteristics of the MIDFET (metal-insulator-doped channel FET), that we have been studying at MIT, over the more popular MODFET. The presence of dopants inside the insulator of the MODFET bends the bands sharply down underneath the gate, favoring thermionic field emission of electrons at lower energies. In the MIDFET, the absence of dopants in the insulator results in a more "squarish" barrier relatively suppressing electron emission out of the gate. This explains the drastically different activation energies obtained in both kinds of devices, about 0.1 eV for the MODFET versus 0.45 eV for the MIDFET.[8]

2.3 Impact Ionization in InAlAs/InGaAs HFETs

We have examined the occurrence of impact ionization in the channel of InAlAs/n^+-InGaAs HFETs fabricated at MIT[9] under regular biasing conditions, that is, with the channel turned on and away from breakdown conditions. Impact ionization in the channel results in excessive shot noise in the drain current and in additional gate leakage current which compromises the sensitivity of photonic receivers based on these devices.

We carried out sidegate current measurements on specially designed HFETs on a heterostructure studied previously (figure 5).[10] By applying a sufficiently negative bias to the sidegate contact (-20 V in this experiment), it is possible to remove a small fraction of the holes that might be produced in the HFET channel as a result of impact ionization. We analyze the sidegate current in a similar manner as Hui et al.[11] which dealt with the gate current of MESFETs. In our case, the gate current is not a good indicator of impact ionization because of the barrier that the insulator presents to the holes in the channel (the valence band discontinuity between insulator and channel which is about 0.2 eV).

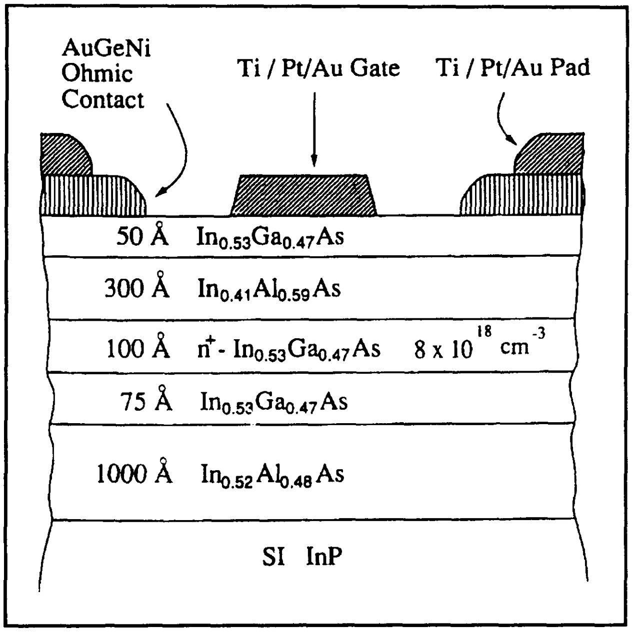

Figure 5. Schematic cross-section of InAlAs/n^+-InGaAs HFET used in the study of impact ionization in the on-regime.

Following the approach of Hui et al., we plot the absolute magnitude of the sidegate current (minus a small baseline electron leakage current through the gate) over the drain current as a function of the inverse voltage drop at the drain-end of the channel. A straight line in a semilog plot that is independent of V_{GS} is the key signature of impact ionization.[11] Indeed, as figure 6 shows, this is what we observe in our devices. This study unmistakeably shows that impact ionization is taking place in the channel of InAlAs/InGaAs HFETs under a variety of bias conditions. This important fact needs to be taken into consideration when designing circuit applications around these devices, particularly, low-noise amplifiers for microwave or photonic applications.

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[9] S.R. Bahl, B.R. Bennett, and J.A. del Alamo, "Doubly-Strained $In_{0.41}Al_{0.59}As/n^+-In_{0.65}Ga_{0.35}As$ HFET with High Breakdown Voltage," *IEEE Electron Device Lett.* 14(1): 22-24 (1993).

[10] S.R. Bahl, B.R. Bennett, and J.A. del Alamo, "A High-Voltage, Doubly-Strained $In_{0.41}Al_{0.59}As/n^+-In_{0.65}Ga_{0.35}As$ HFET," *Proceedings of the Fourth International Conference on InP and Related Materials,* Newport, Rhode Island, April 20-24, 1992.

[11] K. Hui, C. Hu, P. George, and P.K. Ko, "Impact Ionization in GaAs MESFETs," *IEEE Electron Device Lett.* 11: 113 (1990).

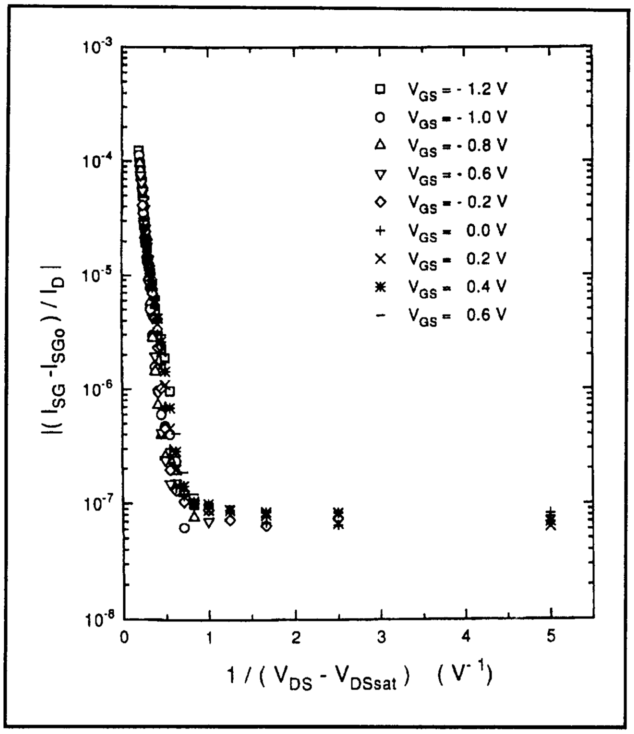

Figure 6. Semilog graph of sidegate current over drain current versus inverse voltage drop at the drain-end of the channel. The bunching of data in a straight line independent of V_{GS} indicates the occurrence of impact ionization in the channel.

2.4 Publications and Conference Papers

Bahl, S.R., B.R. Bennett, and J.A. del Alamo. "Doubly-Strained $In_{0.41}Al_{0.59}As/n^+\text{-}In_{0.65}Ga_{0.35}As$ HFET with High Breakdown Voltage." *IEEE Electron Device Lett.* 14(1): 22-24 (1993).

Bahl, S.R., and J.A. del Alamo. "A New Drain-Current Injection Technique for the Measurement of Breakdown Voltage in FETs." *IEEE Trans. Electron Devices* 40(8): 1558-1560 (1993).

Bahl, S.R., and J.A. del Alamo. "Physics of Breakdown in InAlAs/n^+-InGaAs HFETs." *Proceedings of the Fifth International Conference on Indium Phosphide and Related Materials,* Paris, France, April 18-22, 1993.

Bahl, S.R., J.A. del Alamo, J. Dickmann, and S. Schildberg. "Physics of Breakdown in InAlAs/InGaAs MODFETs." *51st Annual Device Research Conference,* Santa Barbara, California, June 21-June 23, 1993; *IEEE Trans. Electron Devices* 40(11): 2110-2111 (1993).

del Alamo, J.A., and S. Bahl. "InAlAs/InGaAs HFETs with High Breakdown Voltage." *17th European Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE),* Parma, Italy, May 31-June 2, 1993.

Dickmann, J., S. Schildberg, H. Dambkes, S.R. Bahl, and J.A. del Alamo. "Characterization of the Breakdown Behavior of Pseudomorphic InAlAs/$In_xGa_{1-x}As$/InP HEMTs with High Breakdown Voltages." *Proceedings of the 20th International Symposium on Gallium Arsenide and Related Compounds,* Freiburg, Germany, August 29-September 2, 1993. Forthcoming.

Dumas, J.M., P. Audren, M.P. Favennec, D. Lecrosnier, S.R. Bahl, and J.A. del Alamo. "An Investigation of Deep Levels in InAlAs/n^+-InGaAs Heterostructure FETs." *Proceedings of the Fifth International Conference on Indium Phosphide and Related Materials,* Paris, France, April 18-22, 1993.

Theses

Bahl, S.R. *Physics and Technology of InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors.* Ph.D. diss., Dept. of Electr. Eng. and Comput. Sci., MIT, February 1993.

Moolji, A.A. *Regimes of Operation of InAlAs/n^+-InGaAs HFETs.* S.B. thesis, Dept. of Electr. Eng. and Comput. Sci., MIT, June 1993.