Chapter 2. High-Frequency InAlAs/InGaAs Metal-Insulator-Doped Semiconductor Field-Effect Transistors (MIDFETs) for Telecommunications

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2.1 Introduction

Sponsors

Charles S. Draper Laboratories
  Contract DL-H-441694
Fujitsu Laboratories
Joint Services Electronics Program
  Contract DAAL03-92-C-0001
Texas Instruments

The goal of this project is to investigate InAlAs/n^+-InGaAs Metal-Insulator-Doped channel Field-Effect Transistors (MIDFETs) on InP. These devices are of great interest for applications in long-wavelength lightwave communication systems and ultra-high frequency high-power microwave telecommunications.

InAlAs/InGaAs Modulation-Doped Field-Effect Transistors (MODFETs) on InP represent a promising choice for a variety of microwave and photonics applications. The outstanding transport properties of InGaAs have yielded devices with very low-noise and high-frequency characteristics.[2] Unfortunately, the low breakdown voltage of InAlAs/InGaAs MODFETs on InP (typically less than 5 V) severely restricts their use in medium- and high-power applications.[2] Additionally, in InP photonics receivers based on Metal-Semiconductor-Metal (MSM) photodiodes, one must use a separate high voltage supply to operate the photodetectors because they typically require several volts across them to achieve a high-quantum efficiency.[3]

A device strategy with great potential for power handling is the InAlAs/n^+-InGaAs MIDFET featuring an undoped insulator and a thin, heavily-doped channel.[4] Our research over the last few years at MIT on the physics and technology of this device has revealed that its breakdown voltage, V_B, is large and can be engineered using pseudomorphic

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1 Fujitsu Laboratories, Atsugi, Japan.

2 L.D. Nguyen, L.E. Larson, and U.K. Mishra, "Ultra-High-Speed Modulation-Doped Field-Effect Transistors: A Tutorial Review," *Proc. IEEE* 80(4): 494-518 (1992).

3 J.H. Burroughes and M. Hargis, "1.3 μm InGaAs MSM Photodetector with Abrupt InGaAs/InAlAs Interface," *IEEE Phot. Tech. Lett.* 3(6): 532 (1991).

4 J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET with a Heavily-Doped Channel," *IEEE Electron Device Lett.* EDL-8(11): 534-536 (1987).

insulators[5] and quantized channels.[6] This is in addition to having a comparable frequency response to MODFETs of similar gate lengths.[7]

During 1992, we investigated the physics of breakdown in InAlAs/n^+-InGaAs MIDFETs. We developed a hypothesis for the breakdown mechanism in this device that explains our experimental observations to date. We verified our hypothesis by carrying out detailed breakdown measurements as a function of temperature. Our work required the development of a breakdown measuring technique that was unambiguous, safe, and reliable. The following sections describe in greater detail our technical findings and conclusions.

2.2 Drain-current Injection Technique for the Measurement of Breakdown Voltage

Precise knowledge of the breakdown voltage, V_B, of a device, including an unambiguous definition of breakdown and a reliable and safe measuring technique, is essential for application of a device in a circuit environment. However, the FET literature contains many inconsistent definitions of breakdown. In addition, most measuring techniques are ambiguous, not amenable to automation, and can easily result in device destruction. In this section, a new technique of measuring the breakdown voltage of FETs is presented. Its application to InAlAs/n^+-InGaAs MIDFETs is demonstrated.

This new technique, *drain-current injection technique*, uses a semiconductor parameter analyzer HP4145B with the device biased in a configuration schematically illustrated in figure 1. To measure breakdown, a fixed predefined current is injected into the drain, the gate-source voltage is ramped down from a strong forward bias to below threshold, and V_{DS} and I_G are monitored. In this manner, the device goes from the linear regime through the saturation region and into breakdown. This is analogous to tracing the locus of V_{DS} versus V_{GS} at a fixed I_D on the output I-V characteristics. As illustrated below, the *drain-source breakdown voltage* $V_{B(D-S)}$ is the peak drain-source voltage obtained in this scan, and the *drain-gate breakdown voltage* $V_{B(D-G)}$ is the drain-gate voltage at $I_G = -I_D$.

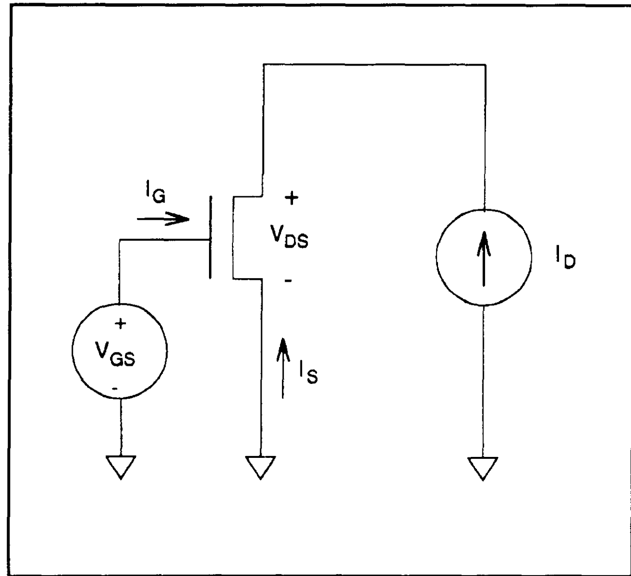

Figure 1. Schematic circuit diagram for implementation of the drain-current injection technique for measuring breakdown voltage in FETs.

We illustrate this technique on one of our devices in figure 2, which is a plot of V_{DS}, V_{DG}, and I_G versus V_{GS} for $I_D = 1$ mA/mm at room temperature. For values of V_{GS} above $V_t = -0.6$V, both V_{DS} and V_{DG} are relatively small and $I_G \approx 0$. At V_{GS} around V_t, both V_{DS} and V_{DG} rise sharply and I_G starts becoming significant. At about $V_{GS} = -1$ V, V_{DS} peaks. This is the drain-to-source breakdown voltage of the device. At a more negative V_{GS}, I_G becomes 1 mA/mm, and the source current becomes zero. This defines the drain-to-gate breakdown voltage $V_{B(D-G)}$. Because of the well-defined nature of these two critical voltage points, they can be extracted using a computer, making this technique easily automatable.

Our drain-current injection technique also provides insight into the physics of breakdown. This is discussed in more detail in the next section of this chapter. Figure 2 shows that when this particular device reaches breakdown, the source current goes to zero and V_{DG} saturates. This shows that the device breakdown is being governed by a drain-to-

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5 S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+-In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 38 (9): 1986-1992 (1991).

6 S.R. Bahl and J.A. del Alamo, "Breakdown Voltage Enhancement from Channel Quantization in InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors," *IEEE Electron Dev. Lett.* 13(2): 123-125 (1992).

7 S.R. Bahl, B.R. Bennett, and J.A. del Alamo, "Doubly-Strained $In_{0.41}Al_{0.59}As/n^+-In_{0.65}Ga_{0.35}As$ HFET with High Breakdown Voltage," *IEEE Electron Dev. Lett.* 14(1): 22-24 (1993).

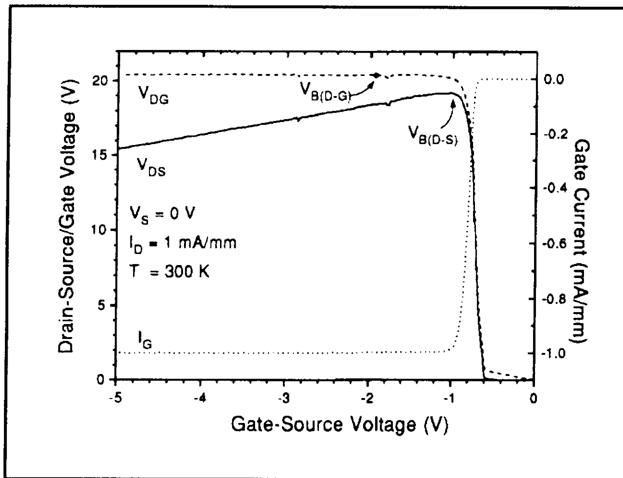

Figure 2. Illustration of drain-current injection technique in InAlAs/n+-InGaAs HFET: V_{DG}, V_{DS}, and I_G versus V_{GS}. The peak of V_{DS} is $V_{B(D-S)}$, and the point at which $I_G = 1$mA/mm is $V_{B(D-G)}$.

gate breakdown mechanism rather than by a channel or source-to-drain breakdown phenomenon. This is not always the case, and, in fact, at very low temperatures, most of our devices are governed by a channel breakdown mechanism.

To conclude this section, we have presented a new method of measuring the breakdown voltage in FETs. This simple technique provides unambiguous determination of $V_{B(D-S)}$ and $V_{B(D-G)}$. The current through the device is limited to a prespecified value so that risk to fragile devices is minimized.

2.3 Physics of Breakdown in InAlAs/n+-InGaAs HFETs

We have performed a detailed study of the physics of breakdown of InAlAs/n+-InGaAs MIDFETs. In brief, our research reveals that, similar to heterojunction avalanche photodiodes, breakdown in these devices is a two-step process (see figure 3). First, electrons are injected from the gate into the channel through thermionic emission or thermionic-field emission. Second, the electrons entering the channel are very hot and release their energy in an impact-ionization process which starts avalanche breakdown in the channel. This hypothesis explains our experimental observations to date and also the low breakdown voltage of InAlAs/InGaAs MODFETs.

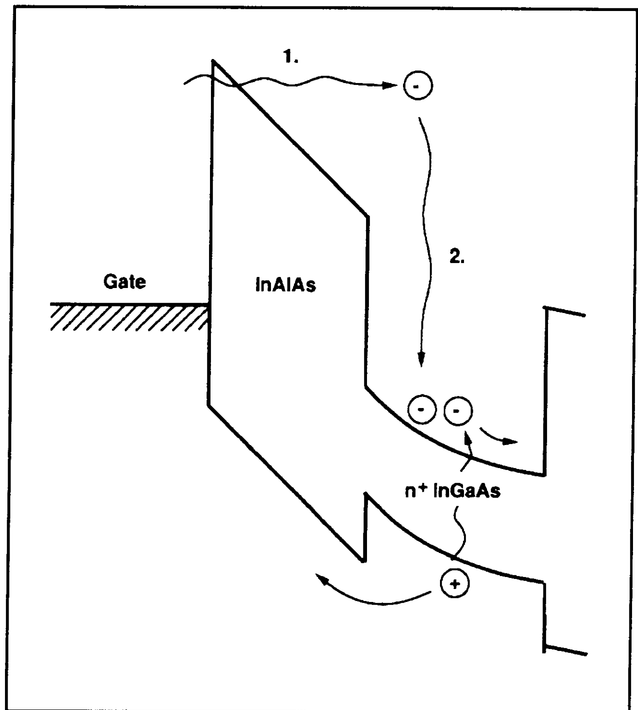

Figure 3. Schematic illustration of the postulated breakdown process in InAlAs/n+-InGaAs MIDFETs. With a strong reverse bias between the gate and the drain, hot-electrons are injected from the gate to the channel through a thermionic or thermionic-field emission process (step 1), and, as they relax in the channel, they cause impact-ionization in the channel (step 2).

The devices used in this study are based on a MBE-grown heterostructure on S.I.-InP. As shown in figure 4, their structure consists of (bottom to top), a 1000 Å $In_{0.52}Al_{0.48}As$ buffer, a 75 Å $In_{0.53}Ga_{0.47}As$ subchannel, a 100 Å n+ (4×10^{18} cm^{-3}) – $In_{0.53}Ga_{0.47}As$ channel, a 300 Å undoped $In_{0.41}Al_{0.59}As$ insulator, and a 50 Å undoped $In_{0.53}Ga_{0.47}As$ cap.[8] HFETs with $L_g = 1.9$ μm and $W_g = 30$ μm were studied. Both drain-source breakdown voltage, $V_{B(D-S)}$, and drain-gate breakdown voltage, $V_{B(D-G)}$, were measured using the drain-current injection technique presented in the previous section as a function of temperature.

At approximately room temperature, the breakdown voltages show a negative temperature coefficient with $V_{B(D-G)}$ increasing from 12.8 V at 360 K to 24.7 V at 260 K (see figure 5). $V_{B(D-S)}$ tracks $V_{B(D-G)}$, and increases from 11.1 V to 23.5 V. Measurements of I_G showed that for the temperature range 260 K-360 K at drain-source breakdown, all the

[8] S.R. Bahl, B.R. Bennett, and J.A. del Alamo, "A High-Voltage, Doubly-Strained $In_{0.41}Al_{0.59}As$/n+-$In_{0.65}Ga_{0.35}As$ HFET," paper presented at the Fourth International Conference on InP and Related Materials, Newport, Rhode Island, April 20-24, 1992, pp. 222-225.

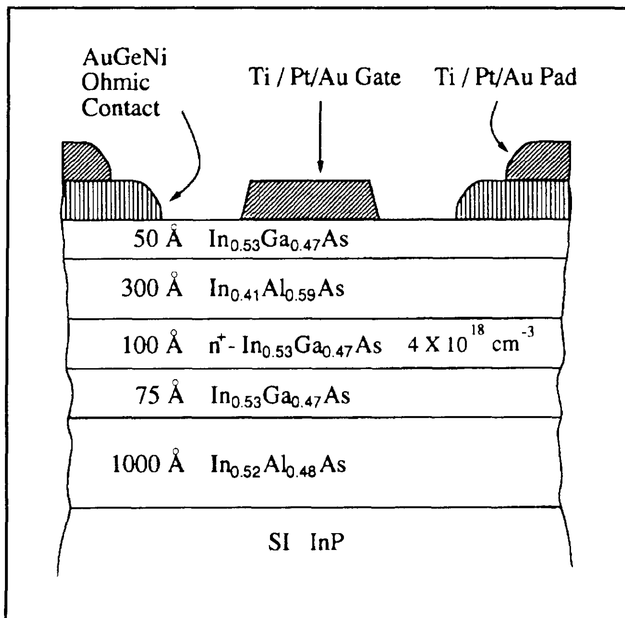

Figure 4. Schematic of device heterostructure used in our breakdown studies.

injected current flows from drain to gate (see figure 5). At these temperatures, drain-gate breakdown limits the value of the drain-source breakdown voltage. The temperature dependence that is measured is also incompatible with a simple impact ionization process in the channel.

To understand the relevant physics, we examined in detail the temperature dependence of I_G at the onset of breakdown. An Arrhenius plot of $\ln(I_G/T^2)$ was generated for V_{DG} steps from below V_T (-0.8 V) through $V_{B(D-G)}$ at 300 K (16 V), as shown in figure 6. Data from the locus of the drain-current injection technique ($I_D = 1$ mA/mm) was used. The gate current was found to be thermally activated with an activation energy of 0.41-0.46 eV, regardless of V_{DG}. This value is consistent with electron thermionic-field emission across the barrier as the breakdown limiting mechanism. The relatively constant activation energy exhibited from below threshold until breakdown implies that the voltage supported by the insulator does not change once the channel has been depleted. Instead, the excess voltage is supported by the lateral fields in the drain-gate gap. Measurements using a gated Hall-bar structure (essentially a long gate-length FET with taps directly into the channel) confirmed this hypothesis.

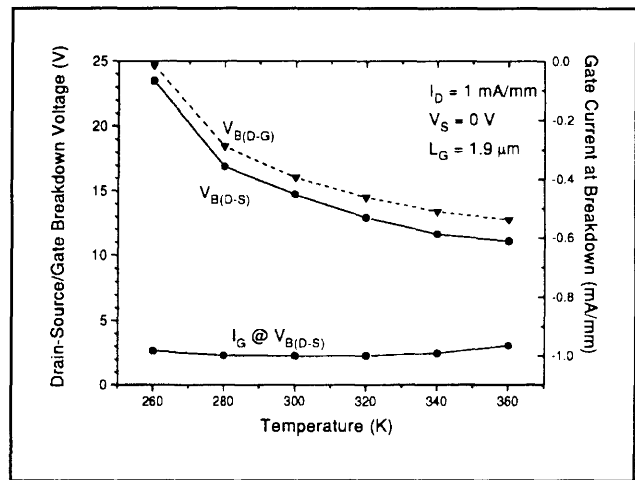

Figure 5. Drain-to-source breakdown voltage, drain-to-gate breakdown voltage, and gate current at drain-to-source breakdown voltage versus temperature.

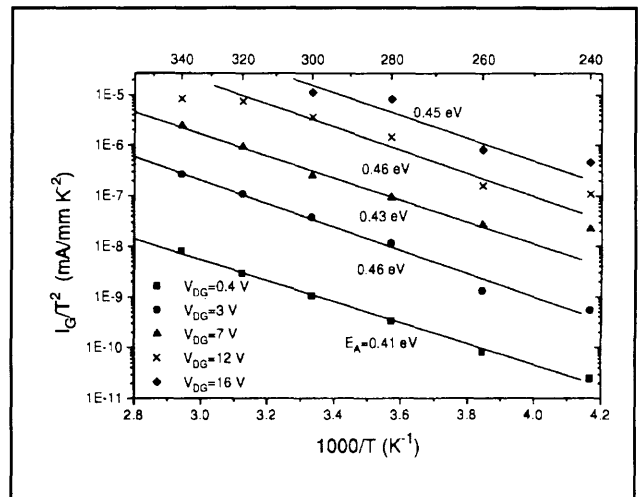

Figure 6. Arrhenius plot of gate current as a function of V_{DG}. The corresponding activation energy is indicated in the diagram.

The simultaneous occurrence of impact-ionization was established by detecting holes directly with a negatively biased sidegate in a specially designed structure, as shown in figure 7. The drain-current injection technique at $I_D = 1$ mA/mm was used, and the sidegate and gate currents monitored. The rise and saturation of the sidegate current coincides with the rise and saturation of the drain-gate voltage and drain-gate current. Since a very negative voltage has been applied to the sidegate, only holes can contribute to the sidegate current. This observation therefore verifies the occurrence of hole generation in the channel in an impact ionization process.

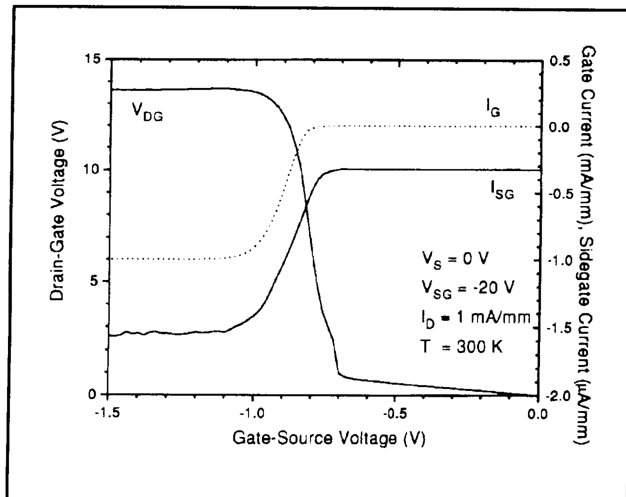

Figure 7. Sidegate current I_{SG}, gate current, and V_{DG} as a function of V_{GS} in a sidegate structure for $I_D = 1$mA/mm. The correlation between I_{SG} and I_G for $V_{SG} = -20$ V unmistakably indicates the existence of holes in the channel.

Our hypothesis, pictorially sumarized in figure 3, explains our previously observed results which show that both the insulator and channel parameters affect V_B. V_B increases if (1) the Schottky barrier height of the insulator is enhanced[9] (lower thermionic emission), (2) the channel bandgap is enlarged[10] (lower multiplication), and (3) the channel doping is decreased[11] (decreased thermionic emission resulting from a higher voltage across the insulator at threshold). Now our hypothesis can be used as a guiding principle for further improvements of the breakdown voltage of InAlAs/n^+-InGaAs MIDFETs.

A combination of thermionic (field) emission and impact-ionization is also likely to limit the breakdown voltage in InAlAs/InGaAs MODFETs, since in these devices, doping the insulator results in a reduced barrier to electron flow. This might pose a fundamental limit to the engineering of InAlAs/InGaAs MODFET breakdown voltages.

2.4 Publications and Conference Papers

Bahl, S.R., B.R. Bennett, and J.A. del Alamo. "Doubly-Strained InAlAs/n^+-InGaAs HFETs." Paper presented at the 1992 Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), San Antonio, Texas, February 16-19, 1992. Unpublished.

Bahl, S.R., B.R. Bennett, and J.A. del Alamo. "High Quality Heterostructures for Doubly-Strained InAlAs/InGaAs HFETs." Paper presented at the Seventh New England MBE Workshop, Cambridge, Massachusetts, May 13, 1992. Unpublished.

Bahl, S.R., B.R. Bennett, and J.A. del Alamo. "A High-Voltage, Doubly-Strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET." Paper presented at the Fourth International Conference on InP and Related Materials, Newport, Rhode Island, April 20-24, 1992, pp. 222-225.

Bahl, S.R., and J.A. del Alamo. "Elimination of Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing." *IEEE Electron Dev. Lett.* 13(4): 195-197 (1992).

Bahl, S.R., and J.A. del Alamo. "Breakdown Voltage Enhancement from Channel Quantization in InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors." *IEEE Electron Dev. Lett.* 13(2): 123-125 (1992).

Bahl, S.R., M.H. Leary, and J.A. del Alamo. "Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructure Field-Effect Transistors." *IEEE Trans. Electron Dev.* 39(9): 2037-2043 (1992).

del Alamo, J.A., S.R. Bahl, and D.R. Greenberg. "InP-Based High Breakdown Voltage HFETs." Paper presented at the Advanced Heterostructure Transistors Conference, Keauhou-Kona, Hawaii, November 29-December 4, 1992. Unpublished.

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[9] S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 38 (9): 1986-1992 (1991).

[10] S.R. Bahl and J.A. del Alamo, "Breakdown Voltage Enhancement from Channel Quantization in InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors," *IEEE Electron Dev. Lett.* 13(2): 123-125 (1992); S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100.

[11] S.R. Bahl, B.R. Bennett, and J.A. del Alamo, "A High-Voltage, Doubly-Strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET," paper presented at the Fourth International Conference on InP and Related Materials, Newport, Rhode Island, April 20-24, 1992, pp. 222-225.

Dumas, J.M., P. Audren, M.P. Favennec, S. Praquin, S.R. Bahl, and J.A. del Alamo. "Une Etude des Niveaux Profonds dand le Transistor a Effet de Champ de Puissance a Heterostructure InAlAs/n+-InGaAs." Paper presented at the Fourth Journees Microelectronique et Optoelectronique III-V, La Grande Motte, France, October 21-23, 1992. Unpublished.