Chapter 2. High-Frequency InAlAs/InGaAs Metal-Insulator-Doped Semiconductor Field-Effect Transistors (MIDFETs) for Telecommunications

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2.1 Introduction

Sponsors

Charles S. Draper Laboratories, Inc.
Contract DL-H-418488
Fujitsu Laboratories
Joint Services Electronics Program
Contract DAAL03-89-C-0001
Contract DAAL03-92-C-0001
Texas Instruments

The goal of this project is to investigate InAlAs/n$^+$-InGaAs Metal-Insulator Doped channel Field-Effect Transistors (MIDFETs) on InP. These devices are of great interest for applications in long-wavelength lightwave communication systems and ultra-high frequency high-power microwave telecommunications.

InAlAs/InGaAs Modulation-Doped Field-Effect Transistors (MODFETs) on InP have recently emerged as an optimum choice for a variety of microwave and photonics applications. This is because the outstanding transport properties of InGaAs have yielded devices with very low-noise and high-frequency characteristics. Unfortunately, the low breakdown voltage of InAlAs/InGaAs MODFETs on InP (typically less than 5 V) severely restricts their use in high-power applications, such as large-signal microwave amplification and laser driving. It also forces the use of a separate high voltage supply to operate the Metal-Semiconductor-Metal (MSM) photodetectors in InP photonics receivers.

A device strategy with great potential for power handling is the InAlAs/n$^+$-InGaAs MIDFET featuring an undoped insulator and a thin, heavily-doped channel. In this structure, the breakdown voltage, V_B, is large and can be engineered using pseudomorphic insulators[2] and channel quantization (shown below). Drain current, I_D, can also be considerably improved with InAs-rich channels.[3] The attainment of high power, however, demands a large $I_D \times V_B$ product. InAs-rich channel devices unfortunately suffer from a low breakdown voltage due to: (1) the reduced channel bandgap, and (2)

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[1] Fujitsu Laboratories, Atsugi, Japan.

[2] S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 38(9): 1986-1992 (1991).

[3] S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100.

severe gate leakage at the sidewall of the mesa, where the gate comes in contact with the heavily-doped channel.[4]

Towards solving this severe problem in this period of performance, we have studied the effect of quantizing the InGaAs channel. This has resulted in a drastically improved breakdown voltage through a quantum mechanically engineered enlargement of the effective bandgap of the channel. We have also solved the isolation problem through a selective chemical recessing of the edge of the channel on the mesa sidewall. We have finally integrated all our understanding developed over the last three years into a device with a strained (InAs-rich) channel, strained (AlAs-rich) insulator, quantized channel, optimized channel doping, and edge isolated device which has displayed unprecedented power and frequency performance. A detailed description of these experiments is presented in this report.

2.2 Quantum-channel InAlAs/n$^+$-InGaAs MIDFETs

In previous work, we have shown that enriching the InAs mole fraction of $In_{0.53}Ga_{0.47}As$ channel results in MIDFETs with superior transport properties. However this comes at the cost of a severely reduced breakdown voltage, V_B, presumably through the decrease in the energy gap, E_g.[3] A method of increasing the effective energy gap in the channel is to introduce energy quantization by reducing the channel thickness to dimensions comparable to the electron wavelength (figure 1). In fact, it has been shown that in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ quantum wells the photoluminescence emission wavelength decreases[5] with a reduction in well thickness.

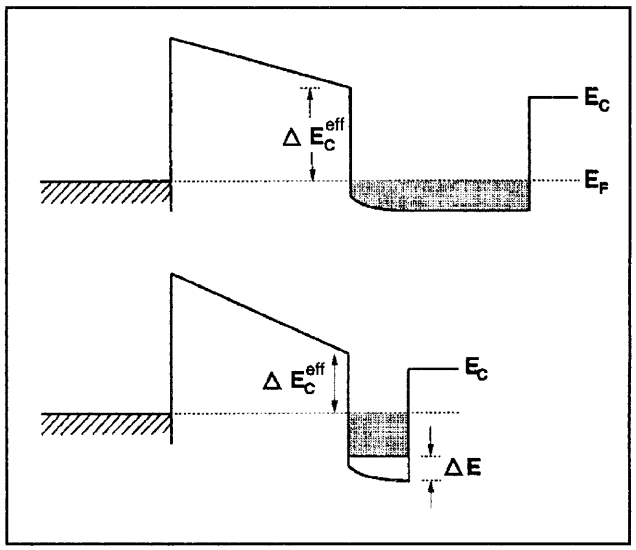

Figure 1. Schematic conduction band diagrams in equilibrium of InAlAs/n$^+$-InGaAs HFETs for thick and thin channels, showing the increase in effective energy gap in the thinner channel.

In this work, we exploit this effect to enhance the breakdown voltage of $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFETs on InP. We have doubled V_B by shrinking the $In_{0.53}Ga_{0.47}As$ channel thickness from 350Å to 100Å, keeping other physical parameters constant. The principle behind our work should allow one to better exploit the excellent transport properties of InAs-rich InGaAs and other promising narrow gap semiconductors like InAs[6] and InSb.

A cross section of the device structure is shown in figure 2. The wafers were grown on SI-InP by MBE in MIT's Riber 2300 system. In an effort to keep the channel charge constant, the thickness of its undoped portion was varied while the thickness of its heavily doped portion was kept constant at 100Å. Four wafers were subsequently grown with subchannel thicknesses of 250Å, 100Å, 50Å, and 0Å, i.e., total channel thicknesses of 350Å, 200Å, 150Å, and 100Å. Devices were fabricated with nominal gate lengths of 1 μm and widths of 30

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[4] S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100.

[5] D.F. Welch, G.W. Wicks, and L.F. Eastman, "Optical Properties of GaInAs/AlInAs Single Quantum Wells," *Appl. Phys. Lett.* 43(8): 762-764 (1983); W. Stolz, K. Fujiwara, L. Tapfer, H. Oppolzer, and K. Ploog, "Luminescence of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ Quantum Well Heterostructures Grown by Molecular Beam Epitaxy," *Inst. Phys. Conf. Ser.* 74(3): 139-144 (1985).

[6] C.C. Eugster, T.P. Broekaert, J.A. del Alamo, and C.G. Fonstad, "An InAlAs/InAs MODFET," *IEEE Electron Dev. Lett.* 12(12): 707-709 (1992).

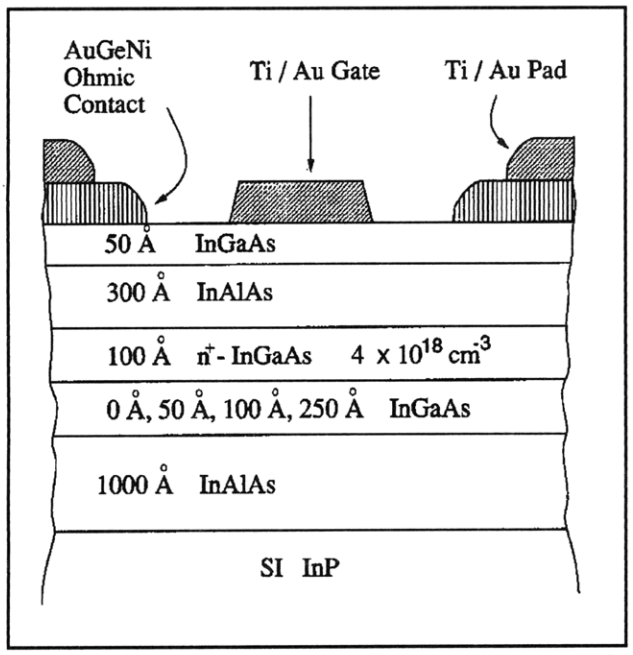

Figure 2. Cross-section of grown device structures in quantum-channel experiment.

μm. Fabrication is similar to that used in Bahl, Azzam, and del Alamo (1991).[7]

Our baseline device, 200Å channel thickness, had a peak transconductance, $g_{m(peak)}$, of 202 mS/mm and a maximum drain current, $I_{d(max)}$, of 312 mA/mm. The output conductance, g_d, was 5.73 mS/mm, resulting in a voltage gain, A_V, of 35. These are average values over five devices. $g_{m(peak)}$ and $I_{d(max)}$ were measured at $V_{ds} = 4$ V, and g_d at $V_{ds} = 4$ V and $V_{gs} = 0$ V. The contact and channel sheet resistances, measured by TLM, are 0.37 $\Omega \cdot$ mm and 625 $\Omega/\square$, respectively.

The reverse gate breakdown voltage, V_B, was measured with the source and drain grounded, and was defined at a reverse gate current of 500 μA, corresponding to about 5% of the peak drain current of our baseline device.[8] Here we focus on our main result: the increased breakdown voltage in devices with thinner channels and the experimental confirmation of the energy quantization therein.

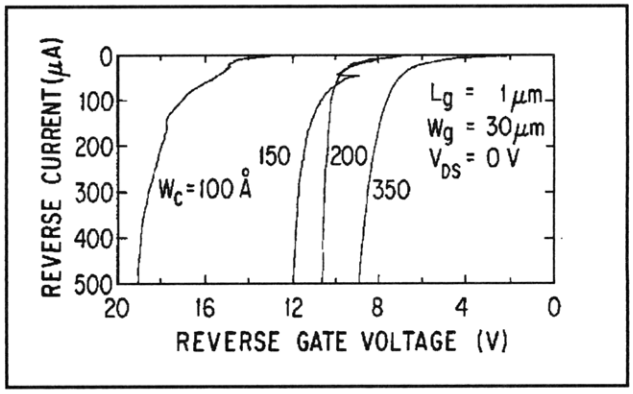

Figure 3. Breakdown voltage, V_B, for typical HFETs with channel thicknesses of 100Å, 150Å, 200Å, and 350Å.

Figure 3 shows typical reverse gate I-V characteristics of HFETs as a function of channel thickness. As shown, V_B increases gradually from 9 V at a channel thickness of 350Å to 10.6 V at 200Å, 11.9 V at 150Å, and to 19.1 V at 100Å. Average V_B measurements over several devices are within 1 V of the typical values shown in figure 3. V_B for the 200Å channel is also similar to what we have previously measured in identical devices grown and processed separately.[8] The drastic improvement in breakdown voltage of our quantized-channel HFETs is a significant merit for high-power applications. This is particularly so in this material system because typical InAlAs/InGaAs MODFET breakdown voltages are on the order of 5 V.[9]

In order to verify the bandgap enhancement in the channel as a result of carrier quantization, we have carried out photoluminescence (PL) measurements on unprocessed portions of the device samples at 77 K. The results are shown in figure 4. The energy of the peak PL intensity increases from 0.83 eV for the 350Å channel, to 0.86 for 200Å, to 0.88 for 150Å, and to 0.92 eV for the 100Å channel. The literature reports a temperature-independent PL energy shift of about 60 meV over

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7 S.R. Bahl, W.J. Azzam, and J.A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.* 38(9): 1986-1992 (1991).

8 S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100.

9 P.C. Chao, A.J. Tessmer, K.-H.G. Duh, P. Ho, M.-Y. Kao, P.M. Smith, J.M. Ballingall, S.-M. Liu, and A.A. Jabra, "W-band Low-Noise InAlAs/InGaAs Lattice-Matched HEMT's," *IEEE Electron Dev. Lett.* 11(1): 59-62 (1990); Y.-C. Pao, C.K. Nishimoto, R. Majidi-Ahy, J. Archer, N.G. Bechtel, and J.S. Harris, Jr., "Characterization of Surface-Undoped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP High Electron Mobility Transistors," *IEEE Trans. Electron. Dev.* 37(10): 2165-2170 (1990).

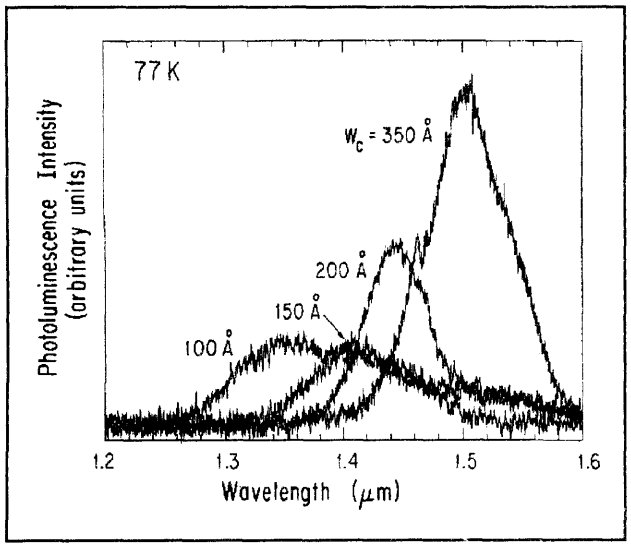

Figure 4. Photoluminescence spectra of the device heterostructures, showing an increase in photoluminescence energy with decreasing channel thickness.

the $In_{0.53}Ga_{0.47}As$ bulk value for 100Å thick $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ quantum wells.[10] This value of 60 meV is also consistent with simple calculations for a finite square well of thickness 100Å. Our slightly larger shift of 90 meV in the 100Å channel might be due to depletion at the top and possibly bottom interfaces, causing a reduced effective well thickness. Additionally, band bending in the insulator results in an effective stronger potential than a square well (figure 1). Both effects will tend to enhance the strength of carrier quantization over a simple quantum well.

Electron quantization, as schematically shown in figure 1, also implies a reduction of the effective conduction band discontinuity between channel and metal gate. This, in return, is expected to result in enhanced forward gate leakage current. We have experimentally found this to be the case at 300 K and 77 K,[11] providing us in this manner with an independent confirmation of the presence of quantization in the channel.

Unfortunately, we have found that a reduction in the channel thickness results in the degradation of transconductance and peak drain current.[11] $g_{m(peak)}$ decreases from 262 mS/mm to 138 mS/mm, and $I_{d(max)}$ from 451 mA/mm to 208 mA/mm in going from a channel thickness of 350Å to 100Å. However, the output conductance g_d, improves due to the enhanced channel aspect ratio, decreasing from 10.8 mS/mm to 1.84 mS/mm. This results in an enhancement in the voltage gain, A_V, from 24 to 75. The degradation in $g_{m(peak)}$ and $I_{d(max)}$ results from an increased source resistance R_s, a reduced channel sheet charge concentration n_s, and degraded mobility, μ. From 350Å to 100 Å, R_s increases from 1.4 Ω • mm to 2.7 Ω • mm, n_s drops from 2.38×10^{12} cm^{-2} to 1.77×10^{12} cm^{-2}, and μ decreases from 4318 $cm^2/V\text{-}s$ to 3591 $cm^2/V\text{-}s$. n_s and μ were measured by the Hall-effect. The acknowledged poor quality of the reverse InGaAs/InAlAs interface at the back of the channel can be held responsible for the mobility reduction.[12] As the undoped subchannel is thinned down, the reverse interface has a larger impact on carrier mobility since the channel electrons travel closer to the reverse InAlAs/InGaAs interface. There are, however, techniques that could mitigate this degradation: superlattice buffers to improve mobility[13] and the Migration-Enhanced Epitaxy (MEE) growth technique to reduce interface roughness.[14]

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[10] D.F. Welch, G.W. Wicks, and L.F. Eastman, "Optical Properties of GaInAs/AlInAs Single Quantum Wells," *Appl. Phys. Lett.* 43(8): 762-764 (1983); W. Stolz, K. Fujiwara, L. Tapfer, H. Oppolzer, and K. Ploog, "Luminescence of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ Quantum Well Heterostructures Grown by Molecular Beam Epitaxy," *Inst. Phys. Conf. Ser.* 74(3): 139-144 (1985).

[11] S.R. Bahl and J.A. del Alamo, "A Quantized-channel $In_{0.52}Al_{0.48}As/n^+\text{-}In_{0.53}Ga_{0.47}As$ HFET with High Breakdown Voltage," Extended Abstracts of the Materials Research Society 1990 Fall Meeting, Boston, Massachusetts, no. EA-21, p. 117.

[12] A.S. Brown, J.A. Henige, and M.J. Delaney, "Photoluminescence Broadening Mechanisms in High Quality GaInAs-AlInAs Quantum Well Structures," *Appl. Phys. Lett.* 52(14): 1142-1143 (1988); T. Sajoto, M. Santos, J.J. Heremans, M. Shayegan, M. Heiblum, M.V. Weckwerth, and U. Meirav, "Use of Superlattices to Realize Inverted GaAs/AlGaAs Heterojunctions with Low-temperature Mobility of 2×10^6 $cm^2/V\,s$," *Appl. Phys. Lett.* 54(9): 840-842 (1989).

[13] T. Sajoto, M. Santos, J.J. Heremans, M. Shayegan, M. Heiblum, M.V. Weckwerth, and U. Meirav, "Use of Superlattices to Realize Inverted GaAs/AlGaAs Heterojunctions with Low-temperature Mobility of 2×10^6 $cm^2/V\,s$," *Appl. Phys. Lett.* 54(9): 840-842 (1989).

[14] Y.C. Chen, P. Bhattacharya, and J. Singh, "Strained Layer Epitaxy of InGaAs (on GaAs) by MBE and Migration Enhanced Epitaxy - Comparison of Growth Modes and Surface Quality," *J. Cryst. Growth* 111(1-4): 228-232 (1991).

Thinning down the subchannel reduces the sheet carrier concentration, possibly from backside depletion. A reduced channel doping can also result in an improvement of breakdown voltage. In a separate experiment on similar devices (with 200 Å channel thickness), we examined the impact of channel doping on V_B. This experiment indicated that a reduction in sheet charge concentration from 2.38×10^{12} cm^{-2} to 1.77×10^{12} cm^{-2} should result in an improvement of V_B by 5 V. Our experimental observation of a 10 V improvement in going from a 350Å to 100Å channel is evidence that quantization is instrumental in drastically enhancing the breakdown characteristics of our HFETs.

In conclusion, $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFETs have been fabricated with channel thicknesses of 100Å, 150Å, 200Å, and 350Å. For devices with channel thicknesses of 100Å, the breakdown voltage improved twofold over the 350 Å devices. This is postulated to arise partially from an enlargement of the effective energy gap caused by energy quantization introduced from electron confinement, as observed by PL.

2.2.1 Elimination of Mesa-Sidewall Gate-Leakage Current by Selective Sidewall Recessing

We have shown in previous work[15] that fabrication of InAlAs/n^+-InGaAs MIDFETs by conventional mesa isolation results in sidewalls where the InGaAs channel is exposed and comes in contact with the gate metallization running up the mesa (figure 5). The low Schottky barrier height of metals on InGaAs[16] potentially results in a sidewall leakage path from the gate to the channel. Sidewall-leakage in InAlAs/InGaAs HFETs results in excessive gate-leakage current,[15] reduced breakdown voltage,[15] and increased sidegating.[17] In HFETs, sidewall-leakage was also found, by the present authors, to worsen with high doping, an increased channel thickness, and increased x ($x > 0.53$) in the $In_xGa_{1-x}As$ channel.[18] This latest trend is particularly consequential, since HFETs with InAs enriched channels have shown excellent electron transport properties.[19]

Airbridging and ion implantation have been utilized in InGaAs HFET isolation. Airbridging is complex, and implantation demands capital-intensive tools. In this paper, we propose and demonstrate a new, simpler technique by which we selectively recess the exposed InGaAs channel into the sidewall. The subsequently e-beamed gate metallization does not enter this cavity and remains isolated from the channel edge. This one-step technique is self aligned to the mesa, requires no additional masks, gate-length insensitive, and works for mesas in all crystallographic directions on the (100) surface.

The MBE grown heterostructure, lattice-matched to S.I. InP, consists of (bottom to top) a 1000Å undoped $In_{0.52}Al_{0.48}As$ buffer layer, an $In_{0.53}Ga_{0.47}As$ channel consisting of a 100Å undoped subchannel and a 80Å heavily Si doped ($N_D = 6 \times 10^{18}$ cm^{-3}) transport layer, a 300Å undoped $In_{0.52}Al_{0.48}As$ gate insulator layer, and an undoped 50Å $In_{0.53}Ga_{0.47}As$ cap. For clarity in SEM imaging, an additional heterostructure with a thicker $In_{0.53}Ga_{0.47}As$ channel (120Å doped and 300Å undoped) was processed along with the device sample.

Devices were fabricated by first chemically etching a mesa down to the InP substrate using a H_2SO_4:H_2O_2:H_2O 1:10:220 etch. Then, before removing the mesa-level photoresist mask, the wafer was dipped for 45 seconds into a SA:H_2O_2

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[15] S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100.

[16] H.H. Wieder, "Fermi Level and Surface Barrier of $Ga_xIn_{1-x}As$ Alloys," *Appl. Phys. Lett.* 38(3): 170-171 (1981).

[17] Y-J. Chan, D. Pavlidis, and G-I. Ng, "The Influence of Gate-Feeder/Mesa-Edge Contacting on Sidegating Effects in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure FET's," *IEEE Electron Dev. Lett.* 12 (7): 360-362 (1991).

[18] S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100; S.R. Bahl, M.H. Leary, and J.A. del Alamo, "Mesa-Sidewall Gate-Leakage in InAlAs/InGaAs Heterostructure Field-Effect Transistors," submitted for publication.

[19] S.R. Bahl and J.A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ Heterostructure Field-Effect Transistor with an In-Enriched Channel," *Proceedings of the Second International Conference on InP and Related Compounds,* Denver, Colorado, April 23-25, 1990, p. 100; U.K. Mishra, A.S. Brown, and S.E. Rosenbaum, "DC and RF Performance of 0.1 μm Gate Length $Al_{0.48}In_{0.52}As$-$Ga_{0.38}In_{0.62}As$ Pseudomorphic HEMT's," *Proceedings of the International Electron Device Meeting,* 1988. pp. 180-183.

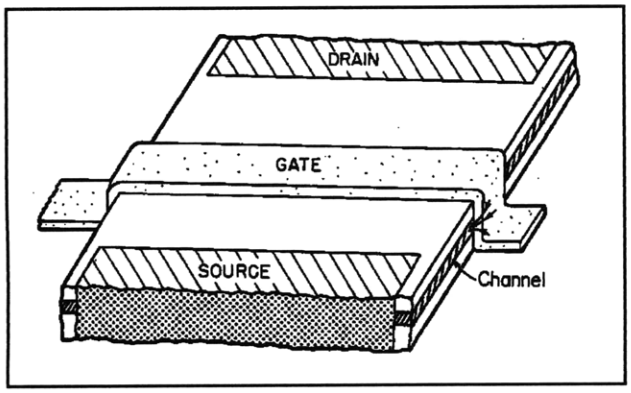

Figure 5. Three-dimensional perspective of an HFET showing the mesa-sidewall gate-leakage path.

6:1 solution[20] to selectively etch the exposed portion of the $In_{0.53}Ga_{0.47}As$ channel in a self-aligned manner. The SA solution was prepared by adding 1 liter H_2O to 200 g. succinic acid with the addition of ammonium hydroxide until the pH was 5.5. A planar selectivity of 23:1 was measured, with the $In_{0.52}Al_{0.48}As$ etching at 25Å/min. For reference, a portion of the wafer was masked during this etch by coating with photoresist using a paintbrush. In this portion, mesa etching was performed, but no selective sidewall-recessing was carried out. For the ohmic contacts, 2000Å of AuGe and 600Å of Ni were evaporated, lifted off, and RTA alloyed at 360° C. For the gate and pad, 300Å of Ti, 300Å of Pt, and 2000 Å of Au were e-beam evaporated and lifted off. This process should be compatible with recessed-gate devices. If the same etchant is used for gate-recessing, then sidewall-recessing could be performed simultaneously.

To study sidewall-leakage, we fabricated special-purpose heterojunction diodes with an active Schottky area of 10,000 μm^2. Gate-metal/mesa-sidewall overlaps were created by etching grooves through the active diode during mesa formation, and then depositing gate metal on top. The ohmic contact surrounds the gate region. Twelve diodes were fabricated in each die, with sidewall-overlap lengths, L_s, of 0, 200, 400, and 600 μm, running in each of [011], [001] and [01$\bar{1}$] crystallographic directions. Figure 6 shows a photograph of the diode test structure with various sidewall-overlap lengths along one selected crystallographic direction.

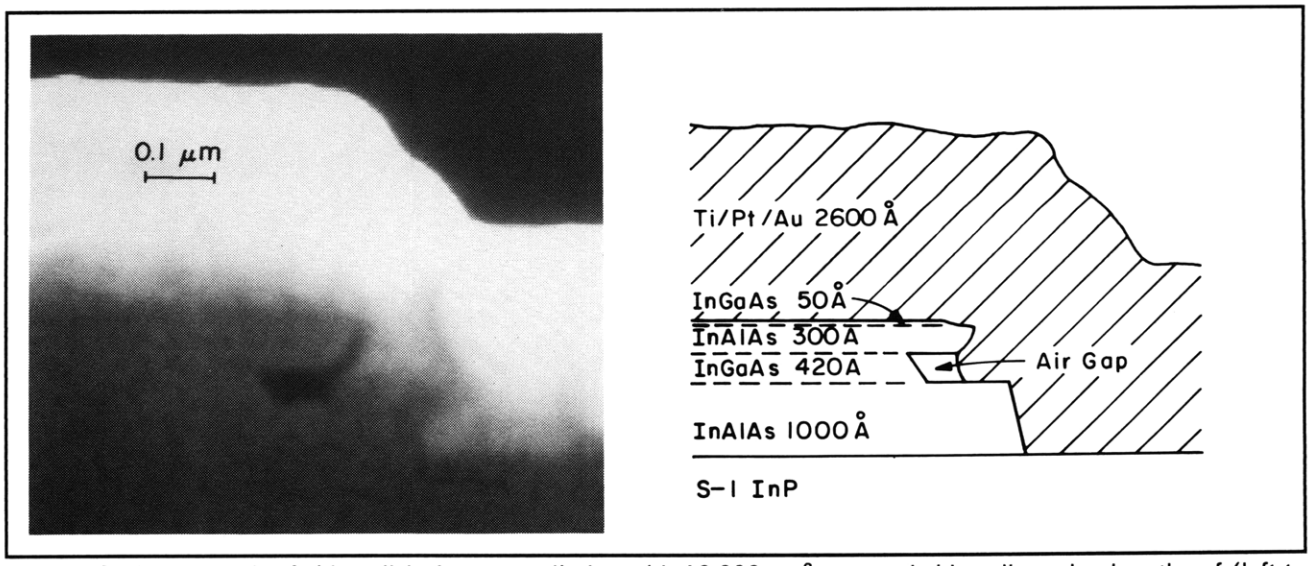

Figure 6. Photograph of sidewall-leakage test diodes with 10,000 μm^2 area and sidewall overlap lengths of (left to right) 600, 400, 200, and 0 μm.

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[20] T.P.E. Broekaert and C.G. Fonstad, "AlAs Etch-Stop Layers for InGaAsAs/InP Heterostructure Devices and Circuits," *IEEE Trans. Electron Dev.,* forthcoming (1992).

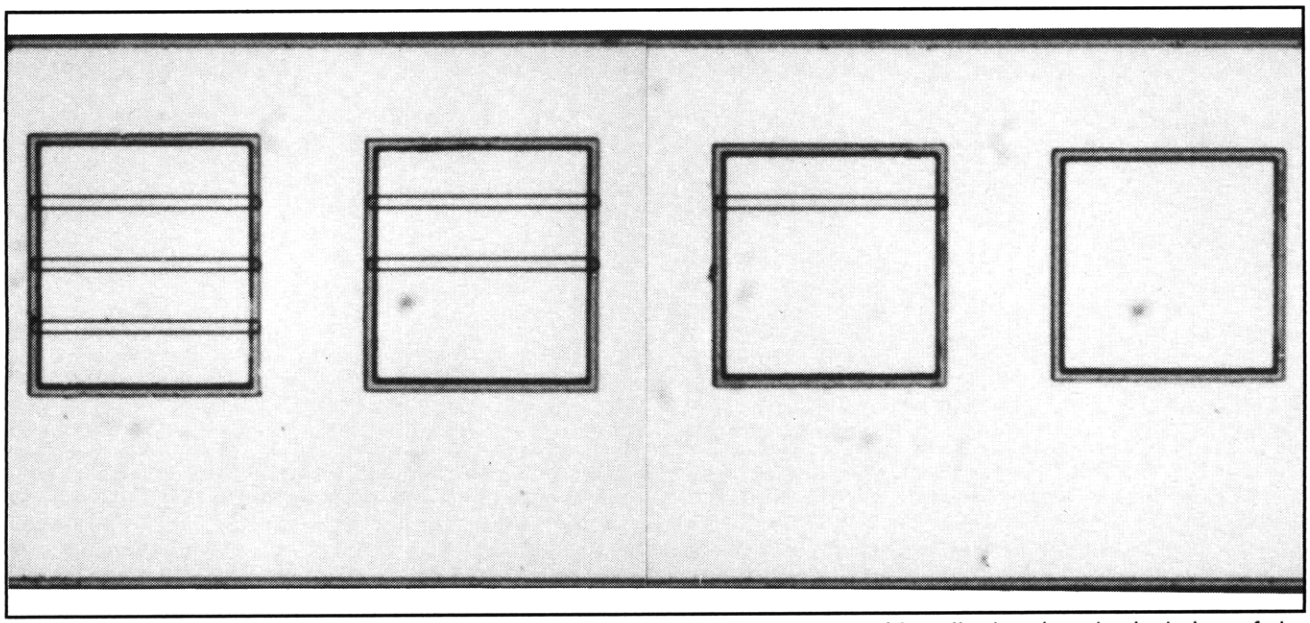

Figure 7. SEM photograph and explanatory sketch of the heterostructure sidewall, showing the isolation of the gate metal from the channel.

Figure 7 shows an SEM photograph and a sketch of the finished heterostructure with 420 Å $In_{0.53}Ga_{0.47}As$ channel processed with the other device samples. The presence of a sidewall cavity is clearly revealed. This confirms the successful action of the selective etchant. The overhang formed by the InAlAs insulator prevents the gate from contacting the channel edge.

Figure 8 shows the I-V characteristics of typical heterojunction diodes from the non-sidewall-recessed portion of the wafer with grooves along the $[0\bar{1}1]$ direction. Both forward and reverse diode currents increase with sidewall-overlap length, as expected from the increase in contact area. This unmistakably proves the existence of a significant sidewall-leakage path. The figure shows that sidewall-leakage plays a major role from forward-bias till threshold (-0.82 V), when the channel is depleted. We also find (not shown) that sidewall-leakage depends on crystallographic orientation as $I[0\bar{1}1] > I[001] > I[011]$. For typical diodes with $L_s = 200$ μm, I increases by 38% from [011] to $[0\bar{1}1]$ at $V = -2$ V.

In the sidewall-recessed portion of the wafer, both sidewall-length and orientation dependence of the diode current have disappeared. This is shown in figure 9, a plot of the I-V characteristics of twelve diodes (one of each stripe and orientation) from the sidewall isolated portion of the wafer. All reverse characteristics are tightly clustered and randomly distributed around the baseline area leakage characteristic observed for zero overlap length in figure 8. The absence of orientation and overlap length dependence confirms that sidewall-leakage has been completely eliminated for all crystallographic orientations.

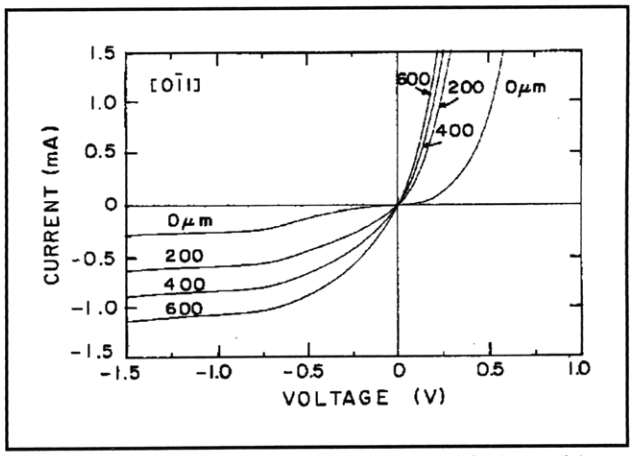

Figure 8. I-V characteristics of test diodes without sidewall recessing, as a function of sidewall overlap length along the $[0\bar{1}1]$ direction on the wafer surface.

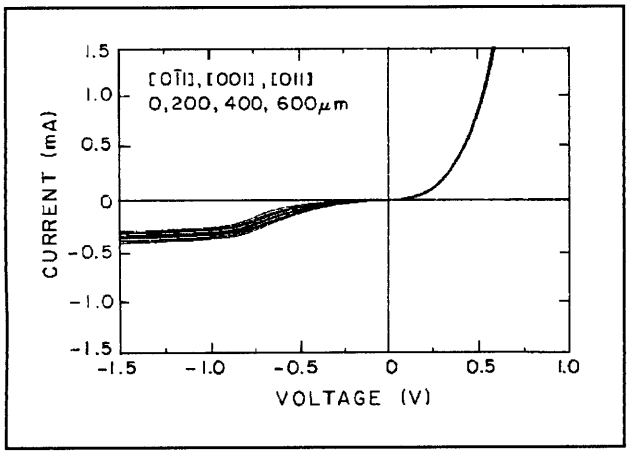

Figure 9. I-V characteristics of test diodes with sidewall recessing, for different orientations and sidewall overlap lengths.

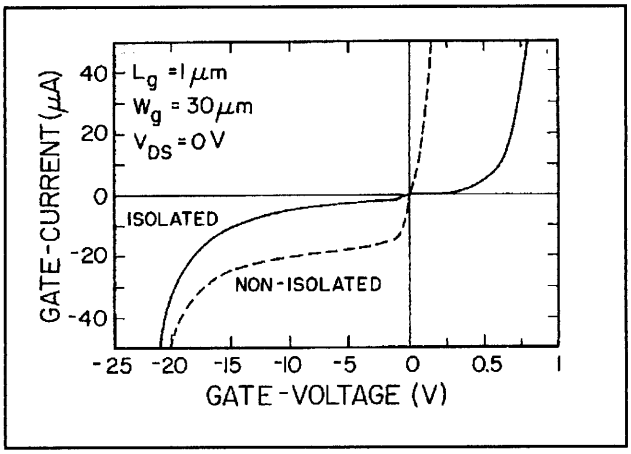

Figure 10. Gate-diode characteristics of HFETs, with and without sidewall isolation, for $L_g = 1$ μm and mesa sidewall along [0$\bar{1}$1].

On the same wafer, we have also fabricated HFETs with nominal gate length, L_g, and width, W_g, of 1 μm and 30 μm respectively. Figure 10 shows the impact of sidewall isolation on the gate characteristics. Sidewall isolation results in lower gate-leakage current, a larger gate turn-on voltage, and an increased breakdown voltage. The complete elimination of sidewall-leakage in HFETs was confirmed by the disappearance in orientation dependence of the subthreshold current (not shown) at several gate-lengths.

In conclusion, a simple self-aligned technique for eliminating mesa-sidewall gate-leakage has been developed. This technique uses selective etching to etch the exposed part of the InGaAs channel into the mesa-sidewall, creating a cavity to isolate the channel from the gate. Measurements on specially designed diodes have shown complete elimination of sidewall-leakage. This process should be useful for any kind of heterostructure in the InAlAs/InGaAs system.

2.2.2 Doubly Strained InAlAs/n$^+$-InGaAs HFET

In this section, we pull together all the knowledge developed over the last three years on InAlAs/n$^+$-InGaAs MIDFETs and present an original device design that features for the first time: (1) complete elimination of sidewall leakage, (2) an optimized channel doping level, and (3) high electron confinement by using a strained (AlAs-rich) insulator and a quantized and strained (InAs-rich) channel. The resulting device, though moderate in L_g, displays unprecedented power handling capabilities.

The MBE grown HFET (figure 11) on S.I. InP consists of (bottom to top), a 1000Å $In_{0.52}Al_{0.48}As$ buffer, a 75Å $In_{0.53}Ga_{0.47}As$ subchannel, a 100 Å n$^+$-$In_xGa_{1-x}As$ channel, a 300Å $In_{0.41}Al_{0.59}As$ strained insulator, and a 50Å $In_{0.53}Ga_{0.47}As$ cap. The insulator thickness and mole fraction were chosen to avoid misfit dislocations while providing maximum conduction band discontinuity. The subchannel thickness was chosen to introduce electron quantization and increase E_g in the channel without significantly degrading current driving capability. The impact of channel doping was examined by growing three wafers with lattice matched (x = 0.53) channels nominally doped to 4, 6, and 8 $\times 10^{18}$ cm^{-3}. From power considerations, as indicated below, an optimum doping level of 6 $\times 10^{18}$ cm^{-3} was selected. This is the doping at which the InAs-rich channel (x=0.65) device was grown.

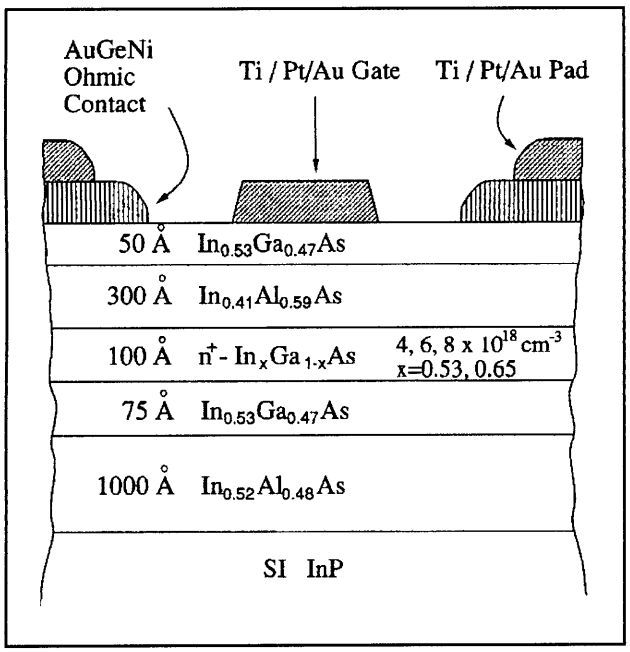

Figure 11. Cross-section of doubly-strained device structure.

Devices (see sketch in figure 11) were processed by mesa etching, sidewall isolation etching, RTA alloying of lifted-off Ge/Au/Ni ohmic contacts, and lifting-off Ti/Pt/Au gates and pads. Sidewall isolation was done by selectively etching the InGaAs channel edge into the sidewall to create a cavity. Gate-metal running up the mesa sidewall does not enter the cavity, and therefore does not contact the channel edge. Measurements are reported for 1.9 μm gate length (L_g) HFETs. All DC measurements are averaged over several devices.

In our x=0.53 channel devices, higher channel doping results in higher $I_{D(max)}$, but lower V_B. $I_{D(max)}$ for dopings of 4, 6, and 8 $\times 10^{18}$ cm^{-3} is respectively 117, 220, and 371 mA/mm. V_B is 21.1, 15.6, and 5.3 V, giving an $I_{D(max)} \times V_B$ product of 2.5, 3.4, and 2.0 W/mm respectively. f_t and f_{max} also increase with doping. f_t is 9.2, 11.3, and 12.8 GHz, and f_{max} is 34, 42, and 68 GHz, respectively.

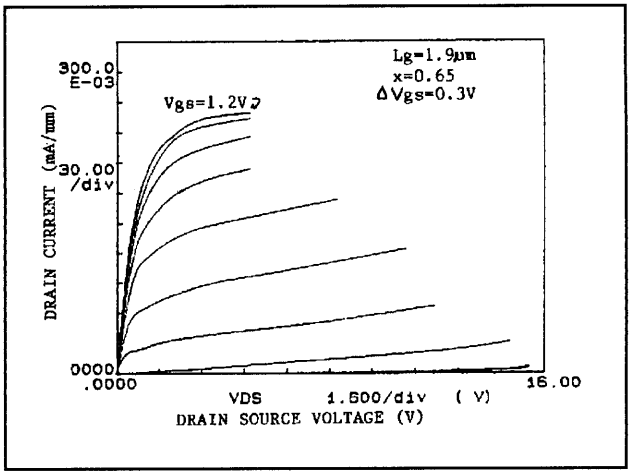

Figure 12. I-V characteristics of x=0.65 HFET.

For our doubly-strained InAs-rich (x=0.65) channel device, we found $g_{m(peak)}$ = 201 mS/mm, and $I_{D(max)}$ = 276 mA/mm (figure 12). f_t was 14.9 GHz and f_{max} 101 GHz (figure 13). This gives an effective electron velocity of 1.8 $\times 10^7$ cm/sec for our 1.9 μm L_g, comparable to values obtained in MODFETs of similar L_g 's. The high f_{max} is a consequence of low g_d (0.9 mS/mm at peak f_t) as this device is now able to enter accumulation at $V_{gs} \geq 0$ V. The voltage gain at peak f_t is 150. The average V_B was 12.8 V (figure 14). This results in an average $I_D \times V_B$ product of 3.5 W/mm. Devices capable of handling as much as $I_D \times V_B$ = 4 W/mm were obtained. These values represent an improvement over similar gate length MODFETs of 2 to 3 times. High electron confinement and reduced gate leakage in these HFETs are instrumental in obtaining these values.

In conclusion, in the pursuit of high-power InAlAs/InGaAs HFETs, we have combined for the first time in a single device, an optimized heavily-doped channel, an AlAs enriched insulator, an InAs enriched channel, channel quantization, and mesa-sidewall leakage elimination. We have thereby been able to fabricate a high-voltage, high-current device with excellent microwave characteristics. Scaled down versions of this device are very promising for high-power microwave and photonics applications.

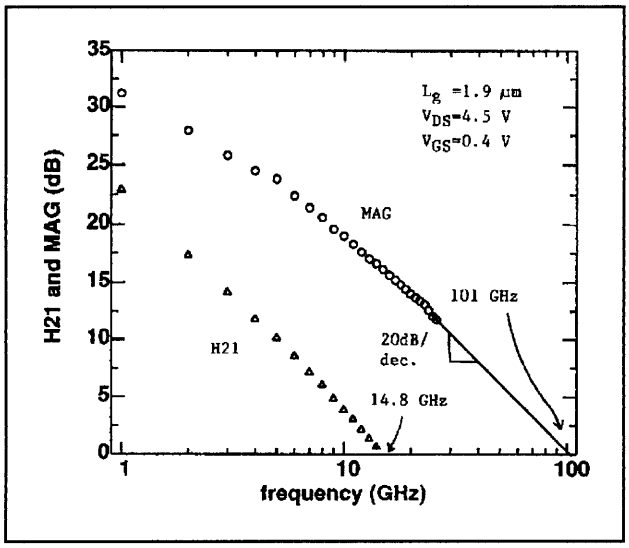

Figure 13. H_{21} and MAG vs. frequency for x=0.65.

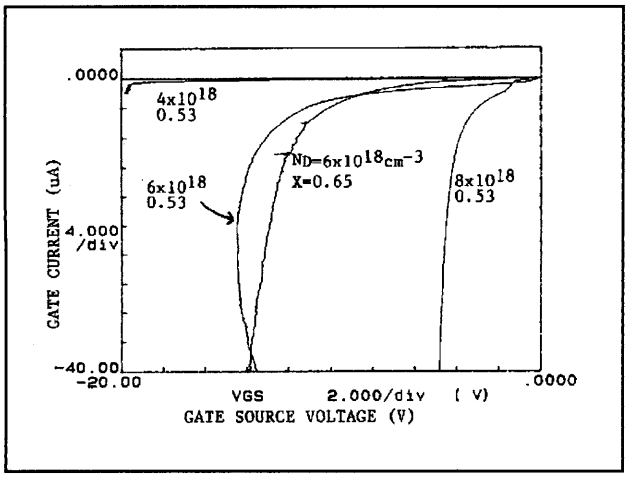

Figure 14. Reverse I_g vs. V_{gs} characteristics for typical HFETs showing that our improvements have mitigated the degradation in V_B for x=0.65 ($W_g = 30\mu m$).

2.2.3 Publications and Meeting Papers

Bahl, S.R., and J.A. del Alamo. "InAlAs/n^+-InGaAs HFETs: Impact of Dislocations and Channel Quantization." Paper presented at the Workshop on Compound Semiconductors Materials and Devices (WOCSEMMAD), Ft. Lauderdale, Florida, February 18-20, 1991.

Bahl, S.R., W.J. Azzam, and J.A. del Alamo. "Orientation Dependence of Mismatched $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ HFETs." *J. Crystal Growth* 111(1-4): 479-483 (1991).

Bahl, S.R., W.J. Azzam, and J.A. del Alamo. "Strained-Insulator $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors." *IEEE Trans. Electron Dev.* 38(9): 1986-1992 (1991).

Bahl, S.R., and J.A. del Alamo. "Elimination of Mesa-Sidewall Gate Leakage in InAlAs/InGaAs HFETs by Selective Sidewall Recessing." *Proceedings of the 18th International Symposium on Gallium Arsenide and Related Compounds,* Seattle, Washington, September 9-12, 1991.