

24. Custom Integrated Circuits

Academic and Research Staff

*Prof. J. Allen, Prof. L.A. Glasser, Prof. P. Penfield,
Prof. R.L. Rivest, Prof. G.J. Sussman, Dr. G.E. Kopec,
Dr. H. Shrobe Jr.*

Graduate Students

*R. Armstrong, I. Bain, Y. Brown, W.H. Evans, L.P.J. Hoyte,
A. Fujimura, M.D. Matson, S.P. McCormick, J.J. Paulos, J. Pineda,
C.R. Seaquist, L.D. Seiler, J. Siskind, B.C. Williams, D.D. Williams,
J.T. Wroclawski*

24.1 Conversion of Algorithms to Custom Integrated Circuits

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Jonathan Allen, Paul Penfield, Jr., Ronald Rivest, Gerald Sussman, Howard Shrobe

The design of custom integrated circuits is concerned with two levels of hierarchy. First of all, there is a hierarchy of different levels of representation, all of which provide a different view of the same structure. Thus, at the highest level, a hardware design language characterizes the overall design, which is then represented in terms of an architecture of interconnected cells. These cells are realized in terms of basic logic and memory functions, which are in turn implemented by a variety of circuit forms, which are finally transferred into the custom integrated circuit by specifying the detailed mask layout. A striking aspect of these different levels of representation is that they are qualitatively distinct, since each of them focuses on a different aspect of the overall design. Complementing this level of hierarchy is a different level which represents the modularity and repeatability of various design elements in an attempt to cope with the complexity of large scale circuits. Thus when circuits must be built that contain half a million or more transistors, individual cells must be used in a repeated fashion and connected together through well defined interfaces to form this large circuit. Given this requirement for dual hierarchies in the design of custom integrated circuits, research is focused on the nature of the different representations used and transformations between them as well as the identification of basic system elements that can modularly comprise the overall circuit structure.

At the highest level, concern is focused on the linguistic means to describe a design. Here the focus is on the desired functionality together with an explicit representation of the required parallelism. In addition means have been derived to transform among alternate specifications that are semantically identical and yet differ in performance. Work on the SCHEME chip has led to the development of a specialized high level specification appropriate for microprogrammed general purpose structures. This style of high level language can then be used as the input to a compilation

strategy for deriving the low level mask specification through various intermediate structures. A second example of a general structure is the MACPITTS system which provides a basic architecture suitable for digital signal processing tasks where there may be multiple parallel processes being executed at the same time. In the MACPITTS system, one finite state machine is provided to instantiate the control for each such process, but all processes share the same basic data path, which in itself contains multiple parallel busses. A simple example of a high level specification is of course the input logic specification for a PLA generator and several such representations have been used in our research.

Moving from the high level functional specification to the various architectural realizations of those specifications, we have provided the formal basis for exploring systematically space/time tradeoffs for any given architecture. That is, given an initial architecture, which is of necessity biased at some particular point of the architectural design space, formal means are available to derive alternate representations of the same functional tasks that vary along the performance dimensions of space, time and power. This capability is particularly important since it provides the designer with the means to explore various alternatives while guaranteeing that the fundamental task is not altered. We have also extended these techniques to the study of serial and parallel techniques for arithmetic (including multiplication) and various memory designs. These tradeoffs interact in a critical way with the layout of the cells and the detailed wiring, and so it is important to be able to systematically explore these alternatives and to derive their consequences at the layout level. Our work in the design of digital signal processing systems has led to substantial insights in this area. Digital filtering tasks, such as those encountered in speech synthesis provide abundant opportunities for parallelism, as do the data paths in the SCHEME and MACPITTS compilation strategies previously referred to. This application domain has also provided us with the motivation to design high performance parallel multipliers as well as multiport memory systems, each of which is used in highly parallel conflict-free signal processing systems. Work is currently underway to generalize the programs for multiplier design so that a multiplier compiler will be available. Thus the designer will be able to automatically generate a high performance parallel multiplier of any size for a variety of different signal processing applications. At the architectural level it is particularly important to be able to explore the consequences of variable word length choices in signal processing systems.

Each of the cells of an overall design, whether characterized as logic or memory, must of course be realized in terms of a circuit in the target technology. Performance considerations concerned with these circuits are a major focus of our laboratory and we have devoted a great deal of effort to the characterization of performance variables (speed, area, and power) and their optimization under various criteria. As circuit scaling goes on, the ability to extract highly accurate circuit parameters from a layout specification becomes more critical. Accordingly we have designed a program that computes resistances and capacitances very accurately, even for nonstandard shapes and internodal effects. We have also done a large number of analytical studies on the delay through RC networks that comprise the interconnect of modern MOS circuits. These bounds permit the assessment of

critical paths in a system, and are an important tool for the designer in exploring the use of various cells and circuit forms. Finally, we are investigating new techniques for modeling nonlinear devices with a view toward high performance circuit simulation systems. Our view is that circuit simulation is an exceedingly valuable tool in the design process, but currently very expensive computationally. Our goal is to discover new modeling and simulation strategies that require less computation, but also to investigate the possibility of special purpose hardware for performing this simulation. Our intent is to incorporate such techniques for investigating performance variables within an overall compilation strategy so that the designer can quickly and correctly investigate various design choices in terms of the impact on these performance variables.

At the lowest level of the design hierarchy, we encounter the problems of generating the detailed mask layout. Here it is necessary to manage a great deal of geometrical detail in an efficient and correct manner. We have designed a highly interactive graphical editor for designing medium sized cells, as well as a text-orientated symbolic language for managing the interconnect of these cells. Our view is that no one layout tool is adequate for all situations, and highly skilled designers often use digitizing for very small cells (such as a memory cell), an interactive graphic editor for medium cells, and a text based language for knitting together these cells at the highest level of the connection hierarchy. To facilitate the placement and connection of these cells, we are continuing to work on a large program that automatically places and routes together rectangular shaped cells of arbitrary aspect ratio with interconnect on all four sides. This program does automatic channel sizing, and uses a hierarchical routing strategy for optimal interconnection. As a natural outgrowth of this research, we have developed a number of powerful channel routers, some of which are very fast and not very optimal, while others provide very efficient channel usage, but require substantial computation due to the combinatorial optimizing process. Another difficult problem at the geometry level is the provision of design rule checking. Many of the tests involved in design rule checking require time proportional to the square of the number of rectangles involved in the layout if special care is not exercised. We have focused on a number of techniques for doing design rule checking in a hierarchal fashion that breaks this square law dependence, but a particularly strong project is the design of special hardware for design rule checking. By using four custom-designed chips, mounted on a board level system, we expect to achieve at least two orders of magnitude speed up in design rule checking. In this way design rule checking can be provided as a modular addition to a VLSI design station providing highly interactive capability for the designer. It is interesting to compare the basic representations used for this hardware design rule checking (which uses a raster scan coarse grid representation) with the conventional rectangle-based design rule checking programs. Both have their place, and are suited for different types of calculations.

All of the techniques described above comprise the basic elements of an overall design system. We are currently working towards the integration of these into a cohesive whole. The requirements for this overall system are being developed through substantial experience in designing explicit chips, ranging from custom microprocessor-type systems intended for the programming language LISP, to

highly parallel signal processing systems. It is our contention that the optimal design of these systems must be performed by those who have intimate algorithmic knowledge of the application areas that require these chips. The design experience gleaned in this way continues to provide direction for the construction of an overall design system, and a number of the modules of this system are currently under development.

24.2 VERY LARGE-SCALE INTEGRATED CIRCUIT RESEARCH

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Lance A. Glasser

The field of Very Large-Scale Integrated Systems (VLSI) is comprised of many different domains of abstraction ranging from machine architecture and VLSI complexity theory to the physics and fabrication of semiconductor devices. Our work is centered on the circuits and switch-level domains, although it also reaches up into the machine organization and functional levels, as well as down to the device physics and modeling regimes.

There are three primary thrusts to our research effort. The first is in VLSI circuit theory which is a new branch of circuit theory specialized to the analysis, synthesis, and optimization of VLSI circuits. Some of the unique aspects of VLSI circuit theory are that it emphasizes techniques which have sufficiently mild computational complexity that one can imagine using them on circuits with millions of transistors. Thus, for an analysis or synthesis algorithm to be considered an element of the theory, its computational complexity should be of order N or $N \cdot \log N$. VLSI circuit theory also seeks to exploit the fundamental properties of correctly constructed digital VLSI systems, including properties derived from the circuit methodology (such as properties of restoring logic), as well as those derivable from the fundamental physics (inductors on an integrated circuit can be neglected and transistors are nonreciprocal). We have made advances in the field of VLSI circuit theory in several different domains of abstraction. For instance, in the area of circuits we have developed hierarchical circuit-simulation techniques which expedite the computationally efficient calculation of voltage waveforms in digital integrated circuits. A unique aspect of this work is that we compute bounds on the shape of waveforms rather than try to compute their exact shape. This technique can potentially save huge quantities of computer time. In the area of analysis we have looked at the syntactic well-formedness of VLSI circuits. We have discovered graph theoretical techniques for looking at a large network and discovering whether or not it contains certain kinds of ill-formed constructs such as write-only-memories. We have also done work on circuit optimization. We have developed a theory for optimally sizing the transistors in a transistor schematic which does not have specified transistor sizes. This work is applicable to large classes of digital integrated circuits. The transistors are sized such that an NMOS circuit meets a delay specification and dissipates minimum power.

A second thrust of our work is the fundamental circuit modeling and design issues such as noise, tolerancing, and delay. These topics are interrelated because, in order to increase noise margins, circuit delays must increase and when delays are low, noise is most important. Both of these issues occur within the context of worst-case design, that is, the tolerancing problem. The performance of all aggressive MOS circuits will become limited by noise in the next five years. Because of the importance of lowering the supply voltage in scaling, voltages will be lowered to the minimum tolerable level in both NMOS and CMOS. To the extent that these voltages are larger than necessary, short-channel, hot-electron, and other detrimental phenomena will degrade the circuit's potential reliability and performance. There are three sources of noise important in digital integrated circuits: external, coupled, and parametric mismatch. External noise comes in each of the power supply lines and the I/O paths. It is aggravated by the inductance and resistance in these paths. In CMOS this noise can also cause latch-up. Coupled noise is of three kinds: capacitive, resistive, and inductive. Each of these is scaling very badly. We have shown, for instance, that certain kinds of inductive noise are getting eight times worse each time dimensions of an integrated circuit are halved. We are working on achieving a much better understanding of these phenomena both theoretically and experimentally.

The final thrust of our research is in the area of computer-aided design for VLSI systems. In this aspect of our work, we apply the knowledge and techniques we have developed in our other areas of research to the design of software to aid VLSI systems design. This is a synergistic relationship because the problems we confront in supporting the design of VLSI systems highlight fertile areas for research in circuit theory and modeling. An example of this is a program to optimally size transistors which is based on new VLSI circuit theory results already discussed. A prototype of this program has optimally sized 4000 transistors in 3.2 seconds of computer time on a DEC system 20/60. While this program is an outgrowth of the theory, the theory was motivated by doing actual designs using an earlier version of the design-automation software. New computer-aided design tools are continually being developed as outgrowths of our theoretical investigations. They are being incorporated into a design environment called Prometheus which we are developing to unite the multiple domains of abstraction needed to incorporate VLSI design into a single structure.

Publications

1. L.A. Glasser and Paul Penfield, Jr., "An Interactive PLA Generator as an Archetype for a New VLSI Design Methodology," Presented at the IEEE International Conference on Circuits and Computers, Port Chester, New York, October 13, 1980.
2. L.A. Glasser, "The Analog Behavior of Digital Integrated Circuits," Presented at the Fall 1980 MIT VLSI Research Review, Cambridge, Massachusetts, December 15, 1980.
3. L.A. Glasser, "The Analog Behavior of Digital Integrated Circuits," Presented at the Eighteenth Design Automation Conference, Nashville, Tennessee, June 29-July 1, 1981.
4. L.A. Glasser and L.P. John Hoyte, "Automated Device Sizing for Integrated Circuit Design," Presented at the Fall 1980 MIT VLSI Research Review, Cambridge, Massachusetts, December 14, 1981.