HARP Collaboration

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A fast front-end electronics for the RPC detector in the HARP experiment

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Abstract

A fast 8-channel summing preamplifier and a 16-channel splitter for the readout of the resistive plate chambers in the HARP detector at the CERN Proton Synchrotron are presented. The on-chamber summing preamplifier has an equivalent input noise of less than 10 fC r.m.s., an amplification of 100 mV/pC and less than 1 ns peaking time. The splitter splits the signals from the summing preamplifier into a timing path and a charge path. In the timing path, the signal amplitude is further amplified by a factor of 10 and then discriminated at a 50 mV threshold. The time-over-threshold signal has an intrinsic time skew of less than 15 ps. The discriminator output is sent via twisted-pair cables to a commercial time-to-amplitude converter. In the charge path, the signal is also amplified and sent via twisted-pair cables to a commercial charge-to-amplitude converter.

Contents

1 Introduction and Requirements

The Resistive Plate Chamber (RPC) detector in the HARP experiment at the CERN Proton Synchrotron was designed for the separation of electrons from pions by time of flight. The requirements were an intrinsic time resolution of better than ∼200 ps and an intrinsic efficiency close to 100%. So-called 'timing' RPCs (as opposed to 'trigger' RPCs) were chosen because of their capability of an intrinsic time resolution in the 100 ps range [1, 2].

The active element of the HARP RPC is a glass stack with four 0.3 mm wide gas gaps consisting of two sets of three glass plates each, placed symmetrically on both sides of the central readout electrode. The glass plates are 0.7 mm thick and made of standard float glass. A detailed description of the RPCs is given in Refs. [3, 4, 5].

Particle identification is achieved by time of flight: the time between the RPC timing signal and the time of arrival of the beam particle at the target. The main challenge for the RPC readout electronics is to preserve the very good intrinsic time resolution offered by the physics of RPC pulse formation.

2 Summing Preamplifier

The precision measurement of time in the 100 ps range requires a very fast, low-noise, front-end amplifier with minimum time slew. To minimize signal reflection and crosstalk, the front-end interconnection lengths must be as short as possible. Hence the summing preamplifier (henceforth denoted SP8) is realized as an on-chamber plug-in module.

The input stage is a very critical low-noise, large-bandwidth circuit. Each of the eight inputs consists of a current-to-voltage converter based on a common-base transistor circuit (PHILIPS BFR92) with 30 Ω input impedance which matches the RPC impedance. Using a transistor input permits good de-coupling between the eight inputs. The eight inputs are connected to a fast summing amplifier (Analog Devices AD8009) through delay lines. This amplifier permits an impedance of less than 10 Ω at the summing point, with less than 1 ns leading-edge rise time and without zero-crossing of the output signal. Each delay line has the same physical length and is realized inside the four-layer printed board as a strip line with 50 Ω impedance and 0.8 ns time delay. The delay lines are terminated by 43 Ω resistors to the summing point.

The SP8 schematics is shown in Fig. 1, its characteristics are summarized in Table 1, and its performance is illustrated in Fig. 2. Photographs of the printed board are shown in Fig. 3.

Eight SP8s are mounted inside each RPC chamber box. The connection length from the RPC signal electrode to the SP8 input is less than 2 cm. Outputs and test signals from each SP8 are connected to a common interface printed board through mini coax cables of individual lengths. From there, the output signals are sent to the 16-channel splitter module through 5 m long coax cables.

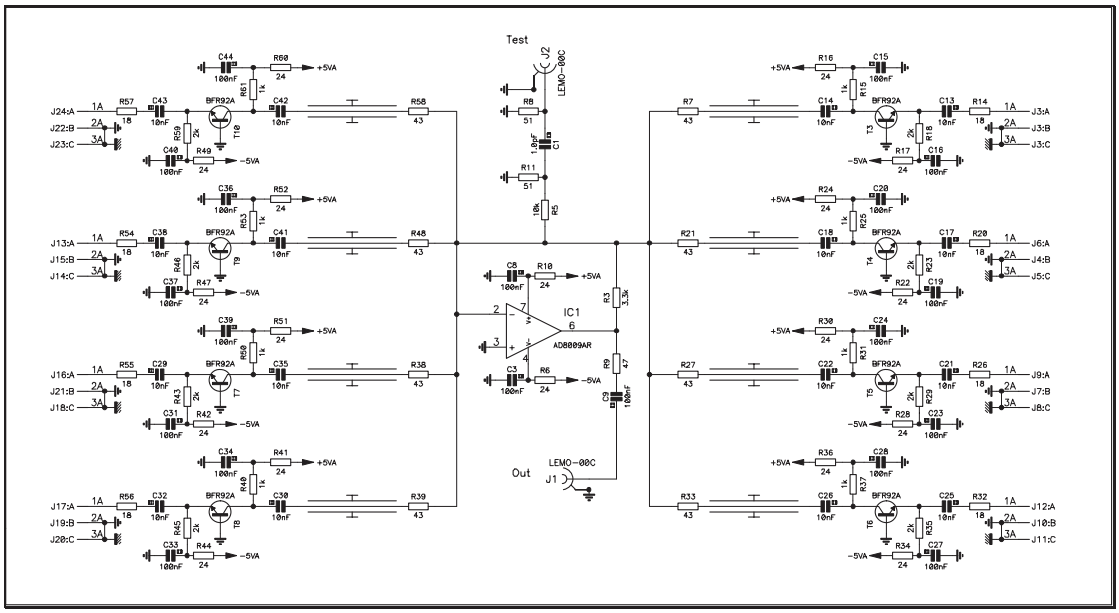

Figure 1: Schematics of the on-chamber summing preamplifier SP8.

Table 1: Characteristics of the On-Chamber Summing Preamplifier SP8

Input impedance	30 Ω
Peaking time	≤ 1 ns
Linear dynamic range	< 20 pC
Amplification factor	100 mV/pC
Equivalent input noise	< 10 fC r.m.s.
Intrinsic I/O time skew (200 fC input)	< 25 ps r.m.s.
Output signal width (10–90%)	25 ns
Input-to-input time skew ($n = 100$)	±15 ps
8-input amplification skew ($n = 100$)	$< 3\%$
Summing amplification skew ($n = 100$)	$< 5\%$
Power consumption	350 mW

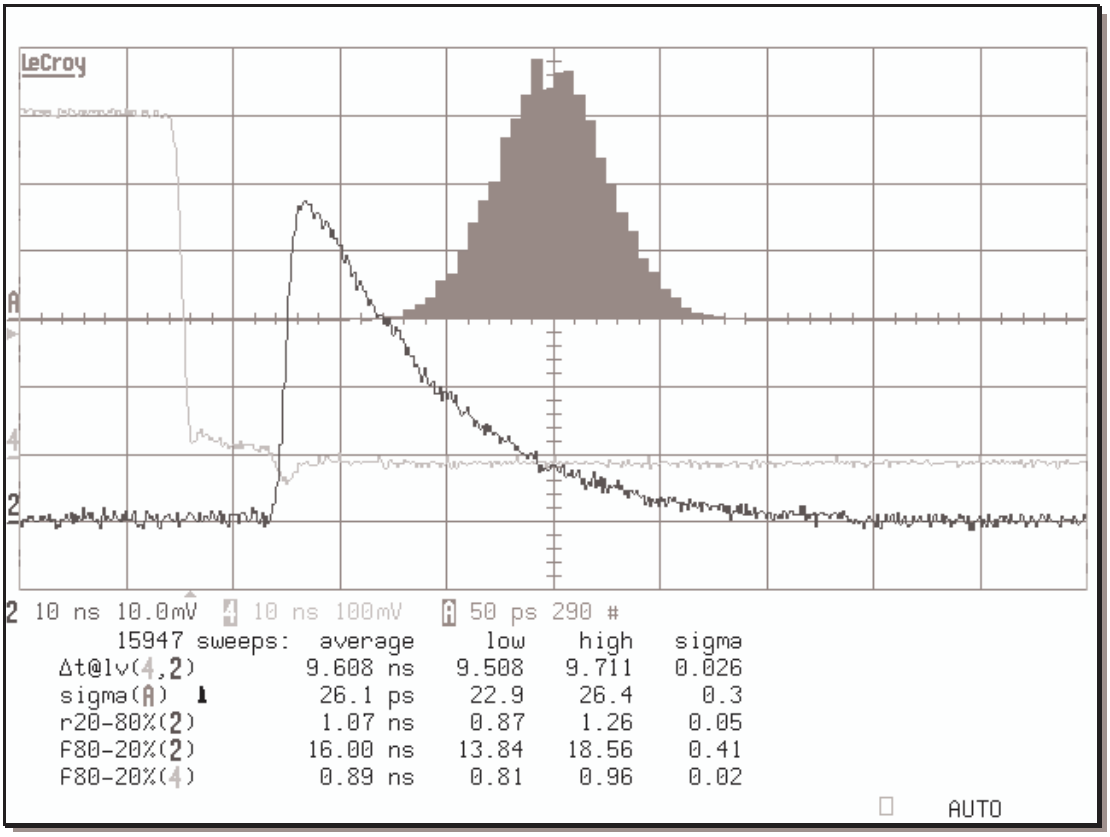

Figure 2: Performance of the SP8 with pulses from a LeCroy LC574A unit; the input signal in one input of the SP8 shown on line 4 corresponds, after differentiation with a 1 pF capacitor, to $Q_{\rm in} = 480$ fC); the output signal is shown on line 2.

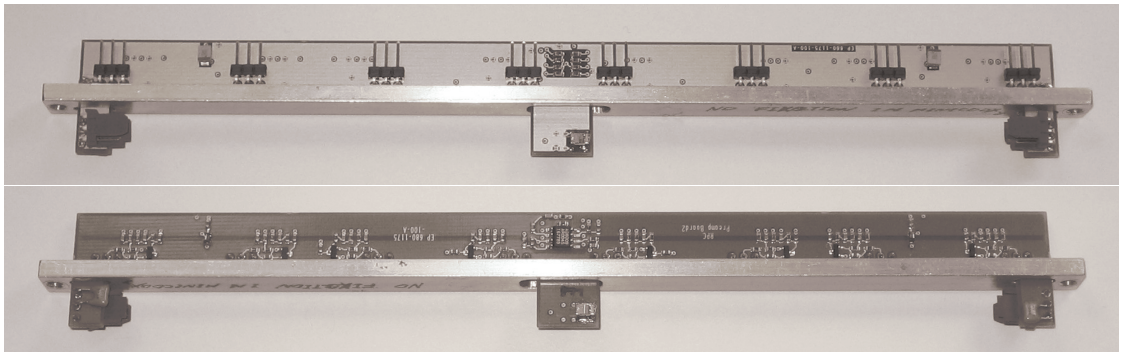

Figure 3: Summing preamplifier SP8 printed board with the eight input connectors and aluminum support plate; the AD8009 chip and the output signal connector are located in the centre of the board.

3 Splitter

The 16-channel splitter (henceforth denoted SSD16) is realized as single-width CAMAC module. Its front panel features three standard connectors of type IDC34 (line input, line output, and ECLine discriminator output) for 17-pair flat twisted-pair cables, and a LEMO connector for the OR (in NIM standard) of the timing discriminator outputs. The latter was used for triggering purposes.

Signals from 16 summing preamplifiers SP8 are received through the first IDC34 connector to 50 Ω line inputs of the path-splitting section of the SSD16. One signal path is the timing path, the other the charge path.

The timing path consists of a fast amplifier and a voltage comparator. The amplifier uses an AD8009AR chip in non-inverting mode. The voltage amplification factor is 10, the slew rate is 5.5 V/ns, and the rise time is 1.2 ns. The discriminator uses one half of an AD96687BR double-comparator chip. The differential ECLine output discriminators have a pulse width of 100 ns. The signals were sent over 80 m long twisted-pair cables to commercial TDCs[1].

The charge path consists of a charge-sensitive inverting amplifier with voltage amplification by a factor of ~ 2, and of charge amplification by a factor of ~ 10. The amplifier output is connected to a passive pseudo-differential driver that provides a symmetric signal for transmission in a 80 m long twisted-pair cable. The transformation of the amplifier signal into a pseudo-differential signal, and the use of a commercial 16-channel impedance adapter[2] caused a charge reduction by a factor of 4. The impedance adapter was to bridge the 110 Ω impedance of the twisted-pair cable to the 50 Ω single-input of the QDC[3].

Table 2 summarizes the characteristics of the SSD16 splitter module. Figure 4 shows a simplified scheme of the 16-channel splitter SSD16, and Fig. 5 demonstrates its intrinsic timing performance.

The average intrinsic RPC time resolution achieved with physics tracks in the HARP experiment, using the described readout electronics, was 127 ps [6], much better than the 200 ps specified at the design stage of the experiment.

[1] C.A.E.N. V775
[2] C.A.E.N. A922
[3] C.A.E.N. V792

Table 2: Characteristics of the SSD16 Splitter Module.

Timing path	
Equivalent input threshold range	(1–10) mV
Threshold skew (100 channels)	$< 5\%$
Voltage-amplification factor	10
Discriminator threshold	50 mV
Channel-to-channel cross talk	-40 dB
Intrinsic I/O time skew	15 ps r.m.s.
Equivalent input noise	< 500 μV r.m.s.
Output signal width	100 ns
Line input resistance	50 Ω
Charge path	
Voltage-amplification factor	~ 2
Charge-amplification factor	~ 10
Output pulse width	250 ns
Output impedance	110 Ω
Power supply current (+6 V / -6 V)	0.9 A / 2.1 A

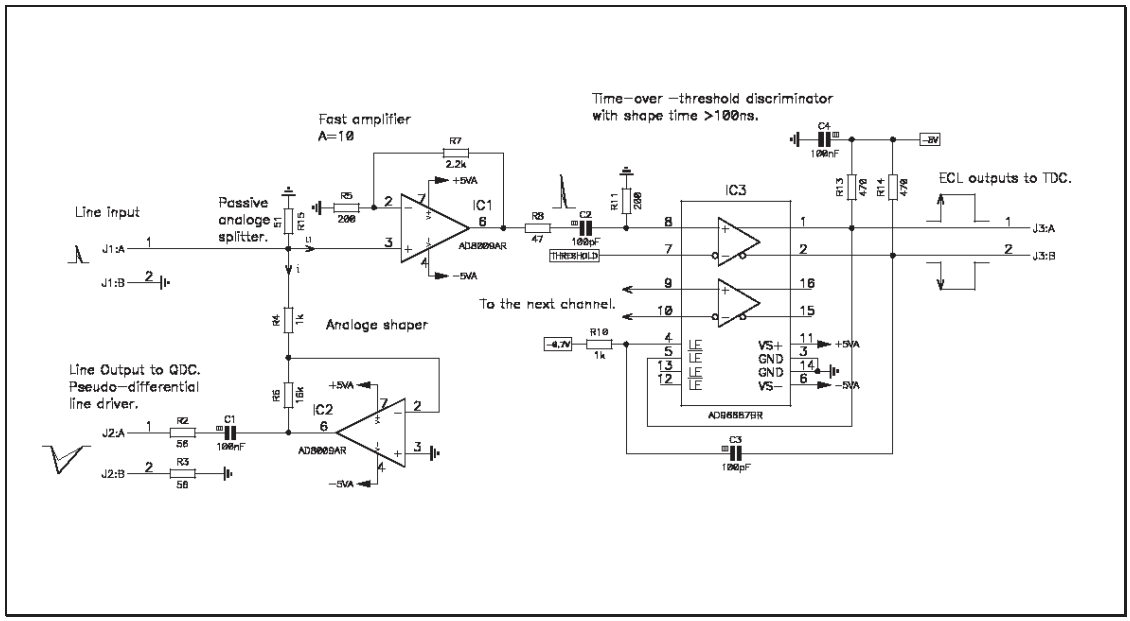

Figure 4: Simplified scheme of the 16-channel splitter SSD16.

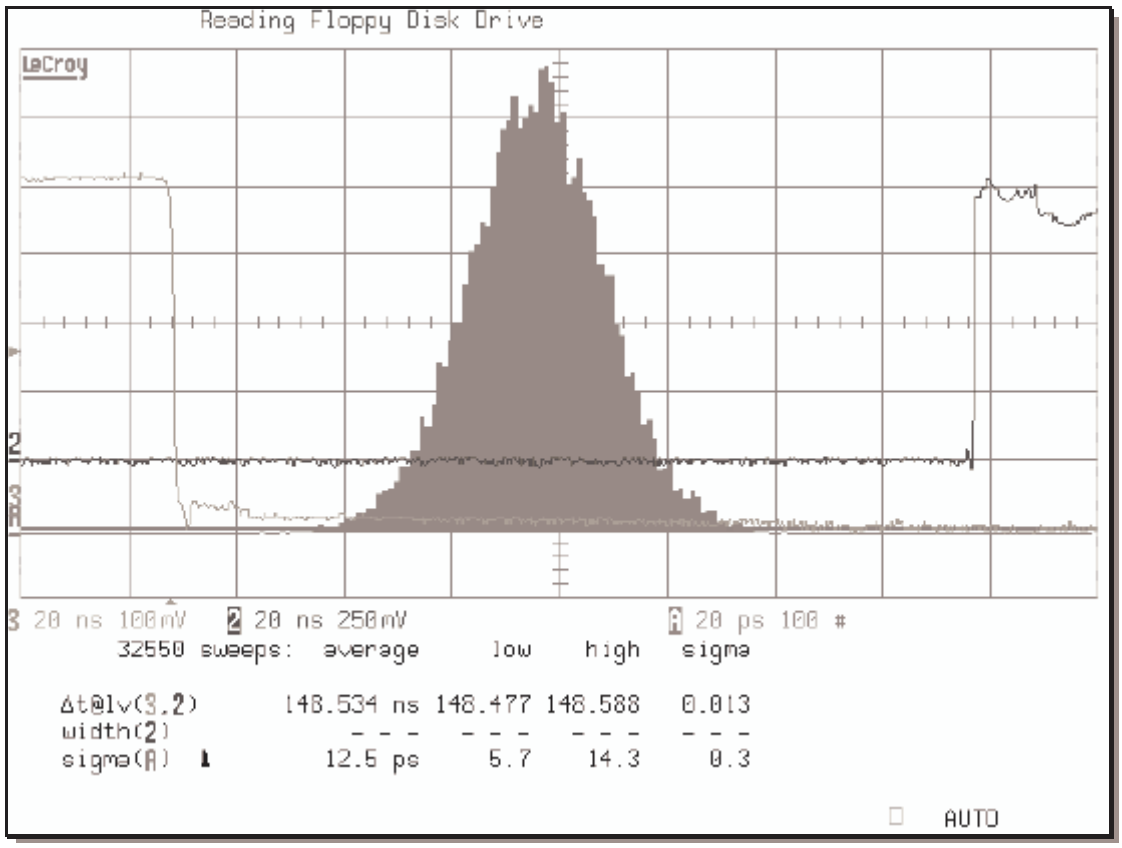

Figure 5: Intrinsic time resolution of the SP8 together with the SSD16, as determined with pulses from a LeCroy LC574A unit; the input signal in one input of the SP8 shown on line 3 corresponds, after differentiation with a 1 pF capacitor, to $Q_{\rm in} = 480$ fC; the output signal is shown on line 2.

References

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[3] M. Bogomilov *et al.*, "The HARP RPC time-of-flight system", Nucl. Instrum. Methods Phys. Res., vol. **A508**, pp. 152–158, 2003.

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[6] I. Boyko *et al.*, "The HARP resistive plate chambers: characteristics and physics performance", submitted to Nucl. Instrum. Methods Phys. Res. **A**.