

ANALOG DESIGN FOR CMOS VLSI SYSTEMS

by

Franco Maloberti

*Texas A & M University, U.S.A. and
University of Pavia, Italy*



KLUWER ACADEMIC PUBLISHERS
BOSTON / DORDRECHT / LONDON

CONTENTS

Preface

xi

Chapter 1

The MOS Transistor

1

- 1.1 Electrical Conduction in Solids 1
- 1.2 Fermi-Dirac Statistic 3
- 1.3 Properties of Materials 10
 - 1.3.1 Silicon 10
 - 1.3.2 Silicon dioxide 14
 - 1.3.3 Polysilicon 16
 - 1.3.4 Silicon Nitride 17
- 1.4 CMOS Technology 18
- 1.5 MOS Threshold Voltage 19
- 1.6 I-V Characteristics 26
 - 1.6.1 Weak Inversion Region 27
 - 1.6.2 Linear (or Triode) Region 28
 - 1.6.3 Saturation Region 30
- 1.7 Equivalent Circuits 32

- 1.7.1 Large Signal Equivalent Circuit 32
- 1.7.2 Small Signal Equivalent Circuit 35
- 1.8 More Sophisticated Models 39
- 1.9 Noise 45
- 1.10 Layout of Transistors 49
- 1.11 Design Rules 53
- 1.12 References 55
- 1.13 Problems 55

Chapter 2

Resistors, Capacitors, Switches

59

- 2.1 Integrated Resistors 59
 - 2.1.1 Accuracy of Integrated Resistors 63
 - 2.1.2 Layout of Integrated Resistors 69
- 2.2 Integrated Capacitors 72
 - 2.2.1 Accuracy of Integrated Capacitors 75
 - 2.2.2 Layout of Integrated Capacitors 78
- 2.3 Analog Switches 81
 - 2.3.1 Charge Injection 86
 - 2.3.2 Charge Injection Compensation 89
- 2.4 Layout of Switches 94
- 2.5 References 95
- 2.6 Problems 95

Chapter 3

Basic Building Blocks 99

- 3.1 Inverter with Active Load 99
 - 3.1.1 Small Signal Analysis 101
 - 3.1.2 Noise Analysis 107
 - 3.1.3 Design of Inverters with Active Load 109
- 3.2 Cascode 114
 - 3.2.1. Small Signal Analysis 115
- 3.3 Cascode with Cascode Load 121
 - 3.3.1 Small Signal Analysis of Cascode Gain Stages 127

- 3.3.2 Gain Enhancement Techniques 131
- 3.4 Source Follower 136
- 3.5 Threshold Independent Level-shift 141
- 3.6 Improved Output Stages 142
 - 3.6.1 Source Follower with Local Feedback 143
 - 3.6.2 Push-Pull Output Stage 146
- 3.7 References 151
- 3.8 Problems 151

Chapter 4

Current and Voltage Sources

155

-
- 4.1 Current Mirrors 155
 - 4.1.1 Simple Current Mirror 156
 - 4.1.2 Wilson Current Mirror 160
 - 4.1.3 Improved Wilson Current Mirror 163
 - 4.1.4 Cascode Current Mirror 165
 - 4.1.5 Layout of Modified Wilson and Cascode Current Mirrors 167
 - 4.1.6 Modified Cascode Current Mirror 168
 - 4.1.7 High Compliance Current Mirror 171
 - 4.1.8 Enhanced Output-Impedance Current Mirror 173
 - 4.1.9 Current Mirrors with Adjustable Mirror Factor 176
 - 4.2 Current References 178
 - 4.2.1 Simple Current Reference 178
 - 4.2.2 Self Biased Current Reference 180
 - 4.2.3 Self Biased Micro-Current Generator 184
 - 4.2.4 Start-up Circuits 188
 - 4.2.5 Use of Parasitic BJT for Current Reference 190
 - 4.2.6 V_{BE} Based Current Reference 190
 - 4.2.7 V_T - Bases Current Reference 192
 - 4.3 Voltage biasing 196
 - 4.3.1 Voltage Divider 197
 - 4.3.2 Diode-Connected Voltage Bias 201
 - 4.4 Voltage References 201
 - 4.4.1 V_{BE} Multiplier 202
 - 4.4.2 V_T Multiplier 203
 - 4.4.3 Voltage Reference Based on Threshold Difference 204
 - 4.4.4 Band-Gap Reference Voltage 205
 - 4.4.5 Curvature Error 212

- 4.5 References 213
- 4.6 Problems 214

Chapter 5

CMOS Operational Amplifiers

217

- 5.1 General Issues 217
- 5.2 Performance Characteristics 221
- 5.3 Basic Architecture 228
- 5.4 Two Stages Amplifier 229
 - 5.4.1 Differential Gain 230
 - 5.4.2 Common Mode dc Gain 230
 - 5.4.3 Offset 231
 - 5.4.4 Power Supply Rejection 235
 - 5.4.5 Effect of External Components on the PSRR 240
- 5.5 Frequency Response and Compensation 242
- 5.6 Slew Rate 255
- 5.7 Design of a two stage OTA: Guidelines 258
- 5.8 Single Stage Schemes 259
 - 5.8.1 Telescopic Cascode 259
 - 5.8.2 Mirrored Cascode 265
 - 5.8.3 Folded Cascode 269
 - 5.8.4 Single Stages with Enhanced dc Gain 273
- 5.9 Class AB Amplifiers 277
 - 5.9.1 Two Stages Scheme 278
 - 5.9.2 Unfolded Differential Pair 280
 - 5.9.3 Single Stage AB-class OTA 282
- 5.10 Fully Differential Op-Amps 286
 - 5.10.1 Circuit Schematics 286
 - 5.10.2 Common Mode Feedback 289
 - 5.10.3 Continuous-time Common-mode Feedback 291
 - 5.10.4 Sampled-data Common-mode Feedback 295
- 5.11 Micro-Power OTA's 297
 - 5.11.1 Dynamic-biasing of the Tail Current 298
 - 5.11.2 Dynamic Voltage Biasing in Push-pull Stages 299
- 5.12 Noise Analysis 301
- 5.13 Layout 308
 - 5.13.1 Parasitic Effects 308

- 5.13.2 Stacked Layout 313
- 5.14 References 319
- 5.15 Problems 320

Chapter 6

CMOS COMPARATORS 325

- 6.1 Introduction 325
- 6.2 Performance Characteristics 326
- 6.3 General Design Issues 330
 - 6.3.1 Architecture of the Gain Stage 331
- 6.4 Offset Compensation 333
 - 6.4.1 Implementation of the Auto-zero Technique 335
 - 6.4.2 Auto-zero in Multi-stages Architectures 339
 - 6.4.3 Fully Differential Implementation 341
 - 6.4.4 Use of an Auxiliary Stage 346
- 6.5 Latches 349
- 6.6 References 356
- 6.7 Problems 356

Appendix A 359

Appendix B 361

Appendix C 365

Index 369
