Results from the Commissioning of the ATLAS Pixel Detector

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***Abstract*—The ATLAS pixel detector is the innermost tracking detector of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. It has a total active area of 1.7 m^2 of silicon read out by approximately 80 million electronic channels, which will detect particle tracks and decay vertices with a very high precision. After more than 10 years of development and construction it is the first time ever the whole detector has been operated together. The paper will illustrate the detector performance and give first results from the combined ATLAS cosmics runs.**

I. Introduction

Many ATLAS physics analyses require precise determination of vertices for pattern recognition near the collision point. A vertex resolution below 12 μm, high granularity and efficiency combined with low mass of the detector material are needed for that. The search for rare events drives proton-proton collisions to take place every 25 ns at the full LHC luminosity of 10^{34} $cm^{-2}s^{-1}$, which requires fast hit identification. Selection of interesting events with the latency of 3.2 μs requires local buffering in the readout electronics. Most important is the tolerance of the 500 kGy radiation dose expected over the lifetime period of about 10 years. The pixel detector, employing silicon pixel hybrid technology, has been designed to fulfill these demands [1], [2].

II. The Pixel Detector

The pixel detector (Fig. 1) consists of three barrel layers at radii 5, 9 and 12 cm and two endcaps of three disks each. This geometry guarantees at least three pixel hits in the pseudorapidity range of interest of $|\eta| < 2.5$. The 1744 identical modules are mounted on a carbon support structure with the integrated C_3F_8 evaporative cooling. The detector building element is a *stave* with 13 modules for the barrel and a *sector* with six modules for the disks. Two neighboring staves (or sectors) share a *cooling loop*. During operation the module temperature will be kept at about -10 °C to minimize irradiation effects.

A. The Pixel Module

The pixel module (Fig. 2) is the smallest unit of the detector. Its main component, a silicon sensor, consists of n^+ implants on an n bulk with a p^+ backplane. The sensor has an active area of 6.08 cm $\times$ 1.64 cm and 250 μm thickness. Normal

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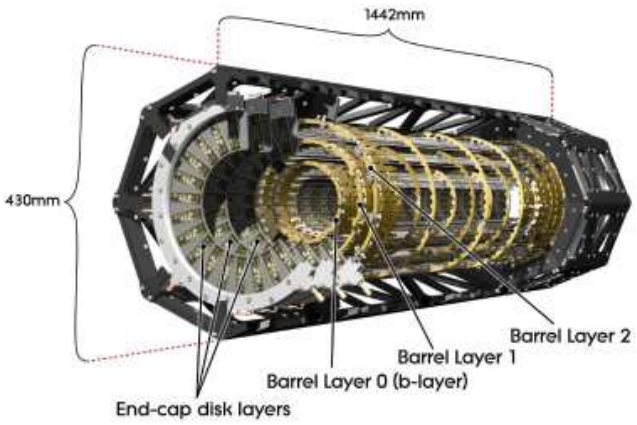

Fig. 1. View of the ATLAS pixel detector, [2].

pixel implantations have 400 μm $\times$ 50 μm size. The sensor technology is optimized for radiation hardness. The sensor is read out by 16 front end chips arranged in two rows and bump-bonded to the sensor. Each of the 46080 readout channels has an individually adjustable preamplifier and discriminator. For signals above the discriminator threshold the hit information, which contains the hit address, timestamp and collected charge in form of *Time-Over-Threshold (ToT)*[1], is stored in the on-chip buffer for 6.4 μs. The front end chips are wire-bonded to the flexible multi-layer PCB (flex), which is glued to the backside of the sensor and used to route signal and power lines. On the top of the PCB, a *Module Control Chip (MCC)* is mounted, which distributes *Timing, Trigger and Control (TTC)* signals to the front end chips and builds a module event from their data upon reception of a *Level One (LVL1)* trigger signal. The MCC can replicate a trigger signal up to 15 times, which allows readout windows of up to 400 ns. The PCB also houses decoupling capacitors and an NTC for temperature measurement. The barrel modules possess additionally another flexible layer, a pigtail, with a connector for a low-mass cable. This cable, used for the connection of modules to the *Patch Panel 0 (PP0)*, is directly soldered on the PCB for the disk modules.

B. Off-detector Readout

An optical signal transmission is used for the communication between modules and off-detector readout electronics,

[1]ToT is measured in units of *Bunch Crossings (BC)*, with 1 BC equal to 25 ns.

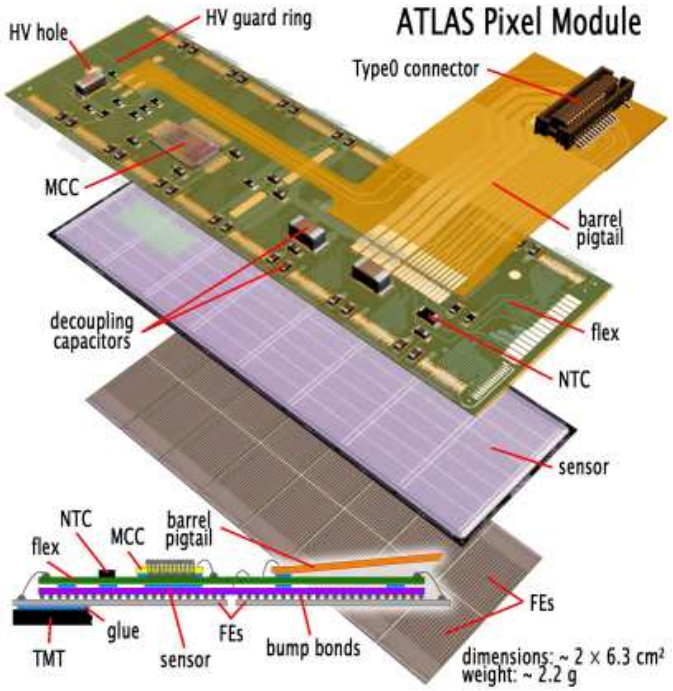

Fig. 2. Components of the pixel barrel module (disk modules have no pigtail), [2].

as shown in Fig. 3. It employs GaAs *Vertical Cavity Surface Emitting Lasers (VCSELs)* with the wavelength of 850 nm and epitaxial silicon PiN diodes. About 80 m of partially radiation-hard fibers interconnect 132 *Back Of Crate cards (BOCs)* in the racks in the USA15 cavern and 272 optoboards on the detector side. The number of connections per BOC depends on the readout speed, which at the full LHC luminosity will be 160 MBit/s for the B-Layer, 80 MBit/s for the Layer 1 and the disks and 40 MBit/s for the Layer 2 modules. On the detector side a group of six or seven modules, corresponding to either a disk sector or a barrel half-stave, is connected by LVDS cables to the PP0 and from there to the optoboard. There is one control fiber and one (or two in the case of the B-Layer) data fiber per module.

The 40.08 MHz clock and control signals are *BiPhase Mark (BPM)* encoded in a TX plug-in on the BOC and sent down to the optoboard where they are decoded by the *Digital Opto-Receiver Integrated Circuit (DORIC)* and transferred to the module. The module differential data output is converted into single-ended current signals in the *VCSEL Driver Chip (VDC)* driving a VCSEL array. Output power of the array is controlled by the VIset voltage, which is common to all channels of the optoboard. Data are received by an RX plug-in of the BOC on the off-detector side, where the phase between the data and the sampling clock needs to be adjusted per channel.

The pixel detector data are processed by 132 *ReadOut Drivers (RODs)*, each being a counterpart to the BOC in the readout crates. Each of a total of nine readout crates houses additionally one *Single Board Computer (SBC)* and one *TTC Interface Module (TIM)*, which interfaces a TTC crate. This crate, organized into three partitions (according to B-Layer, Layer 1 and Layer 2, Disks) distributes TTC signals from the

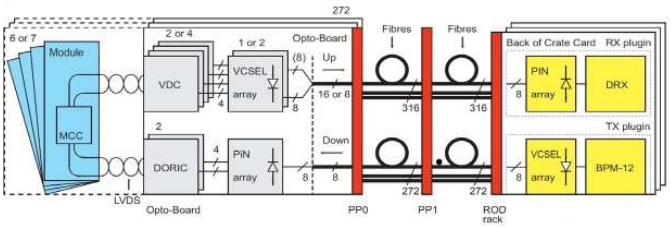

Fig. 3. Optical communication between modules and off-detector readout electronics, [2].

Central Trigger Processor (CTP) and collects BUSY signal from the RODs, which, being transmitted to the CTP, can stop global ATLAS data acquisition. The core of each partition is a *Local Trigger Processor (LTP)*, which can also generate the TTC signals locally. This capability is used in standalone data taking runs.

The readout of the pixel detector can be operated in a data taking or in a calibration mode. In data taking mode the RODs receive LVL1 triggers from the TTC crate and build local events from the received module data. These events are sent through the S-Link to the *ReadOut System (ROS)*, where, depending on the *Level Two (LVL2)* trigger decision, they will be either included into the ATLAS event or discarded. In calibration mode, trigger and control signals are generated in RODs and module events are sent through the VME bus to the SBC for further processing. Since the amount of data generated in calibration procedures is huge, DSP processing on the RODs is employed. The typical DSP processing tasks are histogramming, averaging and fitting of module data, which considerably increases the speed of calibration procedures.

III. Commissioning

The assembly of the pixel detector package was completed in spring 2007 and the package was installed in the ATLAS cavern in June 2007 [3]. The package includes the complete detector and the central ATLAS beryllium beam pipe. During the second half of the year 2007 all electrical services were installed, verified and calibrated using dummy-loads. Simultaneously the off-detector readout electronics were installed in the cavern. It was included into the global ATLAS readout chain and signed-off with the simulated raw data input both in the standalone and combined ATLAS test runs.

A. Connection and Cooling Operation

The connection of the pixel detector package to the cooling, services and off-detector readout electronics began in February 2008 because the connections of the other ATLAS sub-detectors had to be finished first. Full connection, accompanied by performance checks, was accomplished by April 2008. A photograph of the PP1 area (only 0.5 m in diameter) after the connections were made is shown in Fig. 4.

During the sign-off period the cooling loops were commissioned by a variation of the heat load using special module configurations. Some loops showed instability if the detector was switched off, however, after modification of the cooling regulation the system is working more reliably. The

Fig. 4. A photograph of the PP1 area after connection.

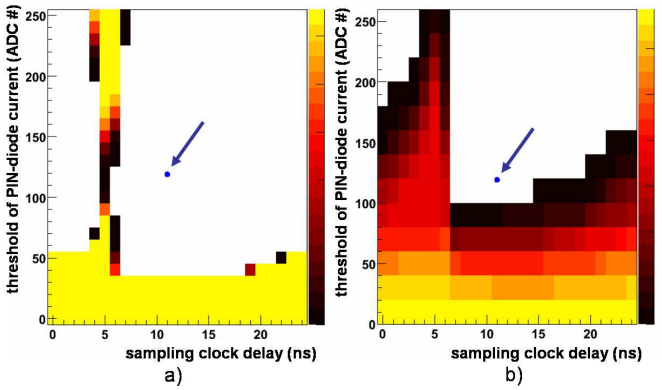

Fig. 5. Scan of the RX plug-in parameter space for the determination of an error-free region (white area) for the optical tuning. The number of bit errors is color-coded. A half-clock data pattern is used for each scan point in a) and a pseudorandom data pattern in b). The non optimal operating point chosen by the tuning algorithm is shown by the blue dot marked with the arrow.

commissioning of the cooling plant was concluded by the end of August 2008 and all 88 cooling loops could be operated. Three cooling loops in the endcaps were found to be leaky and switched off until the ATLAS 2008/2009 winter shutdown, after calibrating the corresponding modules. Further leak rate measurements will be made during the shutdown and we expect to operate these loops in 2009. Temperature regulation is achieved by adjusting the pressure at the exhaust of the cooling circuits (back-pressure). During commissioning tests, described below, it was set to 3 bar absolute, resulting in the operational temperature of -3 °C for most of the barrel modules and -6 °C for the disk modules. We expect to operate about 10 °C colder in 2009 (with the back-pressure of 2 bara).

B. Tuning of Optical Connections

Optoboard temperature was found to be a critical parameter for reliable operation of the optical connections between on- and off-detector electronics during the system test in 2006 [4]. As a result, the pixel package was equipped with an optoboard temperature control system. The temperature of the optoboards must be kept as low as possible to reduce irradiation effects. Therefore as soon as the cooling was available, optical connection tuning at 10 °C was performed. Since several channels have shown a slow turn-on behavior[1], it was decided to raise the optoboard temperature to about 20 °C. As a result, about 95% of the optical connections were tuned using an existing tuning procedure, described in [5]. This procedure scans a three dimensional parameter space: the VIset parameter of the optoboard, the sampling clock delay and the threshold of the PIN diode current in the RX plug-in. For each scan point a data pattern, consisting of alternating zeros and ones (so called half-clock pattern), is sent to the BOC and number of bit errors in the data transmission is counted. For each VIset value a plot similar to one shown in Fig. 5a is obtained. Using this information an algorithm defines an operating point, which is then validated. This operating point is not always correctly chosen. Fig. 5b compares this to the error-free region of another scan, employing a pseudorandom data pattern for each scan point. This second scan is better at mimicking the real data transmission. Clearly, the operating point was chosen too close to the error-band for this channel. Another complication is that some optoboard channels have significant spread in the output power and are therefore difficult to manage with automatic tuning. Improved optotuning algorithms employing among other things a pseudorandom data pattern are under development.

During the connectivity test during detector assembly it was found that the light output power of some TX channels can suddenly drop and remain in a low state resulting in a non-operational optical connection. The number of such channels increases during the operation with the rate of a few new dead channels per month. The effect is caused by ESD damage of the TX plug-ins during production. New TX plug-ins are being produced and used for gradual replacement of the faulty transmission channels (about 50 reported in November 2008).

C. Analogue Performance

The analogue performance of a pixel is measured using an injection circuit, which injects a pulse of a known charge into the preamplifier. By repeating the injection and scanning the range of applied charge, one can measure the discriminator threshold and the noise level of the channel. This scan, known as the threshold scan [2], is also employed for validation of the threshold tuning. In Fig. 6a the threshold distribution of pixels with the tuning from the module production back in 2005-2006 is shown. Tuned to a target threshold of 4000 e^- at about 20 °C, the tuning results are also known to be different between production institutes. As only this tuning was available when we began acquiring muon tracks, it was used until the end of the combined data taking period. With the threshold tuning algorithm, it is possible to tune 74.8 million channels (93% of the detector) to a very low threshold dispersion of only 37 e^- (Fig. 6b). The threshold-to-noise ratio was measured to be about 24 for most of the pixels for the target threshold of 4000 e^-. The tuning algorithm still needs to be improved especially in order to tune the pixels to lower thresholds. Another tuning tunes the preamplifier response to a certain input charge by adjusting the preamplifier feedback

[1]Optoboard lasers need significant amount of time, about 10 to 100 μs, to reach the full output power.

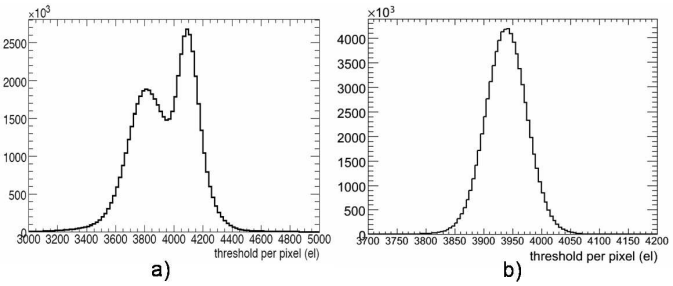

Fig. 6. Threshold distributions of the pixels using production tuning a) and $in\ situ$ tuning b).

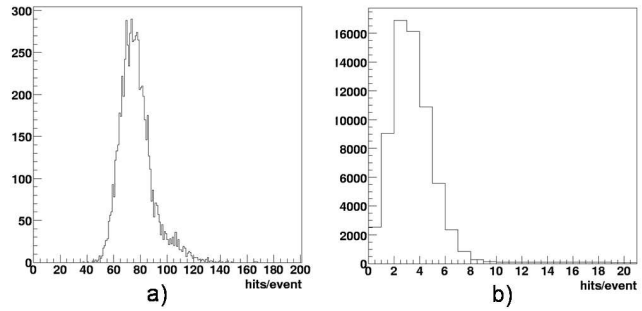

Fig. 7. Number of hits per event before a) and after b) masking of pixels with a noise occupancy above 10^{-5}. The readout window is 200 ns.

current. In the 250 μm pixel sensor the most probable energy loss for 1 MIP is 20 ke^-. By injecting this charge into the preamplifier, the pixel response is tuned to 30 ToT. In this case, the tuning from the module production was also used for the cosmics data taking.

D. Noise Occupancy

The noise occupancy is measured by reading out the detector randomly. For this purpose, standalone data taking runs with trigger frequency of several kHz are used. After disabling the few modules, which stop the readout, stable data taking was achieved and data samples were recorded. Based on these samples noise occupancy per pixel was calculated and the noisy pixels map, containing only the pixels, which had an occupancy greater than 10^{-5}, was created. It contains only about 5000 pixels, which were masked. After applying the masking, the noise occupancy dropped by a factor of 20, as shown in Fig. 7, to about 0.5 hits per event per 25 ns readout window for the whole detector. This corresponds to about $6 \cdot 10^{-9}$ noise occupancy per pixel per BC for the whole detector. The reduction of noise by applying the noise mask also confirms the fact that most of the noise has a fixed-pattern origin. The noise mask is updated on a regular basis.

E. Combined ATLAS Cosmics Data Taking

The pixel detector participated in the combined ATLAS data taking runs for the first time in the beginning of September 2008. After adjustment of the trigger latency, first muon tracks through the pixel volume were recorded. The LVL1 triggers were provided mostly by the ATLAS muon spectrometer

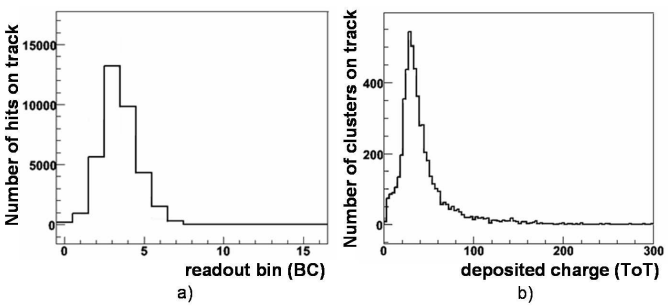

Fig. 8. Number of hits on tracks as a function of position in readout window a) and the ToT distribution of clusters on tracks b).

systems and distributed to the sub-detectors by the CTP. When each trigger is received from the CTP, a time window of 200 ns (or 8 BC) is read out by the pixel modules. Additionally, to increase the dynamic range of the signal, the maximal front end readout latency of 255 BC was used, which required delaying of the trigger signals from the CTP. Before switching off the leaky cooling loops, about 95% of the detector modules were operated in data taking. The commissioning of the LVL2 trigger allowed a cosmic muon track rate through the pixel volume of 0.3 Hz to be reached. In total during the ATLAS combined cosmic runs in September - October 2008 about 250000 pixel tracks with and without magnetic field were collected. This corresponds to about 100 - 400 hits on tracks per module, depending on the geographic position of the module in the detector. Horizontally oriented modules have approximately twice as many hits as vertically oriented ones; pixel endcap modules have significantly lower statistics. The efficiency from muon tracks hits crossing the pixel volume was found to be around 98%, close to the expected value of 99.9%. This depends on the efficiencies of other tracking sub-detectors and the tracking algorithm, which are still being optimized. Alignment studies of the pixel barrel are on-going, a significant bow of some staves with a sagitta of up to 400 μm has been found and is being corrected in the detector offline description. The timing of hits on tracks in the 8 BC readout window and the ToT distribution of pixel clusters are shown in Fig. 8. From the timing distribution one can suspect that the trigger jitter is significant and that there are almost no noise hits associated with the tracks. The ToT distribution of clusters on tracks peaks close to the expected value of 30 ToT. More results from offline analyses of the data are expected in the near future.

IV. Summary

The connection of cooling, electrical services and optical readout fibers to the ATLAS pixel detector, accompanied by performance tests, was finished by spring 2008. The whole detector was cooled and configured for the first time in August 2008. Before the first LHC beam, tuning of optical connections, verification of the analogue performance and special data taking runs for noise studies were performed. There are no data from the first splash beam events since the first beam, being unstable, did not allow the high voltage sensor bias to be switched on. In ATLAS combined data

taking runs, which followed, about 250000 cosmic tracks with and without magnetic field and with 95% of the detector operational were recorded. These data are very useful for offline analyses of the data, such as alignment, resulting in a more realistic detector description. Further calibration tests, optimization of the calibration procedures and recovery of malfunctioning modules are on-going.

ACKNOWLEDGMENT

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