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Multi-terminal dc grid overall control with modular multilevel converters

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This paper presents a control philosophy for multiterminal DC grids, which are embedded in the main AC grid. DC transmission lines maintain higher power flow at longer distances compared with AC lines. The voltage losses are also much lower. DC power transmission is good option for Russian north. Arctic seashore regions of Russia don't have well developed electrical infrastructure therefore power line lengths are significant there. Considering above it is possible to use DC grids for supply mining enterprises in Arctic regions (offshore drilling platforms for example). Three different control layers are presented in an hierarchical way: local, primary and secondary. This whole control strategy is verified in a scaled three-nodes DC grid. In one of these nodes, a modular multilevel converter (MMC) is implemented (five sub-modules per arm). A novel model-based optimization method to control AC and circulating currents is discussed. In the remaining nodes, three-level voltage source converters (VSC) are installed. For their local controllers, a new variant for classical PI controllers are used, which allow to adapt the values of the PI parameters with respect to the measured variables. Concerning the primary control, droop control technique has been chosen. Regarding secondary level, a new power flow technique is suggested. Unbalance conditions are also verified in order to show the robustness of the whole control strategy.

Key words: MMC; MT-HVDC grid; local control; DC connection; power flow calculation; voltage source inverters; droop control; hierarchical control

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Introduction. High voltage direct current (HVDC) networks are becoming a solution to energy transmission and distribution in our days. Indeed, they are a promising alternative to AC systems in some applications, as for example integration of renewable energy, or to link AC grids with different frequencies. This growth has been closely related to the huge development of power electronics and semiconductor devices in the few last years [4, 16]. Implementation of this technology covers long distances power transmission. The benefits are voltage and power losses minimization. These advantages allow to use DC power lines on Russian Arctic. Currently islet grids are used to supply mining enterprises on the north. Connection these enterprises with Russian national grid by means of DC lines is great opportunity to obtain sustainable development of these.

Nevertheless, the vast majorities of HVDC systems are only composed by two nodes (back-to-back operation mode). Some examples of these facilities are: the historical HVDC Gotland (1954), on the Swedish east coast, which could transfer 20 MW over 98 km submarine cables with a voltage of 100 kV [27], or more recently, the INELFE connection (2015) which links France and Spain with a nominal power higher than 1000 MW [4]. On the other hand, there are only a few multi-terminal HVDC facilities in our days: the QuebecNew England transmission line (1991) with a nominal power of 2250 MW and a voltage of 450 kV, or the Sardinia Corsica-Italy (1992) with a nominal power of 300 MW, 304 km and 200 kV of nominal voltage. Both of them have only three nodes, and they operate in multi-terminal mode during a limited time [12, 26]. Nowadays, there exists two multi-terminal high voltage direct current (MT-HVDC) grids completely operational: the NanAo Shantou grid with three nodes, and the Zhoushan islands grid with five terminals [13].

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For the further development of MT-HVDC, two aspects should be mainly enhanced. The first one is related with the coordination between the different devices. In this way the inter-actuation of their different controllers is still an open field. The second important task is related with protections. Unfortunately, the technology for the DC-circuit breakers is not completely mature.

Since MT-HVDC will be connected to the AC main grid, it is clear that, one of the main actors will be the AC/DC converter. Along the history of HVDC transmission systems, several types of converters and semiconductor devices have been utilized. The first converters operated with mercury arc valve technology, which were known as line-commutated converters (LCC). Later, thyristors replaced mercury in the LCC. However, as the LCC presented several limitations, and thanks to the development of fully-controlled power electronic devices, voltage source converters (VSCs) are widely used in several HVDC grids with IGBTs as semiconductor devices. In recent years, a new topology inside the family of VSCs is becoming popular, the modular multilevel converter (MMC) [7, 11, 17, 28]. The main advantages of MMC are the low harmonic distortion due to the multilevel configuration, no need for a bulk DC capacitor, quick response to changes in DC voltage level, power flow operating point and also DC circuit breaker capability, just to name a few [6, 10, 18].

In this paper, a whole control scheme for multi-terminal HVDC grids is presented, discussed and verified via experimental results. This control is checked in a three terminal scaled HVDC grid. The strategy discussed in this paper consists of three different layers, with different time scales [6, 8]. The reduced scale grid is composed by a MMC (five sub-modules per arm) and two three-level VSC. The main contributions of this paper may be summarized into the following:

• a novel model-based optimization method for output and circulating currents for MMC;

• experimental validation of a new algorithm to solve the power flow problem in mixed AC/DC grids;

• implementation and verification of an hierarchical controller for multi-terminal DC grids, which comprises from real time controllers until supervisor control.

This paper is outlined as follows: in section two the different control levels are discussed. In section three the three terminal test-bench is presented and their different devices. In section for the experimentations are shown, and finally in section five the conclusions are drawn.

Explanation of the control levels. The control proposed in this paper is divided in three different levels (local, primary and secondary) with different sample times.

Local controllers. The local controller is responsible for controlling the AC/DC converters. Its sample time is in the order of ms. According with the discussion in I, several topologies could be addressed for the AC/DC conversion, however, in this paper, we will only focus on a two-level VSC and the MMC. For VSC, the local controller commonly has two different layers, which depends on the dynamics of the variables to control (DC capacitor voltage or AC currents). These levels are: the inner, which is the faster and responsible for controlling the AC currents, and the outer, which controls the voltage [9]. On the other hand, VSCs have usually two different objectives: a) the control of the pair – DC voltage and reactive power-, in this case both inner as outer controller are involved, and b) the control of the pair – active and reactive power-. In this last case only the inner controller is implicated. These two different objectives will be explained in next two subsections.

With respect to MMC, and due to the nature of the generated current waves, one of the main control objectives is to reduce the circulating currents, because they increase the perturbations in the voltage of the capacitors, increasing the losses in the converter.

Local controller of VSC (pair VC and Q): In this case, there exists two different dynamics in the local controller; the VC (DC capacitor voltage) dynamic and the dynamic of the the current in the phase reactor inductor, which is related with the Q (reactive power). As explained before, both

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inner as outer controller are involved. There exist numerous studies in the literature for this type of control. For example, those which use a linear control around an equilibrium point (a different PI controller for each dynamic loop) [9], or those which use a non-linear control, and therefore the control range is valid for any value for the involved variables (or inside a pre-defined operation region obtained by theory) [21]. In both approaches, Park's transformation [23] is frequently used, and consequently *dq* frame is applied. In this paper, we consider the *dq* frame, and by means of classic Pulse Width Modulation (PWM) and a new variant for the linear PI controller, which permits to adapt the values of the PI parameters in function of the measured variables, the local controller is implemented as follows: In Fthe *dq* frame, the model of the VSC of node 1 is expressed in (1).

$$\begin{cases} \dfrac{di_q}{dt} = -\dfrac{R_f}{L_f} i_d - \omega i_q - \dfrac{M_d}{L} u_C + \dfrac{U_d}{L_f}; \\ \dfrac{di_q}{dt} = \omega i_d - \dfrac{R_f}{L_f} i_q - \dfrac{M_q}{L} u_C + \dfrac{U_q}{L_f}; \\ \dfrac{du_C}{dt} = \dfrac{3M_d}{2C} i_d + \dfrac{3M_q}{2C} i_q - \dfrac{1}{R_{DC\,grid} C} u_C, \end{cases} \tag{1}$$

where R_f and L_f are the AC phase reactor resistance and inductance respectively, C is the DC bulk capacitor, M_d and M_q are the control variables according with PWM technique, ω is the pulsation of the AC grid and R_{DC} is the Thevenin's resistance equivalent of the DC grid. All of these values are shown in table 1. On the other hand, i_d, i_q and v_C are the state variables.

In systems of equations (1) i_d and i_q are coupled. Elimination of cross-coupling effect could be achieved by forcing the control variables to be as

$$M_d = M'_d + \frac{L\omega}{u_C} i_q \quad \text{and} \quad M_q = M'_q + \frac{L\omega}{u_C} i_d .$$

Inner controller. As it has been explained before, the inner controller regulates the AC current. Considering that i_d and i_q are decoupled, then the active and reactive power could be controlled through the variables i_d and i_q. In this way, if the converter is modelled as a first order system with gain $v_C/2$ and delay (T_g) (this delay is linked with the frequency of the PWM triangular signal), and taking into account the PI controller parameters (K_{pq} and T_{iq}), then we obtain the following control loop as figure 1, *a*.

Consequently, the following transfer function is reached in open loop:

$$H(s) = \frac{u_C}{2}\left(\frac{1}{1+T_g s}\right)\frac{1}{R_f + L_f s} K_{p_q}\left(1+\frac{1}{T_{i_q} s}\right). \tag{2}$$

Applying classical PI tuning techniques, the PI parameter can be determined ensuring a phase margin of 60°, and a module for $|H(s)|$ equal to one, in order to guarantee the stability, as it is shown in (3):

$$K_{pq} = \frac{2L_f \omega_c \sqrt{1+\left(T_g \omega_c\right)^2}}{u_C}, \tag{3}$$

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Table 1

System parameters

	DC grid	
V_{DC}	Nominal DC voltage	150 V
P_{DC}	Nominal DC power	4 kW
	DC line	
R_1	Resistance DC line 1	0.6 Ω
L_1	Inductance DC line 1	10 mH
R_2	Resistance DC line 2	0.6 Ω
L_2	Inductance DC line 2	10 mH
R_3	Resistance DC line 3	0.6 Ω
L_3	Inductance DC line 3	10 mH
	LC filter	
L_{f1}	Inductance filter 1	20 mH
C_{f1}	Capacitance filter 1	0.4 mF
L_{f2}	Inductance filter 2	20 mH
C_{f2}	Capacitance filter 2	0.4 mF
	VSC converters	
$U_{\max}$	Maximum voltage	750 V
$I_{\max}$	Maximum current	30 A
C	DC bulk capacitor	3.3 mF
	MMC converter	
N	Number of sub-modules per arm	5
C_i	Sub-module capacitance	3.3 mF
R_{AC}	Resistance AC side (phase i)	10 Ω
L_{AC}	Inductance AC side (phase i)	0.1 H
	AC grid	
U_{AC}	Phase to phase (rms) AC voltage	127 V
ω	Pulsation	2π·50 rad/s
	AC phase reactor inductance	
R_f	Resistance AC phase reactor	0.142 Ω
L_f	Inductance AC phase reactor	0.01 H
	Step-down transformer	
n	Transformer ratio	127/50
S_n	Nominal complex power	3.5 kVA
R_f	Foucault losses	221 Ω
ωL	Magnetizing reactance	41 Ω
V_{sc}	Short-circuit voltage	5.7 V
	Anti-aliasing filters	
f_s	Sampling frequency	1000 Hz
R_{fanty}	Filter Resistance	3.38 kΩ
C_{fanty}	Filter Capacitor	47 nF

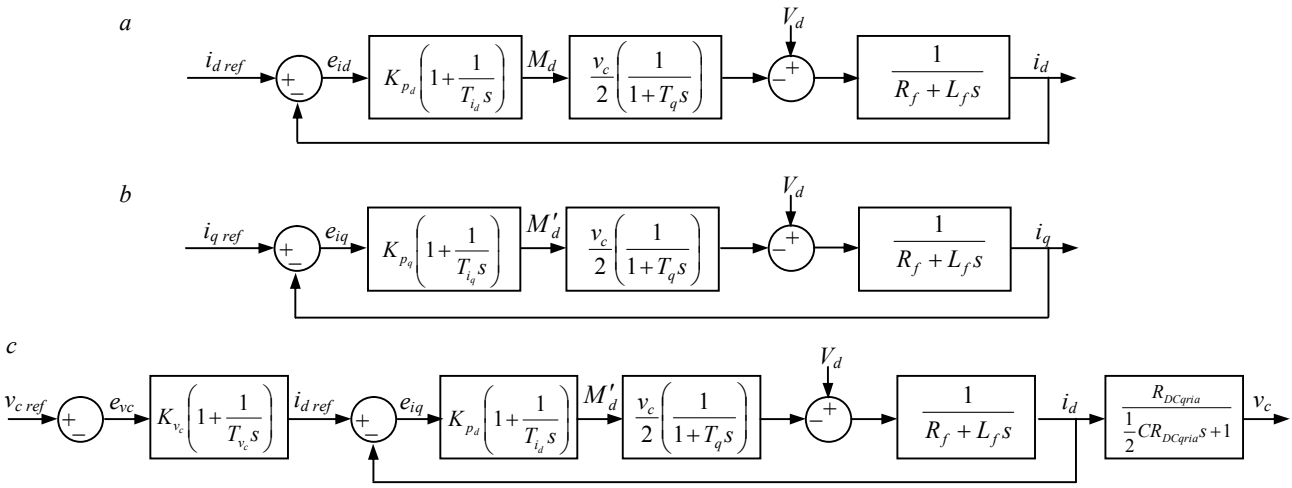

Fig.1. i_q current control loop (*a*), v_C control loop (*b*), i_d current control loop (*c*)

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where ω_c is the critical pulsation obtained with the parameters shown in table I and ensuring a phase margin of 60◦. Also, it is important to remark that in (3), K_{pq} depends on v_C. Therefore, it adapts its value in function of the DC voltage grid.

Outer controller: The outer controller is responsible for controlling the voltage in the DC capacitor. As in the third equation of (1), v depends on i_d, a inner control loops is also involved, as figure 1, *b* shows.

Since R_f and L_f do not vary, then ω_c is the same as the case of the inner controller. Applying the same techniques, we obtain similar expressions for K_{pd} and T_{id}. Once these values are calculated, and considering that the dynamics of id is much faster than the v_C, then the adjustment of the control parameters K_{vC} and T_{vC} could be carried out by Internal Model control theory [22, 24].

Local controller of VSC (*pair P and Q*). In this case, the pair P and Q will be controlled. The model for the VSC is shown in equation (1). From the control point of view, the only difference with the controller shown in previous sub-section is that there is not a voltage control loop, and id ref is given directly by the upper level controller (Fig.1, *c*).

Local controller of MMC. Schematic representation of the local control strategy for MMC is provided in Figure 2. It contains an output current controller and a circulating current controller. Reference signal for the output current controller is provided by the supervisor, while the reference circulating current is generated by a model-based optimisation method that is proposed by [19], where the aggregate and difference capacitance energy in each arm are taken into account (W^{Σ} and W^{Δ}).

Discrete-time mathematical model of the output current is provided by the following equation [3]:

$$i_{sk+1} = \left(1 - T\frac{R+2R_g}{L+2L_g}\right)i_{sk} + \frac{2T}{L+2L_g}u_{sk} - \frac{2T}{L+2L_g}\left(u_{gk} + u_{nmk}\right), \tag{4}$$

where T is the sample time, vg is the phase to ground AC voltage, and R_g and L_g are respectively the resistance and inductance of the AC grid.

Equation (4) has been obtained considering the following change of varibales:

$$i_s = i_u - i_l, \tag{5}$$

$$u_S = \frac{u_l - u_n}{2}, \tag{6}$$

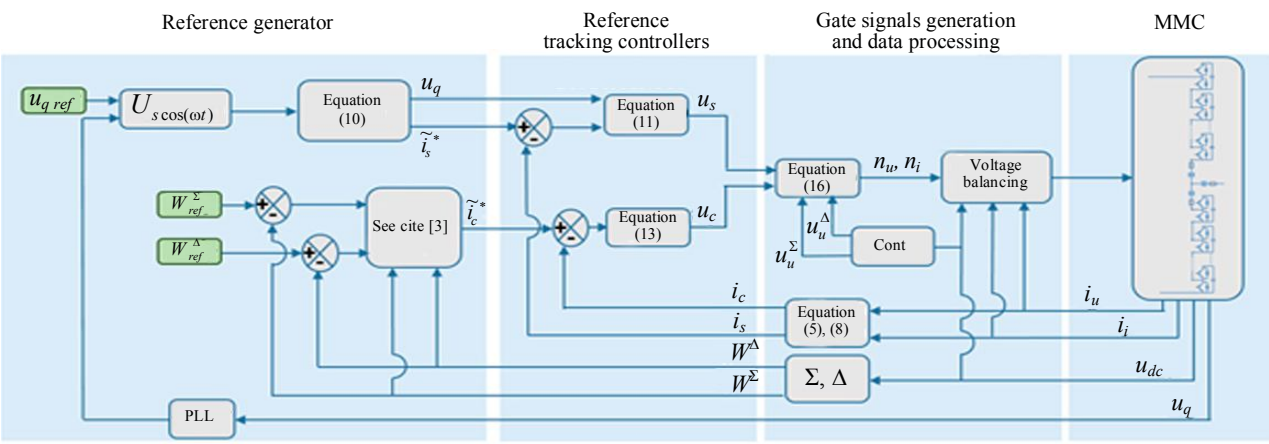

Fig.2. Block diagram of the proposed control strategy for the MMC

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Indices k and $k + 1$ indicate values of the corresponding variable at two consecutive sampling instants. Voltage between the neutral n and the DC-bus mid-point m is denoted by v_{nm}, and it can be considered as a bounded additive disturbance [19].

The following equation characterizes the circulating current:

$$i_{ck+1} = \left(1 - \frac{TR}{L}\right) i_{ck} + \frac{T}{L} u_{ck}, \tag{7}$$

where

$$i_c = \frac{i_u + i_l}{2}, \tag{8}$$

$$u_c = \frac{u_{dc} - u_u - u_l}{2}, \tag{9}$$

and DC-bus voltage u_{dc} is assumed to be constant.

Let the reference output current be characterized by the following disturbance-free dynamics:

$$\tilde{i}_{sk+1} = \left(1 - T\frac{R + 2R_g}{L + L_g}\right)\tilde{i}_{sk} + \frac{2T}{L + 2L_g}\tilde{u}_{sk}. \tag{10}$$

In order to ensure that i_s follows $\tilde{i}_{sk}$, the following linear controller is proposed:

$$u_{sk} = \tilde{u}_{sk} + u_{gk} + K_p^s\left(\tilde{i}_{sk} - i_{sk} - \eta_s\right), \tag{11}$$

where η_s denotes bounded measurement noise. Replacing (11) in (4), and subtracting the result from (10), the following tracking error dynamics is obtained:

$$\tilde{i}_{sk+1} - i_{sk+1} = \left(1 - T\frac{R + 2R_g + 2K_p^s}{L + 2L_g}\right)\left(\tilde{i}_{sk} - i_{sk}\right) + \frac{2T}{L + 2L_g}\left(u_{nmk} + K_p^s\eta_s\right). \tag{12}$$

Based on (12), gain K_s p can be selected via the pole placement method.

For a bounded zero-mean additive disturbance v_{nm} and measurement noise η_s, control signal (11) is able to maintain i_s in a bounded set with the center in $\tilde{i}_{sk}$. Details on the characterization and construction of such a set can be found in [20].

For a given reference circulating current $\tilde{i}_c$, the following control signal v_c is obtained:

$$u_{ck} = K_p^c\left(i_{ck} + \eta_c\right) + K_i^c x_k^c, \tag{13}$$

where input η_c denotes measurement noise, while xc represents controller's state which is characterized by the following dynamics

$$x_{k+1}^c = x_k^c + T\left(\tilde{i}_{ck}^* - i_{ck} - \eta_c\right). \tag{14}$$

By replacing (13) in (7), while taking into account (14), one obtains the following closed-loop form:

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$$\begin{bmatrix} i_{ck+1} \\ x^c_{k+1} \end{bmatrix} = \begin{bmatrix} 1 - T\dfrac{R - K^c_p}{L} & \dfrac{TK^c_i}{L} \\ -h & 1 \end{bmatrix} \begin{bmatrix} i_{ck} \\ x^c_k \end{bmatrix} + \begin{bmatrix} 0 \\ h \end{bmatrix} \tilde{i}^*_{ck} + \begin{bmatrix} \dfrac{TK^c_i}{L} \\ -h \end{bmatrix} \eta_c . \tag{15}$$

By assuming that (15) is completely state controllable, control parameters K^c_p and K^c_i can be determined by using the pole placement method, and therefore the state matrix of (15) is asymptotically stable.

For every sampling period, control signals (11) and (13) are translated into insertion indices n_{uk} and n_{lk} according to the following mathematical expressions 16:

$$\begin{cases} n_{uk} = \dfrac{N}{u^{\Sigma}_u}\left(\dfrac{u_{dc}}{2} - u_{sk} - u_{ck}\right); \\ n_{lk} = \dfrac{N}{u^{\Sigma}_l}\left(\dfrac{u_{dc}}{2} - u_{sk} - u_{ck}\right). \end{cases} \tag{16}$$

Primary controller. Primary controller handles the voltage level of the whole DC grid. Among the possible candidates for the primary task [2, 5, 25], the droop control has been chosen, because it is able to adapt the DC voltage level of the grid when disturbances appear in the network.

With this approach, no communication between nodes is required. In addition, it is not necessary to implement the primary controller in all the nodes. The droop control is a well known technique, and it is governed by equation (17): it is also known as virtual impedance control [29], or adaptive voltage position [1].

The droop control technique is governed by equation:

$$v_{DC,j} = v^*_{DC,j} + \frac{1}{k_j}\left(i^*_{DC,j} - i_{DC,j}\right) \forall j \in D, \tag{17}$$

where $i_{DC,j}$ is the DC measured current in the DC part of the corresponding node j, $v_{DC,j}$ is the output of the primary controller (which will serve as voltage reference for the local controller $v_{C\,ref}$), $i^*_{DC,j}$ and $v^*_{DC,j}$ are respectively the references for the current and the voltage provided by the secondary controller and k_j is the droop gain with dimensions of [Ω − 1]. Finally D is the set of nodes where droop control is implemented.

In nodes where droop control is applied, and depending on variations in the current for each node, the voltage is adjusted following the droop law (17). In this way, the voltage level of the grid is maintained within a desirable value during a period time (the secondary sample time). On the other hand, each primary sample time, a voltage reference for the local controller is calculated. Therefore, to avoid problems of stability between primary and local controllers, the droop's dynamic is chosen slower than the dynamic of the outer controller in the local level.

For the scaled grid, the droop control is only applied in node 1 (see Fig.3). In addition, its sample time is around 1 *s*.

Secondary controller. The task of secondary controller is to supervise the operation of the whole grid. In this way, it periodically updates current and voltage data coming from each node. With these data, this secondary controller solves the power flow problem, and it sends accurate references foreach nodes. As a novelty in this paper, the resolution of the DC power flow problem, which is governed by a second order non-linear system of equations, is carried out by a new methodology whose theoretical development is explained in detail in [15]. This technique is based

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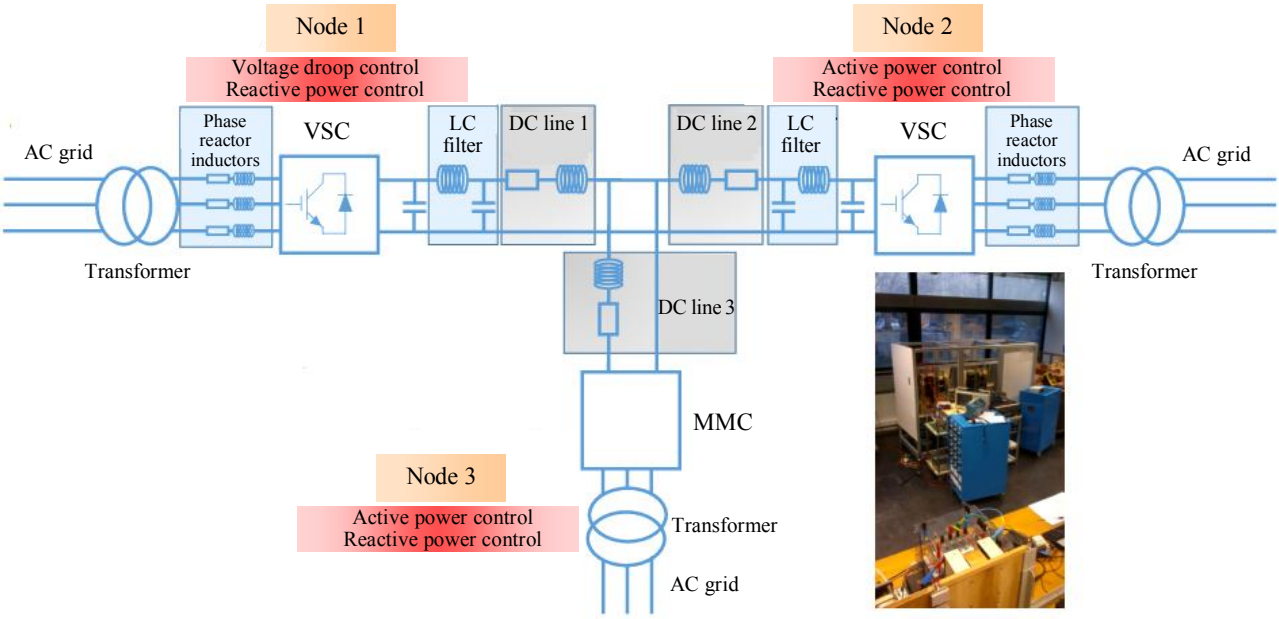

Fig.3. Three terminals test bench

on the fixed-point theorem of the contraction mapping. Therefore, this paper serves as a experimental verification of the method.

This new technique presents some important advantages. For example, if some mild constraints are fulfilled, the algorithm is always convergent and converges to a solution (which is unique). Besides, it needs less computational effort than others, because it does not use the inverse of a Jacobian matrix. Also, the number of iterations for a given error could be known a priori. Finally, this new algorithm allows to handle several slack buses, which are responsible for maintain the voltage of the grid. This last point fits perfectly with the philosophy of droop control, where several nodes are responsible for maintaining the voltage level.

A brief commentary for the main method's guidelines is given below. We can distinguish three different types of nodes: nodes where the load conductance (*LC*) is known, power reference (*PR*) nodes and voltage reference (*VR*) nodes. If the DC grid has n nodes, therefore, and taking into account that there are *m*, *j* and *n-m-j LC*, *PR* and *VR* nodes respectively, then the inputs for the algorithm will be: $g_1,.. g_m$ in *LC* nodes, $P_{m+1},.., P_{m+k}$ *PR* nodes, and $\omega_{m+k+1},.., \omega_n$ in *VR* nodes. Accordingly, once we know the line's parameters, we can express the conductance matrix of the network (where the known loads are included in the corresponding elements of the diagonal) in the following form:

$$G = \begin{bmatrix} G_{m+k} & -\Gamma_{m+k} \\ -\Gamma^T_{m+k} & \Lambda_{n-m-k} \end{bmatrix}, \tag{18}$$

where

$$G_{m+k} = \begin{bmatrix} g_{1,1} & .. & -g_{1,m} & -g_{1,m+1} & .. & -g_{1,m+k} \\ \vdots & .. & \vdots & \vdots & .. & \vdots \\ -g_{m,1} & .. & g_{m,m} & -g_{m+1,m} & .. & -g_{m,m+k} \\ -g_{m+1,1} & .. & -g_{m,m+1} & g_{m+1,m+1} & .. & -g_{m+1,m+k} \\ \vdots & .. & \vdots & \vdots & .. & \vdots \\ -g_{m+k,1} & .. & -g_{m,m+k} & -g_{m+1,m+k} & .. & g_{m+k,m+k} \end{bmatrix};$$

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$$\Gamma_{m+k} = \begin{bmatrix} g_{1,m+k+1} & .. & -g_{1,n} \\ \vdots & \vdots & \vdots \\ -g_{m+k+1,1} & .. & g_{n,n} \end{bmatrix};$$

$$\Lambda_{n-m-k} = \begin{bmatrix} g_{m+k+1,m+k+1} & .. & -g_{m+k+1,n} \\ \vdots & \vdots & \vdots \\ -g_{n,m+k+1} & .. & g_{n,n} \end{bmatrix}.$$

In consequence, the following non-linear system expresses the power flow behavior in the grid:

$$G_{m+k}U = \Psi(U) + \Gamma_{m+k}W, \tag{19}$$

where $U = [u1,.., um + k]$ and $W = [\omega m + k + 1,.., \omega n]$ represents the unknown and known voltages respectively. $\Psi(U)$ is defined as

$$\Psi(U) = \left[0,..,0,\frac{P_{m+1}}{u_{m+1}},..,\frac{P_n}{u_n}\right]. \tag{20}$$

In this way, for a given nominal voltage of the grid, and taking into account a few restrictions explained in [15], vector U is calculated by solving an algorithm based on the fixed-point theorem of the contraction mapping, in which all voltages are close to the nominal value. In addition, and with the purpose of avoiding non feasible solutions, rating constraints of each converter are considered in the formulation.

Three terminals test bench explanation. The DC reduced scale grid is composed by three AC/DC stations and three lines as the schema of figure 5 shows. The DC nominal voltage is 150 V, and the rated power is 4 *kW*. In nodes 1 and 2, three level VSC converters are inserted and in node 3 a MMC with 5 modules per branch is placed. The voltage levels of each external grid are the same (127 *V* RMS), and for appropriate converters' connection, step-down transformers are included. Afterwards, AC phase reactor inductors are introduced with the purpose of smoothing the currents and consequently achieving sinusoidal currents. In the DC side, each line is composed by inductor and resistors to be as close as possible to real transmission lines. Moreover, in nodes 1 and 2, physical *LC* filters are inserted aiming to achieve a more constant DC voltage. Finally, from the secondary controller point of view, node 1 is a *VR* node, and nodes 2 and 3 are *PR* nodes.

In the following, all test bench components are described with more detail.

• *Voltage source converters.* Three-level voltage source commercial converters are implemented in nodes 1 and 2. The IGBTs used are commercial devices: SEMISTACK-IGBT. They can support a maximum DC voltage of 750 V, and a maximum current of 30 A (rms). The three-level VSC are controlled in real-time thanks to commercial hardware DS1104 R&D. In this card, analogue signals from sensors are processed for the control in the PC (through MATLAB-SIMULINK and ControlDesk interfaces).

• *Modular multilevel converter.* As mentioned above, the scaled MMC consists of 5 submodules per branch. Each submodule has a half-bridge configuration, which is composed by IGBTs. In each sub-module there is a capacitor, which is the key element in this converter. Thanks to this capacitor, desired AC currents are obtained. The MMC is controlled through an OPAL-RT hardware, which is able to handle the high number of required signals for the MMC.

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• *Step-down transformers.* Step-down transformers are included in the system with the purpose of reducing AC voltages for the convenient use of the AC/DC converters. They have Δ/*d* configuration, and they provided galvanic isolation for each node.

• *AC phase reactor inductors.* With the aim of smoothing the AC currents, and reducing harmonic components, AC phase reactor inductors are inserted in nodes 1 and 2 (VSC nodes). It is important to remark that by using MMC, it is not necessary to include filters in the AC area.

• *LC filter*. In the DC side, and for a specification of a maximum ripple of 5 % in voltages and currents, physical LC filters are included in nodes 1 and 2. In this way, we can achieve a more constant voltage level in DC grid.

• *DC lines.* The DC lines are composed by real inductances and resistances in order to emulate the real transmission lines. Their values can be mechanically modified. Thereby, we can emulate multiple scenarios from the point of view of DC transmission lines.

• *Anti-aliasing filters*. In order to improve the control signals, analogue first order anti-aliasing filters are inserted in the hardware.

• *Secondary controller hardware.* The secondary controller is carried out by means of a supervisor *PC*, which calculates periodic power flows. In each sample time, 30 s, data from all nodes are received in the supervisor *PC* via Ethernet. After power flow calculations, the supervisor sends the new references to the three nodes via the same environment (Ethernet).

Experimental results. In this section the experimental results for the scaled DC grid are exhibited. The robustness of the hierarchical controller (which includes several control layers with different time scales) is verified under unbalanced conditions. The unbalanced circumstances are emulated in AC side of node 2, by means of forcing the node to consume zero power. The control parameters for each controller are shown in Table 2.

Table 2

Control parameters

VSC node 1		
Local controller		
h_{VSC}	Control sampling period	0.1 ms
f_{PWM}	PWM sawtooth waveform frequency	10 kHz
K_{pq}	Proportional action (axe *q*)	0.03
T_{iq}	Time constant of integral action (axe *q*)	0.002 s
K_{pd}	Proportional action (axe *d*)	0.03
T_{id}	Time constant of integral action (axe *d*)	0.002 s
K_{uc}	Proportional action (voltage)	0.14
T_{uc}	Time constant of integral action (voltage)	0.0005 s
Primary controller		
h_{pri}	Control sampling period	1 s
k	Droop	0.1 A/V
VSC node 2		
Local controller		
h_{VSC}	Control sampling period	0.1 ms
f_{PWM}	PWM sawtooth waveform frequency	10 kHz
K_{pq}	Proportional action (axe *q*)	0.03
T_{iq}	Time constant of integral action (axe *q*)	0.002 s
K_{pd}	Proportional action (axe *d*)	0.03
T_{id}	Time constant of integral action (axe *d*)	0.002 s
MMC node 3		
Local controller		
T	Control sampling period	50 μs
K_p^s	Proportional action (output current)	11.8
K_p^c	Proportional action (circulating current)	14.3
K_i^c	Integral action (circulating current)	6400
Secondary controllers (*MPC & TSO*)		
h_{sec}	Control sampling period	30 s

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In Figure 4, *a*, the powers in the converters are exhibited. The sign criterion is as follows, positive for incoming power in the DC side, and negative otherwise.

The experiment starts from an equilibrium state in t = 0 s (given by a past secondary reference), and approximately at t = 5.55 s a perturbation appears in node 2, which was consuming power from DC side (0.5 kW), and it begins to demand zero power. This is an unbalance condition, and therefore the primary control in node 1 detects that there is less power in the system and by means of the droop law, it orders to increase the voltage level in this node. Consequently, the grid's voltage grows until a new equilibrium point is achieved (Fig.4, *a*). Also, it is interesting to remark that thanks to the local controller of the MMC (node 3), the consumed power in this node remains constant, as shown in Figure 4.

At t = 15 s, and taking into account the system state, a new secondary reference is given for each node. These new references have been calculated without data of node 2, which is still under problems. Accordingly, nodes 1 and 3 receive the references calculated by means of solving a power flow problem, which guarantees an stable reference for the operation point of the whole grid.

At t = 31.7 s the node 2 is recovered, and it starts again to consume 0.5 kW. This fact is also a perturbation for the grid, and the droop control acts in node 1 and it decreases the grid's voltage because there is more power in the system. Once again, the primary controller leads the system to a stable point. However, this point could be not optimal or not advisable for the whole grid. For this reason, the secondary is implemented, which solves this issue in the following reference.

Finally, at t = 45 s a new secondary reference is given for all nodes, and a new stable equilibrium point is achieved.

In Figure 4, *b*, a zoom for the powers is shown. We can remark as the dynamics of the powers are faster in nodes where the current is controlled (nodes 2 and 3). With respect to the reactive power, all the references are always zero in all nodes.

In Figure 5, the voltage in node 1 is shown. Some zooms are illustrated in order to exhibit the dynamics of the primary controller at important moments of the experimentation. The voltage level is always close to the nominal value of the grid, but it varies in function of the droop law. However, the voltage in this node is always stabilized, and hence, the voltage of the grid.

In Figure 6, the voltage in the MMC capacitors of one leg are shown.

We can observe as the capacitors are always with the same voltage level, even if the power references for the MMC changes or if the DC voltage level of the grid varies. This fact shows the robustness of the MMC controller in particular, and the reliability of the proposed whole control in general.

In Figure 7, *a* the generated voltage between the upper and lower arm of phase A is shown. We can observe the five steps, which corresponds with the 5 sub-modules. These generated voltages (phases A, B and C) are responsible to create the AC currents at MMC node.

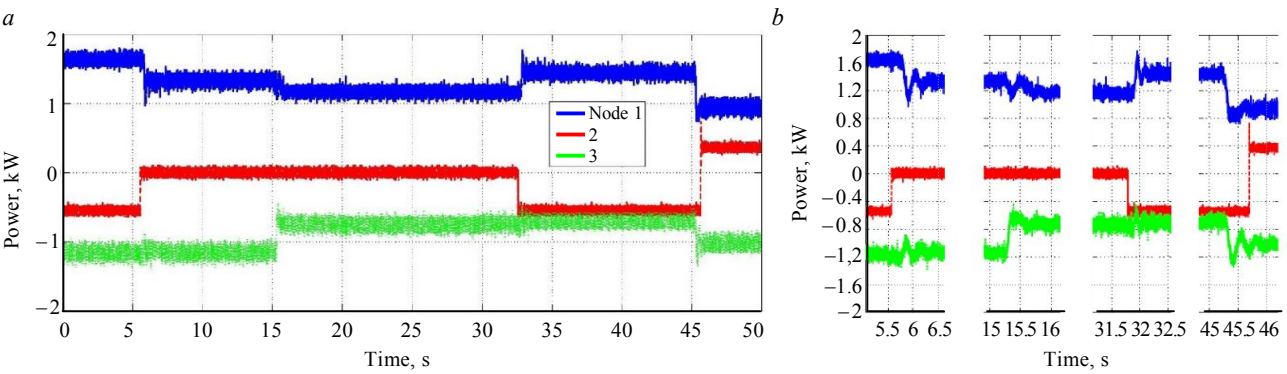

Fig.4. Powers in the converters (*a*), powers in the converters (zoom) (*b*)

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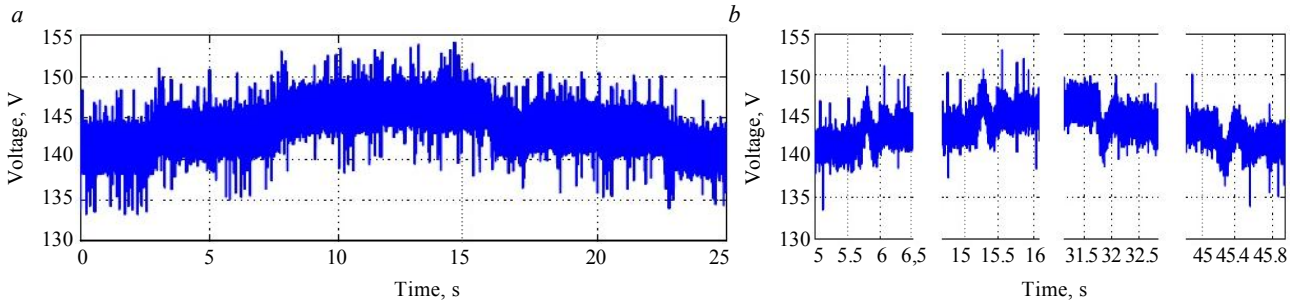

Fig.5. Voltage in node 1

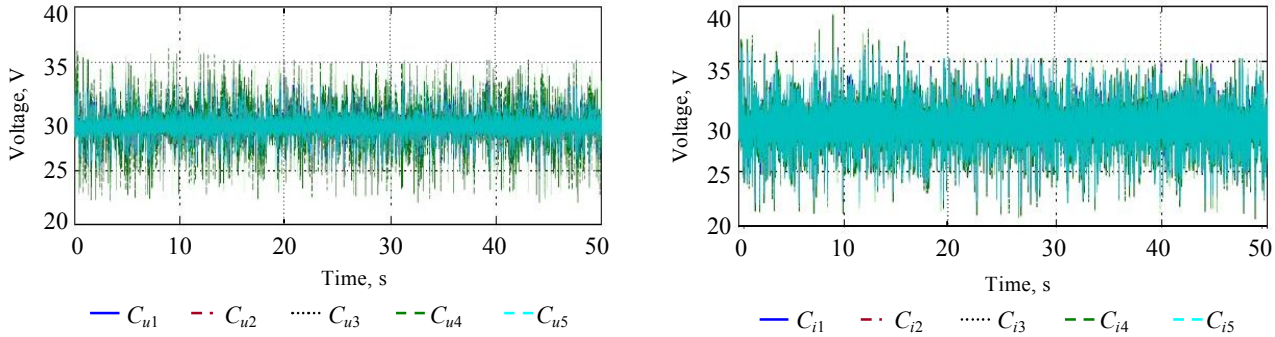

Fig.6. Voltage in MMC capacitors

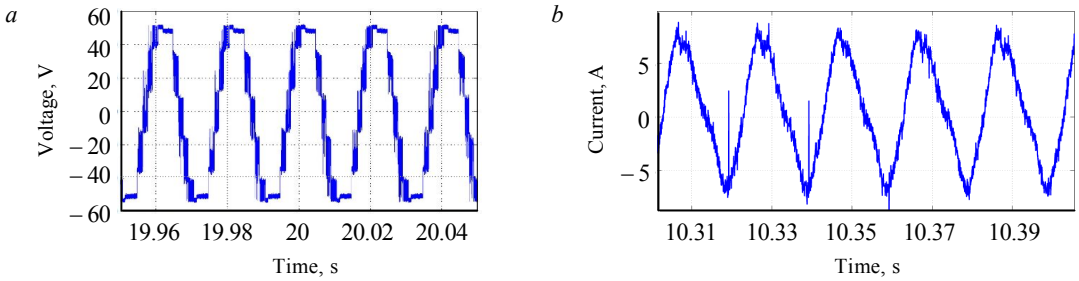

Fig.7. AC output voltage in phase A of MMC (node 3) (*a*), AC current phase A at node 3 (*b*)

In Figure 7, *b* the AC output current at MMC node is illustrated (phase A). Although it has an almost sinusoidal form, since the MMC operates with few sub-modules (it is a laboratory prototype) the harmonic's level is not negligible. This fact will be improved in real operations, where it is expected to work with hundreds of sub-modules.

Finally, and with respect to secondary controller, in Table 3 a comparison between the proposed method and the classic Newton-Raphson algorithm for solving the power flow is addressed. We can note that for each secondary sample time, the time calculation is approximately five times lower with the proposed algorithm, with the same relative error (ε = 0.001). With respect to the number of iterations, we can notice as these values are similar.

Table 3

Power flow methods comparison

Polling period, s	Fixed-point		Newton – Raphson	
	Relative error (ε = 0.001)		Relative error (ε = 0.001)	
	Number of iterations	Elapsed calculation time, s	Number of iterations	Elapsed calculation time, s
15	3	0.021	3	0.098
45	3	0.023	4	0.107

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Conclusion. This paper proposes a full control strategy for multi-terminal DC grids with the implementation of modular multi-level converters (MMC) for the AC/DC conversion. This philosophy includes different control levels: secondary, primary and local in a hierarchical way. The real experimentation in a 3 nodes DC grid (150 V rated voltage) verifies the robustness of the whole hierarchical controller in normal conditions and also under unbalance conditions.

In the secondary layer, a new method to solve the power flow is addressed. It provides several advantages, which have been checked by experimentation, as for example less computational efforts or convergence guarantee under some mild constraints.

For the primary level, the droop control is implemented to maintain the DC voltage of the whole grid. The practical test shows as the DC voltage is always in a stable zone, even when perturbations appear.

And finally, the local controllers depend on the converter's topology. For the voltage source converters (VSC), a variation of the PI controllers is discussed, meanwhile for the MMC a new model-based optimization method to control the output (AC) current loop and circulating current controller are studied. In both cases, each control objectives are achieved. For example, in the MMC case, the test has shown as the energy in the capacitors and the exchange power with the AC side track the references.

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