Design of the LHCb Silicon Tracker and the Common TELL1 Board

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on behalf of the LHCb Silicon Tracker Group

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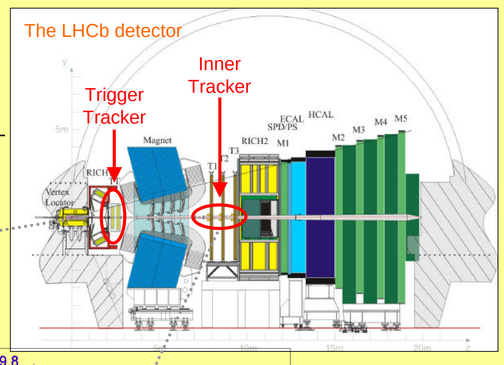
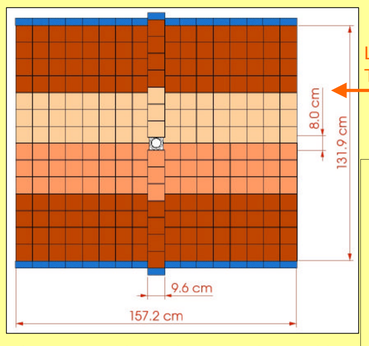
Layout of the Silicon Tracker

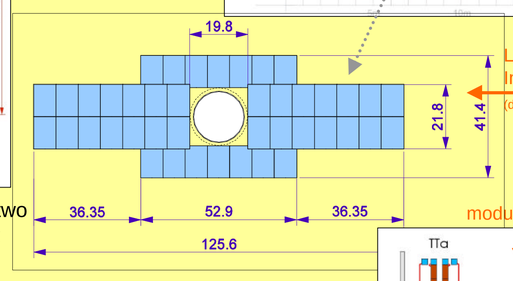
The Silicon Tracker consists of two subsystems: the **Trigger Tracker** (TT) in front and the **Inner Tracker** (IT) behind the magnet. The IT covers the region of high occupancy around the beam pipe, while the purpose of TT is to provide momentum information already at the 1st level trigger stage.





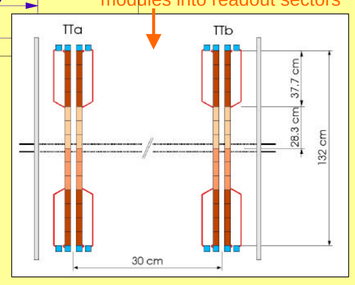
Layout of a Trigger Tracker Station

The TT consists of two stations with two layers of silicon strip sensors each; it covers the full acceptance of LHCb.



Layout of an Inner Tracker Station
(dimensions in cm)

Partitioning of the TT modules into readout sectors



For the TT, in order not to place the readout electronics within the acceptance, the signals of the inner readout sector are routed to their front-end chips via Kapton cables. The sectors comprise three or four sensors bonded in a row. The sum of cable and strip capacitances is ***~ 55pF*** for each readout sector.

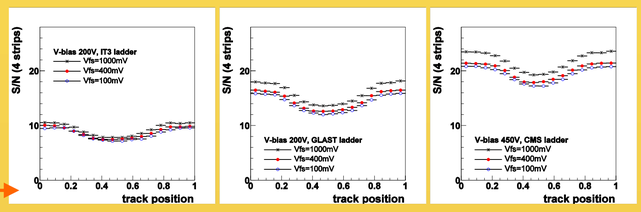
Sensor Design

In order to minimize the material budget within the acceptance, the **thickness** of the sensors should be ***as small as possible***. A larger pitch of the strips reduces the number of readout channels. The smaller the strip width, the smaller is the strip capacitance, resulting in a ***better noise performance***.
Prototype modules with Beetle front-end chips and sensors of thicknesses between 320 and 500µm (see Table) were tested in a 120GeV p^- beam at CERN. The performance of these modules was measured as a function of the bias voltage and for three different shaping times (see below).

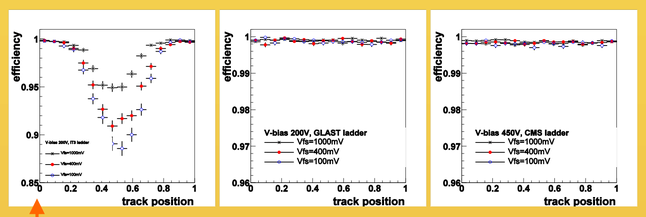
[LHCb Reoptimized Detector Design and Performance, CERN-LHCC 2003-30]

Module	Length [cm]	Thickness [µm]	Pitch [µm]	C_{strip} [pF]
IT3	32.4	320	198	50.6
Glast	26.3	410	228	41.3
CMS	28.9	500	183	37.6

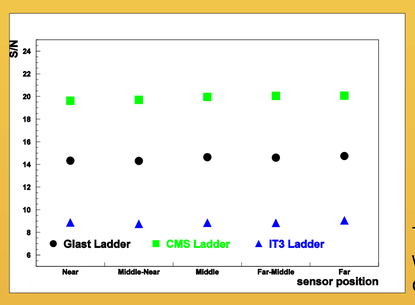
Properties of the tested prototype modules



Signal to noise (S/N) ratio as a function of the track impact position between two readout strips (0 = center of the left neighbouring strip, 1 = right strip). In the centre between the strips, a ***significant drop*** of S/N is observed for all prototypes.



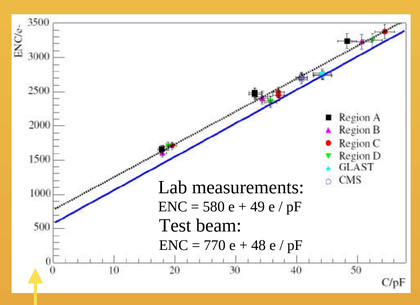
Hit finding efficiency as a function of the track impact position between two readout strips. For the Glast and CMS modules, S/N is high enough everywhere to obtain efficiencies very close to ***100%*** (above 99.8%) while for the IT3 module, a clear dip is observed, indicating that the S/N values in the middle of the sensors fall below a critical threshold. Therefore, the sensors used for the TT must be at least **410µm** thick.



The values of S/N were independent of whether they were measured on the first, second or third sensor or on a transition in-between two sensors of a module.

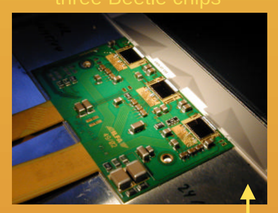
The Beetle Front-End Chip

is a custom development for the Silicon Tracker and other LHCb subdetectors. It is designed in radiation hard 0.25µm CMOS technology and has been tested for total ionizing doses of up to 40 Mrad. The chip comprises 128 channels with a fast front-end amplifier followed by an analog pipeline with a programmable latency of up to 160 sampling intervals and a differential output driver. Four analog output ports permit to read out the multiplexed analog data of the 128 channels within 900 ns.



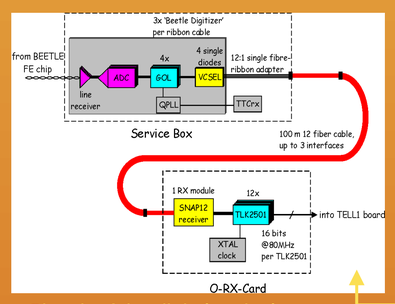
The Beetle front-end has been optimized for fast signal shaping and low noise for the large load capacitances provided by the long readout strips of the Silicon Tracker. The noise performance of the Beetle as a function of the load capacitance has been measured in a laboratory setup. The results of these tests have been confirmed in the test beam using Silicon Tracker prototype modules.

A front-end hybrid with three Beetle chips



The Digital Optical Read-Out Link

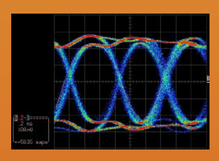
A front-end hybrid carrying three or four Beetle chips is attached to the end of each silicon module. The analog output data of the Beetle chips are transmitted over ~5m long low-mass copper cables to a service box that is located in an area of reduced radiation dose close to the detector.



Sketch of the digital optical readout link

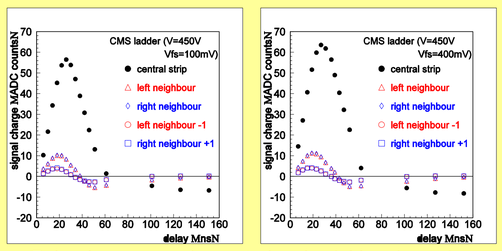
In the service box, data are digitized, multiplexed and converted to optical signals. The optical data are transmitted to the LHCb counting room via ~100 m long 12-fibre parallel ribbon cables.
In the counting room, two ribbon cables are connected to an optical receiver card that carries commercial optical receivers and de-multiplexers and provides the interface to the TELL1 readout board.

A full prototype link has been tested successfully in a laboratory setup. From an analysis of the measured eye-pattern at the receiving end of the optical link, an upper limit for the bit error rate of < 10^{-12} has been estimated.

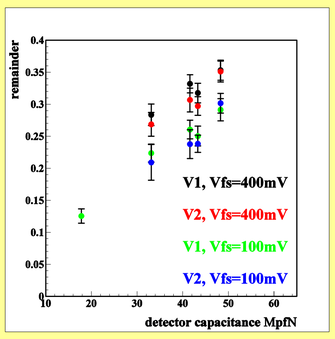


Shaping Time

The shaping time was adjusted by programming the Beetle front-end chip parameter V_{fs}. On the right hand side, plots are shown for two different shaping times (corresponding to V_{fs} = 100mV and 400mV). It is clearly visible, that the charge induced on the neighbouring strips arrives earlier than the signal on the main strip. This behaviour has also been found in simulations.



Pulseshape scans for central and neighbouring strips for two different shaping times.



Remainder of the signal as function of the readout strip capacitance.

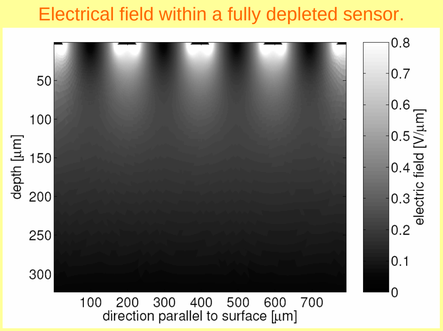
Remainder

For operation in LHCb, it is very important, how much of the signal is still seen in the next bunch crossing, i.e. 25ns later. For the IT, the remainder has to be at most 30%, for the TT less than 50% of the signal. The left plot shows that all prototype modules are ***compliant*** with these requirements for shaping times corresponding to V_{fs} = 400mV or less.

The S/N dip

It has been shown in a simulation [LHCb Note 2003-159] that the drop of the S/N values in-between two strips above bias voltages of 140V is not due to a ballistic deficit. Instead, charge carriers (mainly holes) are ***trapped*** in the low-field region between the strips at the surface of the silicon.

Electrical field within a fully depleted sensor.

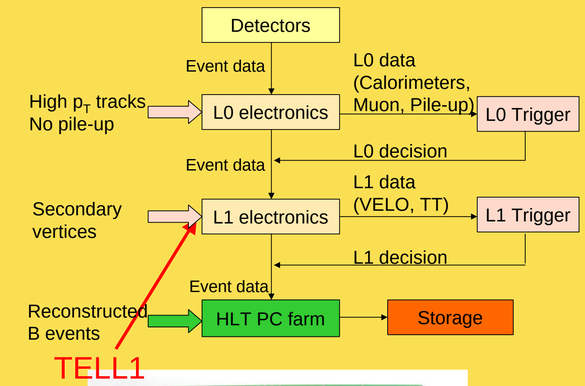


The LHCb trigger strategy is based on three levels:

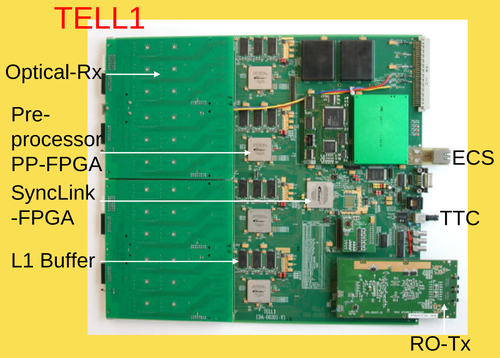
L0: fully synchronous and pipelined fixed latency of 4 µs (max L0 accept rate: 1.11 MHz);

L1: software trigger with maximal latency of 52.4 ms (max L1 accept rate: 40 KHz);

HLT (High Level Trigger): software trigger (HLT output rate: 200 Hz).

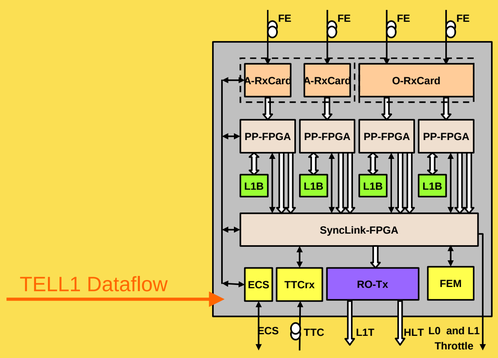


TELL1



The TELL1 readout board

The TELL1 is an FPGA based board made to readout the data accepted by the L0 trigger (see left column) and output them, after some processing, to L1 and HLT. To cope with two different link systems used, either 24 x 1.6 Gbit/s high speed optical links (ST, Outer Tracker, Muon, HCAL, ECAL) or 64 x analog copper links (VELO, VETO) are accepted as input. After synchronisation, event identification and error checking the dataflow is split. For the L1 data path, zero suppression is applied and processed data are sent to the L1 PC farm. For the HLT data path, raw data are stored in the L1 buffer and, if the event is accepted, zero suppressed and sent to HLT. The interface to the L1 and HLT event building network is provided by four Gigabit Ethernet links.



TELL1 Dataflow

L1 zero suppression and preprocessing

→ Pedestal subtraction, faulty channel masking, common mode suppression (see right column), hit detection, cluster encoding and encapsulation (PP-FPGAs).

L1 buffering

→ 58254 events stored in DDR SDRAM (96MB).

→ The DDRs are operated at 120MHz, to obtain a write bandwidth of 11.5 Gbit/s.

HLT zero suppression

→ Once a L1 accept is received, the corresponding event is read from the L1 buffer, zero suppressed, and linked to be sent to HLT (SyncLink-FPGA).

Timing and control interfaces

→ Timing and fast control are provided by an optical fiber transmission system (TTC).

→ Slow control interface common to the LHCb experiment (ECS) used for configuration, control and monitoring of the on-board chips.

Event building network

→ IP over Gigabit Ethernet.

→ Several events are packed into one MEP (Multi Event Packet), allowing moderate packet rates of 40 to 50 KHz.

→ The number of events per MEP can be adjusted for optimal packet size (1 Ethernet frame per MEP).

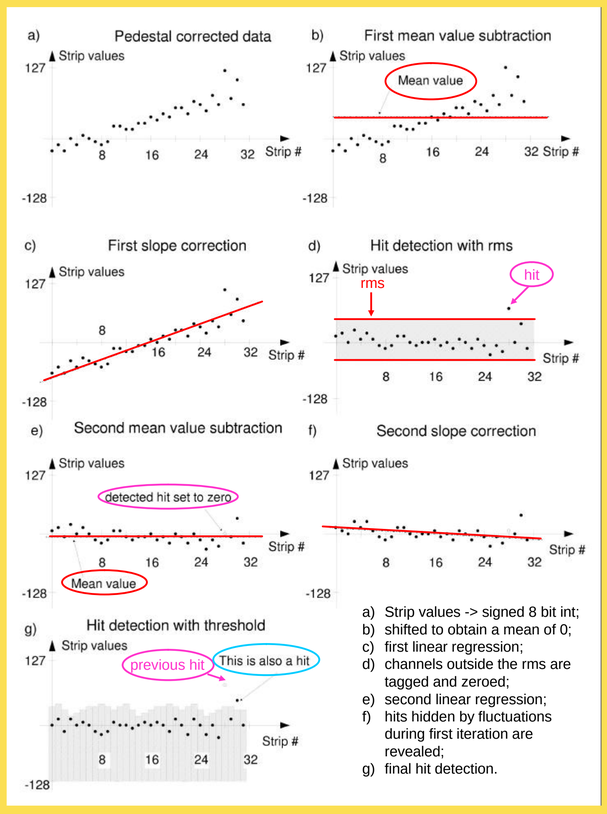
Conclusions

An FPGA readout board has been developed and will be used by the majority of LHCb detectors. Two boards have already been produced and are currently under test. Most of the needed firmware has already been written and tested with previous prototypes of TELL1.

Common Mode Suppression

For silicon detectors the algorithm implemented in the PP-FPGAs will perform a linear common mode correction:

Noise in channel *i* $Y_i = a + b \cdot i$



a) Strip values -> signed 8 bit int;
b) shifted to obtain a mean of 0;
c) first linear regression;
d) channels outside the rms are tagged and zeroed;
e) second linear regression;
f) hits hidden by fluctuations during first iteration are revealed;
g) final hit detection.