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A FAST DIGITAL INTEGRATOR FOR MAGNETIC FIELD MEASUREMENTS AT CERN

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A self-calibrating digital instrument for flux measurements on magnets for accelerators used in basic research on subnuclear particles is proposed. The instrument acquires voltage arising from rotating coils transducers with a theoretical resolution of 10 ppt and a maximum sampling frequency of 800 kS/s. Then, samples are integrated on-line and suitably processed in order to improve time resolution and flux accuracy. This allows the limits of state-of-the-art digital fluximeters, related mainly to newgeneration rotating coils, with trigger rate of 20 kHz and coils speed of 10 rps, to be overcome. The instrument has been prototyped at Magnetic Measurement and Testing (MTM) Group of European Laboratory for Nuclear Research (CERN), under a framework of cooperation with the University of Sannio. Details on hardware and firmware conception, as well as on experimental results of the instrument principle validation, and of the preliminary metrological characterization of the prototype, are provided.

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Abstract *– A self-calibrating digital instrument for flux measurements on magnets for accelerators used in basic research on subnuclear particles is proposed. The instrument acquires voltage arising from rotating coils transducers with a theoretical resolution of 10 ppt and a maximum sampling frequency of 800 kS/s. Then, samples are integrated on-line and suitably processed in order to improve time resolution and flux accuracy. This allows the limits of state-of-the-art digital fluximeters, related mainly to new-generation rotating coils, with trigger rate of 20 kHz and coils speed of 10 rps, to be overcome. The instrument has been prototyped at Magnetic Measurement and Testing (MTM) Group of European Laboratory for Nuclear Research (CERN), under a framework of cooperation with the University of Sannio. Details on hardware and firmware conception, as well as on experimental results of the instrument principle validation, and of the preliminary metrological characterization of the prototype, are provided.*

Keywords –Magnetic Materials/Magnetics, Particle Accelerator Science & Technology/Nuclear and Plasma Sciences, Signal Analysis/Signal Processing.

INTRODUCTION

Large Hadron Collider (LHC), the accelerator for subnuclear basic research in construction at CERN, is capable of providing a collision energy of 7 T eV to particle beam [1]. With this aim, magnetic fields over 8 T are necessary to manage the beam, and, thus, suitable superconducting magnets have to be realized. This pushed requirements for measuring magnetic quantities over current state-of-the-art limits [2].

In particular, LHC magnets are tested by measuring magnetic flux through digital instruments, integrating voltage output by transducers based on rotating coils. At CERN, Portable Digital Integrators (PDIs) [3], based on gain programmable voltage-to-frequency converters, were developed and have been used for 20 years successfully over the world [4]-[6]. The old generation of rotating coils (Fig. 1) allowed flux to be measured with integration times (i.e., time between two consecutive flux increment samples) of 10 ms. However, LHC magnet tests generated more constraining measurement requirements of 10 ppm on a flux fundamental of 5 Vs, with a typical integration time of 10 μs, and the need for analyzing harmonics up to 200 Hz. Such requirements are not satisfied by PDI (Fig. 1), and moreover, a new generation of more advanced rotating coils is going to be developed.

In other research laboratories, full digital solutions exploiting rotating coils have been proposed [7]-[9]. In Fig. 1, working areas of state-of-the-art solutions and PDI, delimited by lines related to input fullscale, offset, noise, and resolution limits, are compared. At Japan Atomic Energy Research Institute, suitable DSP algorithms manage a measuring chain based on three PDIs in order to select the best flux result [7]. At SACLAY (Fig. 1), a PXI acquisition board hosts numerical integration of voltage samples. A patent-protected concept guarantees time uncertainty to be reduced by a time-stamp resolution within 5 ns. However, the voltage is quantized by a 16-bit ADC [8]. At FERMILAB (Fig. 1), an ADC-DSP chain is exploited [9]. However, the method was validated at conceptual level on two VME boards, and resulted only 5 times faster than PDI. Moreover, offset and gain errors on the measuring chain requires repeated corrections and adjustment to a skilled operator.

At CERN, in the framework of a cooperation between Magnetic Tests and Measurements (MTM) Group and Engineering Department at University of Sannio, a self-calibrating digital integrator board, called Fast Digital Integrator (FDI), for measuring magnetic flux by new

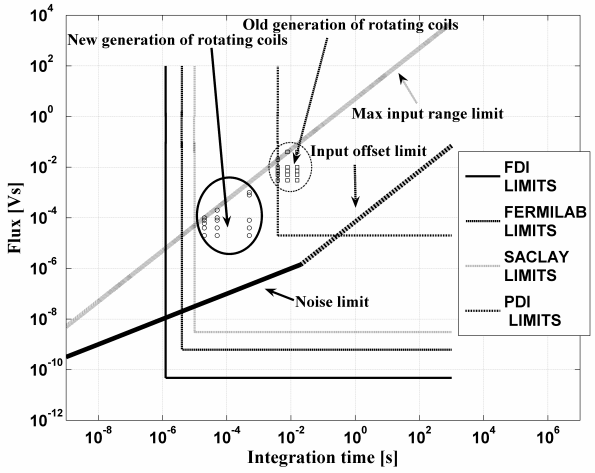

Fig. 1. Comparison among FDI and other state-of-the-art instruments.

generation of rotating coils is developed. A 18-bit 800 kS/s ADC and a 32-bit floating point DSP at 200 MHz allow an ideal adimensional quantization of 3,8 ppm and the use of suitable on-line flux interpolation algorithm, respectively. In the following, in Section II, the measuring principle and the architecture of the FDI are highlighted. In Section III, the experimental validation of the principle by a PXI measurement station is reported, as well as, implementation details of the realized prototype are given by showing results of preliminary metrological tests.

THE PROPOSAL

In the following, (i) the *key design concepts*, and (ii) the *architecture* of the FDI are shown.

A. The key design concepts

The FDI design is based on the following basic ideas:

a) *Immediate high-performance analog-to-digital (A/D) conversion*: the FDI leading concept is an immediate A/D conversion of the input voltage in order to measure flux by digital integration. Previously, the signal is only conditioned in order to optimize the conversion. State-of-the-art A/D converters (ADCs) allow on-line integration time of 1.25 μs and adimensional resolution of 10 ppt. This moves performance limits toward to analog signal conditioning, digital signal processing, and on-board noise;

b) *Differential measurement chain*: signal conditioning and A/D conversion are fully differential in order to increase the CMRR, strategic for satisfying noise requirements (Fig. 1) at lower integration times.

c) *Digital signal processing*: a digital signal processor (DSP) supervises the board and processes data; an FPGA acts as the I/O.

d) *Dichotomic algorithm of self-calibration*: the FDI calibration is carried out automatically by the following steps: (i) offset calibration with a short circuit at the input, by means of a 16 bit DAC; the step ends when the ADC output is the zero code, (ii) gain calibration: according to the selected gain, a suitable output of the voltage reference is chosen to reach the ADC full scale; the calibration is obtained through a digital Kelvin resistor*;* in this case, the step ends when the ADC output is the maximum positive code; (iii) offset calibration with the coil signal at the input by means of a 16 bit DAC; the step ends when the ADC output is the zero code. These steps are based on a fine calibration at 16 bit (digital potentiometer for the gain and DAC for the offset), thus, they are carried out through a suitable dichotomic algorithm in order to reduce times.

e) *Real-time correction of systematic errors*: the calibration values are stored in a EPROM; thanks to the calibration procedure, offset and gain errors are corrected in real-time automatically;

f) *Real-time algorithms of digital measurements* [10]: the DSP hosts easily updatable firmware for digital measurements, accuracy improvements, integration between asynchronous triggers, noise reduction, and so on.

B. The architecture

The architecture of the FDI is shown in Fig. 2. A differential block, including the voltage reference, a programmable gain amplifier (PGA) and the ADC, is highlighted. The voltage reference includes the digitally programmable Kelvin resistor. A DSP supervises the board while an FPGA supervises the PGA operations and provides the interface for the board bus. The FPGA and the DSP, interfaced by command and data registers, host real-time self-correction and processing algorithms [10], respectively.

III. EXPERIMENTAL RESULTS

In the following, (i) the *measurement method validation*, (ii) the *prototype design*, and (iii) the *preliminary test results* of the FDI are presented.

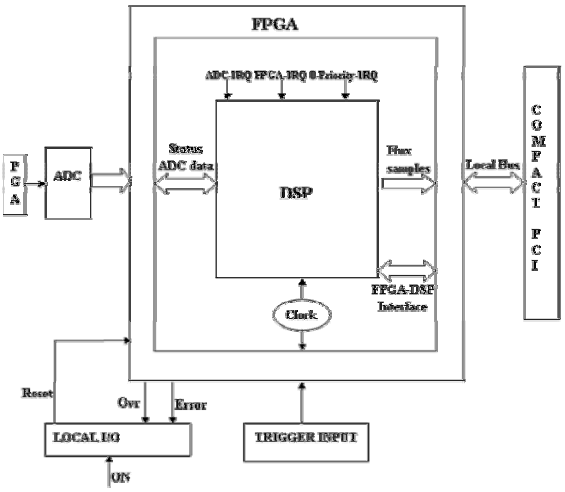

Fig. 2. Architecture of the FDI.

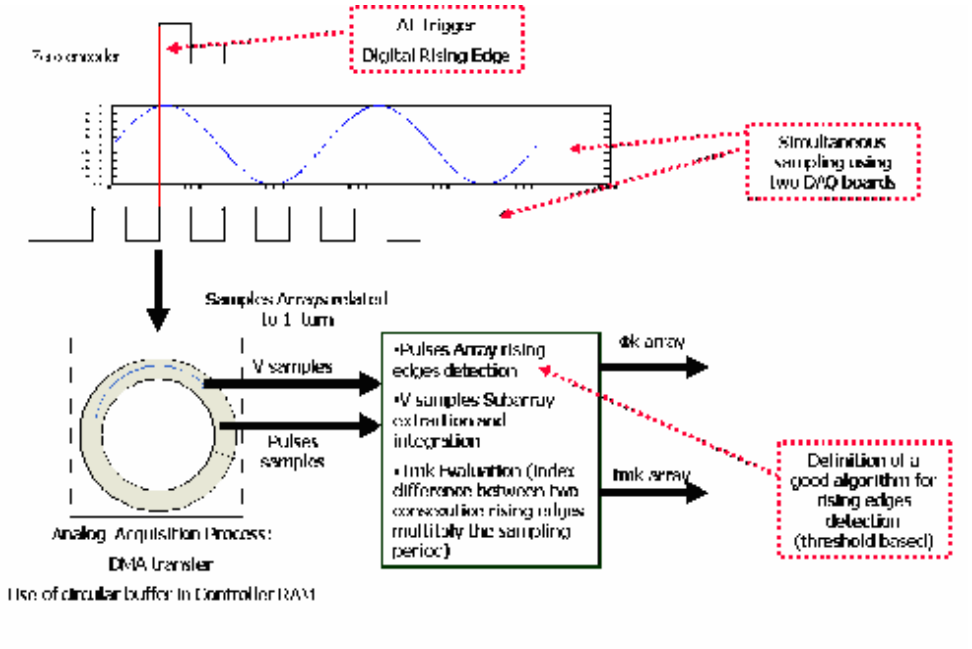

Fig. 3. Acquisition of rotating coil and encoder signals.

A. The measurement method validation

The FDI measurement method was validated experimentally at CERN laboratories by means of a suitable PXI platform [11]. In the following, the *measurement station*, and the c*omparison between FDI platform and PDI* are illustrated.

Measurement station

The FDI method was validated on a measurement station (FDI platform) based on:

A) 2 PXI boards NI 6289, with:
- 18 bit A/D converter;
- 625 kS/s maximum sampling frequency (500 kS/s in multiplexed mode on 16 differential channels);
- Analog input range programmable form $\pm$ 100 mV to $\pm$ 10 V;

B) Controller NI 8173, with:
- PIV 2.5 GHz 1GB RAM;
- OS RT PharLap;
- HD 40 GB or 512 MB flash memory.

Table 1. Test conditions.

Rotation Speed [rad/s]	6.469
Absolute Integrator Gain	1
Compensate Integrator Gain	1
Number of Points	512
Max Flux Variation [Vs]	$-3.5293*10^{-4}$
Max signal [V]	0.1859

This station was used to measure the flux of the magnetic field through a reference rotating coil: the pulses output by the encoder on the coil shaft, rotated by a motor, are exploited to integrate the coil voltage output in the angle domain. The coil signal and the pulses of the encoder are simultaneously acquired by the 2 NI 6289 PXI boards, synchronized by the PXI-bus trigger signal. The rising edge of the zero encoder triggers the acquisition of the analog voltage of the coil and the output pulses of the encoder (Fig. 3). The samples acquired and converted are integrated in block of N points, determined by the rising edge of the encoder pulses.

The uncertainty on the time $T_{mk,}$ the time interval time in between two triggers, is given by the resolution of the ADC sampling period, 1.6 µs, by knowing the number of ADC samples acquired. The value of an increment flux is released at each trigger. Then, the coil signal can be acquired and integrated over more turns.

Comparison between FDI platform and PDI

Magnetic field measurements were carried out on a LHC dipole magnet in the conditions of Tab. I (warm measurement conditions), in order to compare the performance of the above FDI platform with the PDI.

This test demonstrates the increased resolution achieved by the FDI with respect to the PDI. Fig. 4 shows that the numerical integration, with a 18-bit ADC at a sampling rate of 625 kS/s, can resolve increments of flux below the threshold of 10^{-5} Vs.

For the PDI system, the main source of uncertainty is represented by the voltage offset, at the output of the analog

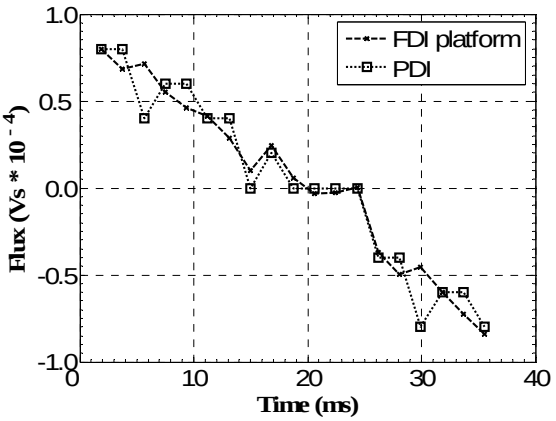

Fig. 4. Comparison between FDI platform and PDI.

front-end. This is higher than the main source of uncertainty in the FDI platform, represented by the trigger detection.

B. The prototype design

In the following, the *analog front-end design* and the *firmware design* of the PDI prototype are shown.

The analog front-end design

The FDI is based on an on-line numerical integration, carried out by the DSP Analog Device Sharc 21262, by providing a high resolution. However, main source of uncertainty arises from the analog front-end. Thus, main design challenges are imposed by the abovementioned accuracy requirements of $\pm$ 10 ppm, for 1 s of measurement time, for different full scale range (V): 0.1, 0.25, 0.5, 1, 2.5, 5, 10, 25, 50, and 100.

The design of the analog front-end includes the ADC Analog Device AD7674, the FPGA Xlink Spartan III, the voltage reference generator for the gain calibration, and the DAC for the offset calibration.

The input configuration, from the PGA to the ADC, is differential and realised with a Differential Input Differential Output (DIDO) structure to improve the stability of the measurements over a long time period by assuring a high CMRR. Only one very high-accuracy reference resistor is used for the gain calibration. The digital Kelvin divider assures a good stability to prevent drift and its value is automatically programmed by a digital bit-line. A real-time compensation of the voltage offset is implemented too. A periodic procedure of self-calibration of the board is foreseen by giving as input a ground signal. These are the main hardware design concepts implemented in the 8-layer prototype board shown in Fig. 5.

The firmware design

Figure 6 shows the conceptual State Machine of the FDI. The first state is the *bootstrap*, in which all the FDI devices are initialized after the power on. If there are no errors, the

Fig. 5. FDI prototype board.

FDI goes in the *ready* state, and waits for a user command. In the *ready* state, according to the command received from the user, the FDI moves to a further corresponding state. The *Self-Calibration* and *Measurement* commands force the instrument to move in the *self_calibration* and *measurement_acquisition* states, respectively. In the *self_calibration* state, the instruments carries out the calibration of gain and offset autonomously. In the *measurement_acquisition* states, the measurement is carried out by acquiring ADC data, performing the configured digital processing, and saving the results on the PC by the PXI bus. All the other user commands (including also instrument configuration) are executed in the *send_receive_cmds* state.

The instrument state is updated into the *instrument_status* register when the state is changed, excepting for the *recovery* state (in order to have memory of the state where the error occurred). After executing the operations foreseen in each state, the instrument moves back to the *ready* state, if no error occurred. In case of errors, the instrument moves into the *recovery* state. By knowing the previous state machine, the FPGA status, and the DSP error code, the instrument recognizes the current occurred error and writes it in the *instrument_status* register. In this way, being informed about the error, the user can decide to reset the instrument or to force it in the *ready* state.

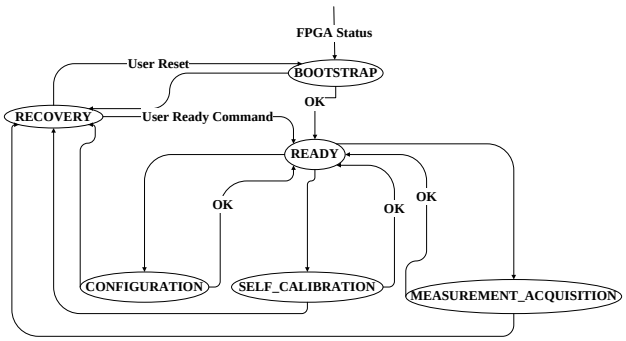

Fig. 6. Firmware architecture of FDI.

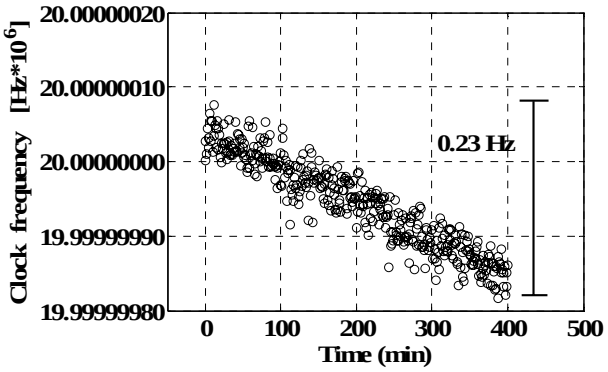

Fig. 7. Clock stability test.

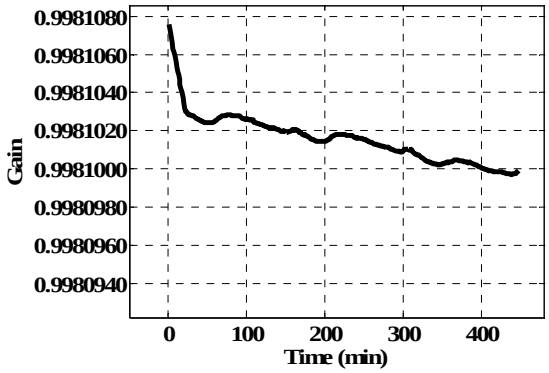

Fig. 8. Gain stability test.

C. Preliminary tests

A fully comprehensive metrological testing of the FDI prototype must be carried out in order to characterize the analog front-end of the board. At to date, preliminary stability tests of the clock and the gain were carried out at laboratory temperature.

In Fig. 7, results of the frequency survey of the prototype clock over about 7 hours are reported. With respect to a nominal value of 20.00000 MHz, a drift of about 0.23 Hz was measured.

In Fig. 8, results of the survey of the gain over about 8 hours are reported. With respect to a nominal value of 1.000000, a drift of about 8.0 ppm was measured also in this case.

These preliminary results show encouraging stability results without any temperature control. However, more rigorous tests under environmental controlled conditions have to be carried out in order to verify the actual stability of FDI performance.

IV. CONCLUSIONS

A digital integrator capable of satisfying measurement requirements imposed by LHC magnet testing at CERN has been developed under the framework of a cooperation between Magnetic Measurement and Testing Group of CERN and Department of Engineering of University of Sannio.

The FDI showed to be capable of achieving the requirements in experimental validation tests on an emulation platform based on PXI. Comparison with PDI proved satisfying outcome. A first 8-layer prototype board was also realized and preliminary stability tests showed gratifying results. A full metrological characterization is in progress in order to verify static and dynamic performance.

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