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METROLOGICAL CHARACTERIZATION OF AN IMPROVED DSP-BASED ON-LINE INTEGRATOR FOR MAGNETIC MEASUREMENTS AT CERN

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An improved on-line version of the self-calibrating digital instrument for flux measurements on superconductive magnets for particle accelerators, prototyped at the European Organization for Nuclear Research (CERN) in cooperation with the University of Sannio, is proposed. The instrument acquires voltage arising from rotating coils transducers. Then, the samples are online integrated and suitably processed in order to achieve flux analysis time down to 2.0 ìs, with resolution of 50 ns. Details about hardware and firmware conception, on-line measurement principle, and preliminary results of metrological characterization of the prototype are provided.

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Metrological Characterization of an Improved DSP-Based On-Line Integrator for Magnetic Measurements at CERN

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Abstract *– An improved on-line version of the self-calibrating digital instrument for flux measurements on superconductive magnets for particle accelerators, prototyped at the European Organization for Nuclear Research (CERN) in cooperation with the University of Sannio, is proposed. The instrument acquires voltage arising from rotating coils transducers. Then, the samples are on-line integrated and suitably processed in order to achieve flux analysis time down to 2.0 μs, with resolution of 50 ns. Details about hardware and firmware conception, on-line measurement principle, and preliminary results of metrological characterization of the prototype are provided.*

Keywords *– Accelerator measurement systems; Magnetic variables measurement; Digital measurements; Integrators.*

INTRODUCTION

At to date, at CERN and in other sub-nuclear research centers, magnetic measurements are demanding for more performing instruments in order to better characterize the dynamic features of superconducting magnets. One of most accurate techniques for analyzing the magnetic field is based on rotating coils [1]. The output signal of a coil rotating inside the magnet under test is integrated in the angular domain by means of pulses of an encoder mounted on the coil shaft, in order to obtain the magnetic flux. The flux sampling rate is determined by the frequency of the encoder trigger pulses.

A new generation of rotating coils is demanding for an increasing flux sampling rate and a higher accuracy [2]. Until now, the Portable Digital Integrator (PDI), based on a voltage-to-frequency-converter, has been used at CERN and in other sub-nuclear research centers [3]. However, its performance gets worse if the Over-Sampling Ratio (OSR) decreases, i.e. the flux sampling rate increases. Other digital solutions were proposed [4]-[5]. At SACLAY, the voltage signal is acquired by a digitizer board and the timebase is provided with a resolution within 5 ns for the final integration on the PC. This batch integration limits the bandwidth intrinsically [4]. At FERMILAB, though a Digital Signal Processor (DSP) acquisition board is exploited, the method resulted only 5 times faster than PDI [5]. Moreover, both these state-of-the-art solutions are validated only at conceptual level on separate boards, and the most critical impact of noise is not assessed at board level actually. At CERN, during the last year, a Fast Digital Integrator (FDI) has been proposed for a batch real-time on-board integration of the coil signal [6]. This instrument can analyze the magnetic flux over a bandwidth larger than state-of-art solutions and with a higher accuracy, owing to its 18 bit-resolution and 800 kS/s-rate digital conversion. Moreover, an absolute timebase measurement with a resolution of 50 ns, higher than the encoder accuracy, links angular and time domain.

A Programmable Gain Amplifier (PGA) and an Analog-to-Digital Converter (ADC) are the core of the FDI measurement machine (Fig. 1 [6]), capable also of correcting offset and gain automatically in real time. The DSP is the main board processor and the computational unit; it interacts with the measurement machine and the external PXI bus through a Field Programmable Gate Array (FPGA). However, preliminary metrological tests [7]-[8] showed some limits in real-time analysis, mainly related to batch integration.

In this paper, an improved version of the FDI, with a DSP-based on-line integration, allowing the flux to be measured over a bandwidth up-limited only by the Nyquist frequency of the ADC, is proposed. In the following Sections, (i) the on-line measurement principle, and (ii) the statistical metrological characterization of the new

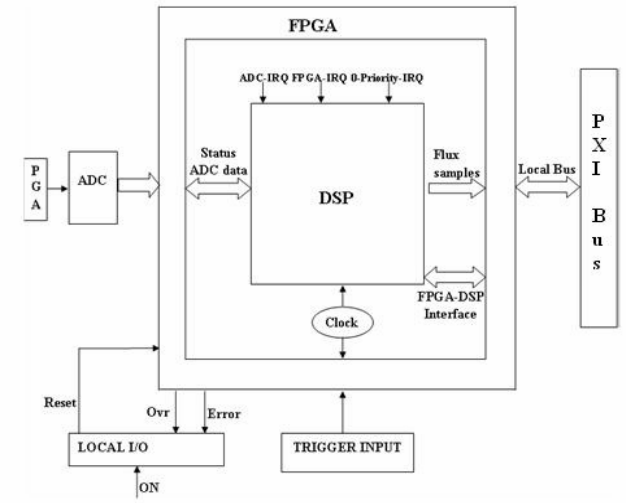

Fig. 1. FDI architecture [6].

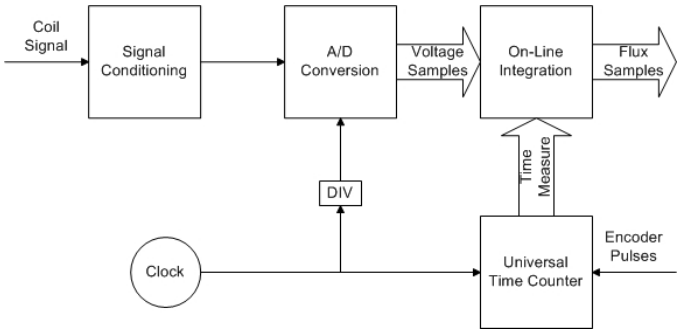

Fig. 2. FDI on-line measurement principle

instrument are shown.

ON-LINE MEASUREMENT PRINCIPLE

The FDI on-line measurement principle is shown in Fig. 2. The digitized signal in the time domain is integrated on-line in the angular domain, in order to assess the magnetic field, by means of the trigger pulses coming out form the encoder. The time instant of the trigger pulses are measured by a timebase within a resolution of 50 ns. Basically, the DSP releases a flux sample at each trigger pulse by integrating on-line the coil signal. Thus, the trigger frequency represents the flux sampling rate, whose theoretical maximum value is limited by the ADC Nyquist frequency.

The possibility of applying on-line algorithms and, in particular, on-line integration was achieved by a smart management of the DSP Interrupt Service Routines (ISR) and the reading operation from the parallel port.

The interrupt routines were implemented in Assembly code at machine level and the stack memory was saved customarily. In particular, the DSP interrupt routine for the measurement is critic because it is called at each ADC conversion. The DSP has therefore to read the data from the FPGA, save them into the memory, and return the control to the interrupted task before another interrupt occurs. Moreover, the interrupted task must have enough time to perform all the required computations, included the execution of the integration algorithm, before the following interrupt takes place. In other words, all the

Table I. Main components plugged on the board.

Area	Component	Type
A	ADC	AD 7634
B	Amplifier	AD 625
C	FPGA	Xilinx Spartan
D	PCI Interface	PLX 9030
E	Relays Calibration	#
F	Power Supplies	#
G	Resistors and Decoders	#
H	Voltage Reference	#
I	Clock Reference	#
J	DSP	AD Shark 21262

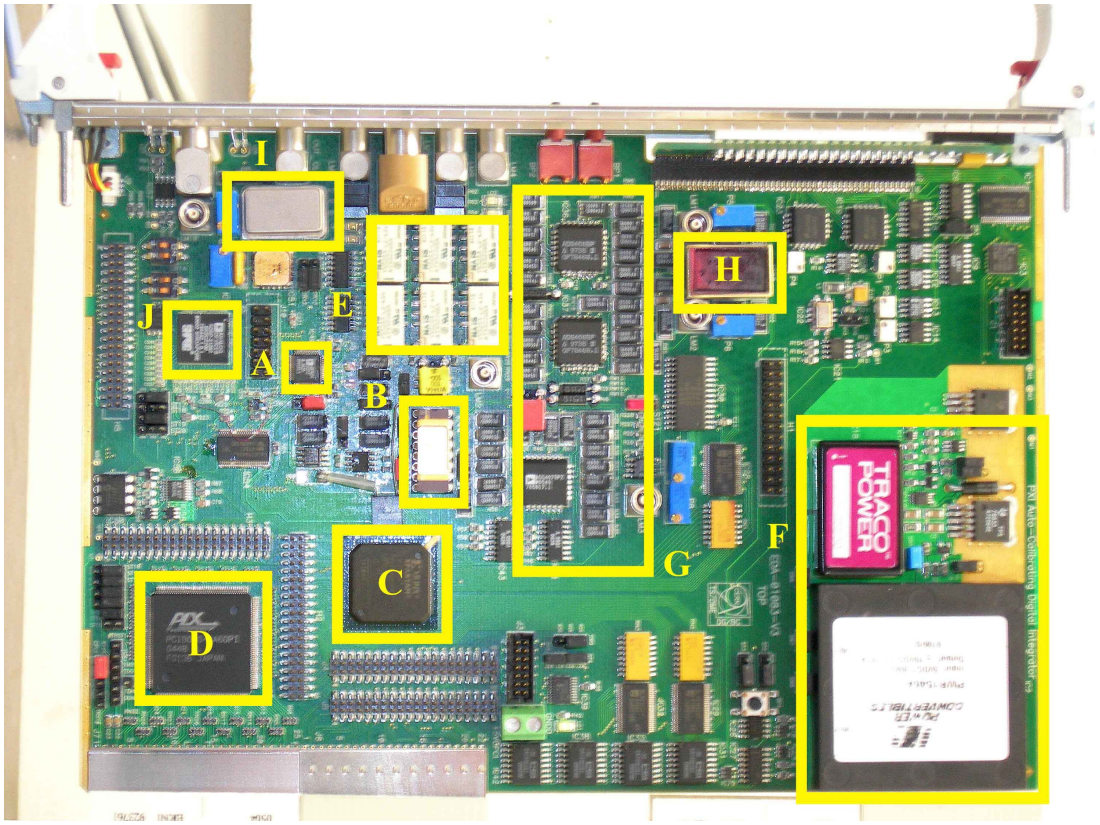

Fig. 3. FDI prototype board.

tasks must be performed within an ADC sample period. The code was at first developed using high level C/C++ code, but the resulting interrupt latency (the time from the interrupt occurrence to the beginning of the ISR execution) was so long that a new ADC conversion took place before the ISR was started. Better results were obtained by means of C code optimization. In this way the ISR execution started before a new ADC sample was read, but the time left within a sampling period was not enough in order to allow the completion of all the required computations.

Due to the strict above-mentioned time constraints, it was necessary to use Assembly code. By programming at low level, the decision not to save the stack was taken in order to decrease interrupt latency. It was necessary to use Assembly also for ISR programming, referring only the CPU registers and giving special attention to the reduction of execution time. A mixed approach, based on a Direct Memory Access (DMA) driven mode and on a core-driven mode, was used. This allows the reading of the data through the DSP parallel port for each measurement case to be sped up at the maximum. In fact, according to the content of the FPGA status register, read at each ADC conversion, the number of registers to be read and the operations to be carried out, are different. While reading is running in DMA-driven mode, under the control of the I/O processor, the DSP does not have to stall on the status register for the word to be read. It can therefore keep executing program instructions, as long as they do not last longer than the time required to read the word in DMA mode. Then the DSP can check the first word read by stalling on the status register (core-driven mode), in order to decide the right number of read cycles to be performed. In this way it is possible to save time by executing all the checks to update the pointers of the input data FIFO while the DMA mode is active. Moreover, the polling of the status register allows the right number of registers to be read, without overloading the parallel port. Owing to this ISR strategy, a significant improvement in time performance was achieved (Fig. 4).

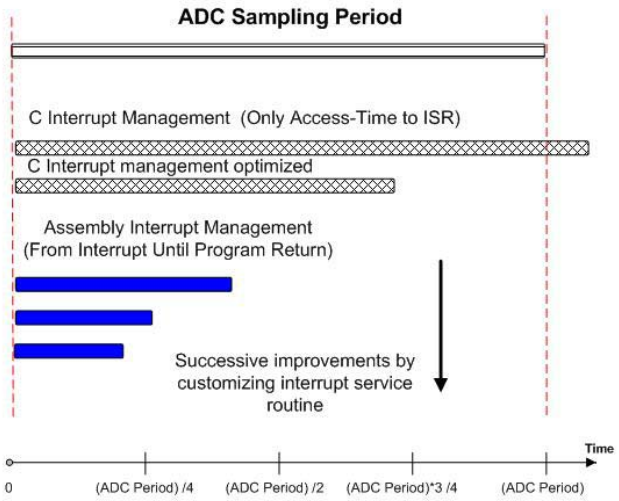

Fig. 4. ISR improvements

The voltage samples to be integrated come from the ADC in 32-bit integer representation. In principle, the integral is obtained as current sum of the contributions of the single samples, which in turn are computed by multiplying the samples by the sample period. Thus, a conversion from integer to floating point representation would be required. In the algorithm implementation, instead, in order to avoid loss of precision, the sum of integer samples is first computed. Subsequently, the multiplication by the sampling period is accomplished. The conversion to floating point is therefore performed as late as possible. Special attention has to be given to avoid overflow in the accumulator register, where the current sum of integer samples is hold. Before a new integer is added, a check is performed to detect whether the resulting value would lead to an overflow. In that case, the conversion to floating point is performed before the sum computation. In the end, it is worth pointing out that the output of the integration algorithm consists of the variations of flux between two consecutive trigger pulses. As a consequence, at each pulse all the registers are reset and a new computation is started, and therefore rounding errors are drastically reduced.

FDI ON-LINE PROTOTYPE

The main hardware components of the prototype board are shown in Fig. 3 and described in Table I. Among them, a special mention should be done for the analog circuit to drive correctly the new ADC AD 7634. The 18-bit differential bipolar ADC belongs to a new generation of SAR high-speed converter. In order to let it work properly, its input must be differential and bipolar, the common mode voltage must be limited, and the two input legs (positive and negative) must be in anti-phase to full exploit the input dynamic range. To accomplish such conditions, the output differential legs of the instrumentation amplifier are conditioned by a couple of fast operational amplifiers, thus deleting the common mode voltage and assuring the anti-phase condition required by the ADC.

The instrumentation amplifier AD 625 allows various gains to be applied by using feedback resistors. The voltage references are used to apply a reference input during the procedure for gain and offset on-board calibration. The FPGA acts as I/O processor of the board and manages the interfaces and the communication among the different parts of the board (namely the ADC, the DSP and the PXI interface). The DSP is the main board processor and handles the measurement algorithm for the on-line integration. The PLX 9030 is the controller of the PXI bus, used for the remote control of the board.

METROLOGICAL CHARACTERIZATION

The performance of the on-line FDI was evaluated by static and dynamic tests, according to the standards ISO ENV 13005-1995 [9] and IEEE 1057-1994 [10], respectively. A measurement station, based on AC FLUKE 5720A calibrator, remotely controlled via GPIB bus, was set up. Software applications were developed in MATLAB™ and LabVIEW™.
In the following, the preliminary results of (i) the *static tests*, and (ii) the *dynamic tests* are described.

A. Static tests

The *static tests* were performed by using the calibrator in order to supply a DC voltage as input to the instrument. Various input values were chosen. The correspondent outputs were obtained by setting a unitary gain and integrating for 1 s. For each input value, several measurements were performed and the mean value computed. Subsequently, the gain and offset errors were corrected, and the resulting values were used to obtain the input-output characteristic of the device. From the comparison between measured and calibrators values, the static errors were computed. The results give an estimation of the non-linearity errors as well as of the uncertainty. Fig. 5 shows the obtained deterministic static errors, along with the correspondent uncertainty bandwidth at $\pm$ 2 σ.

B. Dynamic tests

The *dynamic tests* aim at determining the SIgnal-to-Noise And Distortion ratio (SINAD), the Total Harmonic Distortion (THD), and the Signal Non Harmonic Ratio (SNHR) of the instrument, through an analysis in the frequency domain. The calibrator was used in order to supply a sine wave input voltage with specified amplitude and frequency. The input signal was acquired by the instrument, passing through the phases of conditioning, A/D conversion and on-line integration, thus obtaining the flux samples. A unitary gain was set.
Subsequently, a four-term Blackman-Harris window was applied and the FFT of the windowed signal was finally computed.
Table II summarizes typical results of the preliminary dynamic tests. In these tests, a sine wave input signal with a frequency of 20 Hz and an amplitude of 6 V_{rms} was applied. The tests were performed for different trigger frequencies with a measurement time of 2 s. Results show a typical SINAD of about 85 dB.

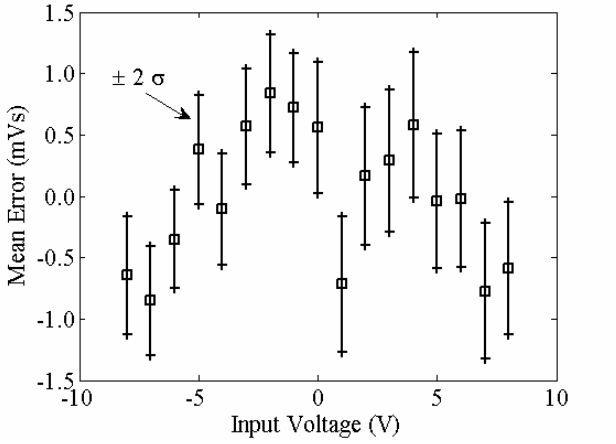

Fig. 5. FDI deterministic and random static errors.

CONCLUSIONS

The improved release of the FDI was prototyped and tested at CERN. With respect to the previous release, it includes and on-line integration, in order to achieve time analysis of the flux down to 2.0 µs. Preliminary results of static and dynamic characterization of the improved version of FDI working as on-line integrator showed satisfying static and dynamic metrological performance.

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Table II. Preliminary results of dynamic tests.

Input: 20 Hz, 6 Vrms; Measurement time: 2 s			
Trigger frequency (kHz)	SINAD (dB)	SNHR (dB)	THD (dB)
0.5	84.0	87.6	-85.7
1.0	84.8	91.3	-85.2
2.0	85.0	90.5	-85.8

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