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UNCERTAINTY REDUCTION VIA PARAMETER DESIGN OF A FAST DIGITAL INTEGRATOR FOR MAGNETIC FIELD MEASUREMENT

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Abstract

At European Centre of Nuclear Research (CERN), within the new Large Hadron Collider (LHC) project, measurements of magnetic flux with uncertainty of 10 ppm at a few of decades of Hz for several minutes are required. With this aim, a new Fast Digital Integrator (FDI) has been developed in cooperation with University of Sannio, Italy [1]. This paper deals with the final design tuning for achieving target uncertainty by means of experimental statistical parameter design.

Introduction

In high-accuracy instrument design, accuracy is enhanced usually by selecting higher-quality components and imposing narrower variations to influence parameters. A different approach is used in control system and electronic circuit design, or in quality engineering [2]-[5]: the system output is made as much insensitive as possible both to component tolerances and to influence parameters by selecting a suitable system configuration. This is carried out through analysis techniques of system theory, range methods, or statistical experiment design. In any case, the same aim of only finding better nominal values of system components or design parameters is pursued, by avoiding a cost increase.

In this paper, a procedure of uncertainty reduction, as well as of optimization of metrological characteristics, through statistical experimental parameter design in the input range as a whole is proposed and applied to the abovementioned FDI [1].

The proposed method

A measurement system can be formalized in terms of measurand parameters x_j (j = 1, 2,..., m), design parameters c_i (i = 1, 2,..., n), influence factors u_j (j = 1, 2,..., r), and reading parameters y_k (k = 1, 2,..., p) [6]. The c_i are sampled in order to assume q levels ($q = 1, 2, ..., z$). The problem of uncertainty reduction is defined as to find the combinations of c_{iq} that reduce the reading variance without loss in other metrological performance [6]. The burden of this task is reduced by *experimental fractional factorial* plans [2]-[6].

The first step of the proposed approach is to choose a suitable objective function η. Under the hypothesis of parameter independency, the relationship between η and c_i can be expressed by the following model:

$$\eta = \mu + \sum_{i=1}^{n} \delta_{iq} + \varepsilon \qquad (1)$$

where μ is the overall mean of η for the experimental plan, δ_{iq} is the deviation from μ due to c_{iq}, and ε stands for the uncertainty.

Experimental results are then analysed by [2]**:** (i) analysis of mean (ANOM)**,** in order to estimate the effects of the configuration options on the optimum attainment; and (ii) analysis of variance (ANOVA), in order to evaluate the relative weight of such options with reference to the uncertainty of the estimate, and to select only the most significant ones.

Experiments

The proposed method was applied to the FDI developed at CERN, under the framework of a cooperation between Magnetic Tests and Measurement (MTM) Group and the Dipartimento di Ingegneria of University of Sannio [1].

At CERN, Portable Digital Integrators (PDIs), based on gain programmable voltage-to-frequency converters, have been used for 20 years successfully [7]. However, in most advanced applications of test and control for the LHC under construction, more constraining requirements of 10 ppm on integrated voltage measurement for an integration time of 1 s or more are needed for the measurement of magnetic field based on rotating coils. Other laboratories proposed full digital solutions [8]-[10], however drawbacks related to timing constraints still arise.

The main sections of the FDI analog part are shown in Fig. 1:

- the Programmable Gain Amplifier (PGA);
- the 18-bit Analog-to-Digital Converter (ADC);
- the Field Programmable Gate Array (FPGA);
- the digital trimmer for the gain adjustment;
- the Digital-to-Analog Converter (DAC) for the offset compensation.

The input signal, picked up form the coil, is conditioned by the PGA and quantized and converted by the ADC; the digital signal is sent to a Digital Signal Processor (DSP) ADSP-21262 through the FPGA Xilinx Spartan III which represents the I/O processor of the FDI. The digital trimmer and the DAC operate in the calibration procedure for the adjustment of the selected gain and for the correction of the offset voltage.

The list of the selected design parameters with the respective levels is shown in Tab. 1: f_{FPGA} is the clock frequency of the FPGA, V_{ref} is the external reference voltage of the ADC, AVDD is the ADC analog power input, while V_{pow} is the power voltage fo the instrumentation amplifier of the PGA, and R_{gain} is a resistor that contributes to the final value of $R_{G,}$ the sensing resistor of the PGA (Fig. 1).

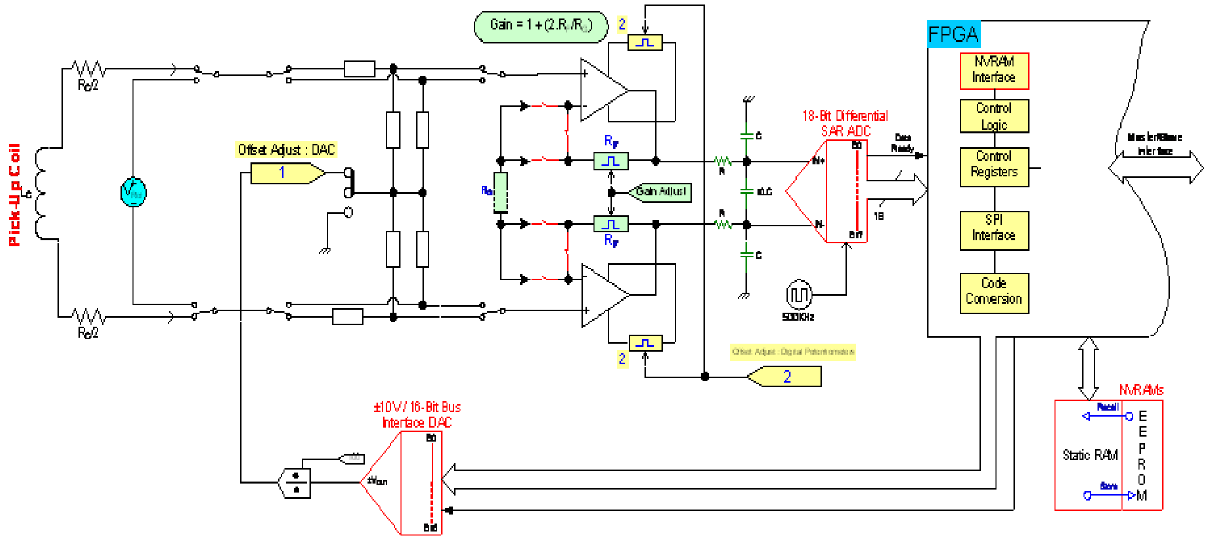

Figure 1. Prototype scheme.

There are five parameters with three levels thus the experimental plan L18 [2]-[6] (Tab. 2) was selected.

The chosen objective function was:

$$\eta_f = -10 \cdot \log\left(\sigma_f^2 + \left(\mu_f - 1\right)^2\right) \qquad (2)$$

each experiment (a row of the matrix) was replied n_r = 30 times. In the presentation, the optimal combination of parameter level, carried out with ANOM test, and the terms that have gone over Fisher test on ANOVA for a significance level of 99 %, and the achieved uncertainty reduction is reported.

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Table 1 – Control parameters with the respective levels

	Parameter	Lev. 1	Lev. 2	Lev. 3
x_1	f_{FPGA} [MHz]	20	35	50
x_2	ADC V_{ref} [V]	4.09	4.096	5.02
x_3	AVDD [V]	4.75	5.00	5.25
x_4	V_{pow}	14.0	14.5	15.0
x_5	R_{gain} [kΩ]	10	11.0	12

Table. 2 – Experimental Plan L18 (e: empty)

Exp.	x_1	x_2	x_3	x_4	x_5	e	e 7	e
1	1	1	1	1	1	1	1	1
2	1	1	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3
4	1	2	1	1	2	2	3	3
5	1	2	2	2	3	3	1	1
6	1	2	3	3	1	1	2	2
7	1	3	1	2	1	3	2	3
8	1	3	2	3	2	1	3	1
9	1	3	3	1	3	2	1	2
10	2	1	1	3	3	2	2	1
11	2	1	2	1	1	3	3	2
12	2	1	3	2	2	1	1	3
13	2	2	1	2	3	1	3	2
14	2	2	2	3	1	2	1	3
15	2	2	3	1	2	3	2	1
16	2	3	1	3	2	3	1	2
17	2	3	2	1	3	1	2	3
18	2	3	3	2	1	2	3	1