The ATLAS barrel level-1 Muon Trigger Sector-Logic/RX off-detector trigger and acquisition board

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Abstract

The ATLAS experiment uses a system of three concentric layers of Resistive Plate Chambers (RPC) detector for the Level-1 Muon Trigger in the air-core barrel toroid region. The trigger algorithm looks for hit coincidences within different detector layers inside the programmable geometrical road which defines the transverse momentum cut.
The on-detector electronics that provides the trigger and detector readout functionalities collects input signals coming from the RPC front-end. Trigger and readout data are then sent via optical fibres to the off-detector electronics. Six or seven optical fibres from one of the 64 trigger sectors go to one Sector-Logic/RX module, that later elaborates the collected trigger and readout data, and sends data respectively to the Read-Out Driver modules and to the Central Level-1 Trigger.
We present the functionality and the implementation of the VME Sector-Logic/RX module, and the configuration of the system for the first cosmic ray data collected using this module.

I. INTRODUCTION

The Sector-Logic/RX board is an important component of the ATLAS Level 1 Muon Trigger in the Barrel Region that is used to implement the level-1 trigger algorithm for one trigger sector and for detected data acquisition.
The ATLAS experiment [1] Level-1 Muon Trigger uses a system of three concentric layers of Resistive Plate Chamber (RPC) detectors in the barrel region.
The full experiment is divided on the azimuthal plane in sixteen sectors, and longitudinally in two half-parts, side A for positive eta (pseudorapidity) values and side C for negative eta values, so that we can identify 32 geometrical sectors (Fig. 1).
Each geometrical sector is longitudinally segmented, from a trigger point of view, in two trigger sectors, corresponding to the High-Voltage and the Read-Out sides of the RPC chambers. The global trigger system is therefore structured in 64 trigger sectors.
A trigger tower is composed of three RPC doublets detectors (inner, middle-pivot and outer) belonging to the same trigger sector. Each trigger sector is composed of six or seven trigger towers.

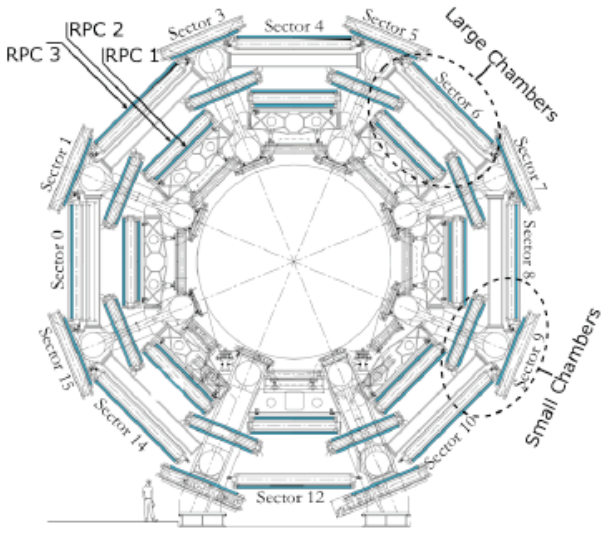

Figure 1: The ATLAS barrel region section on the azimuthal plane, showing the positions of the three concentric RPC detectors.

The trigger system [2] processes data of about 350.000 trigger chambers channels, reducing the raw rate of 40MHz bunch-crossing to 75 kHz within a maximum total latency of 2 µs including cable delays.
The trigger classifies muons within different programmable transverse momentum ranges, and tags the identified tracks with the corresponding bunch crossing number.
The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut.
The trigger is composed of the low-p_T and the high-p_T systems which apply different selection schemes.
Their algorithms ask for ¾ majority logic in the RPC1 and RPC2 layers in the low-p_T system, and ½ majority logic in the RPC3 doublet in the high-p_T (Fig. 2).
For each trigger tower the algorithm selects the muon trigger candidate, tagging it with the Bunch-Crossing ID (BCID), which is the number that identifies the p-p event inside LHC (the Bunch Crossing frequency is 40MHz). The algorithm then selects the Region Of Interest (ROI) which is the projective region that locates the muon track in the detector.
For each trigger sector the algorithm selects the two muon candidates with highest p_T corresponding to the same BCID, and identifies both of them by their ROIs.
The elaborated data of the sector trigger logic is sent to the Central Trigger Processor (CTP) which takes the final decision.

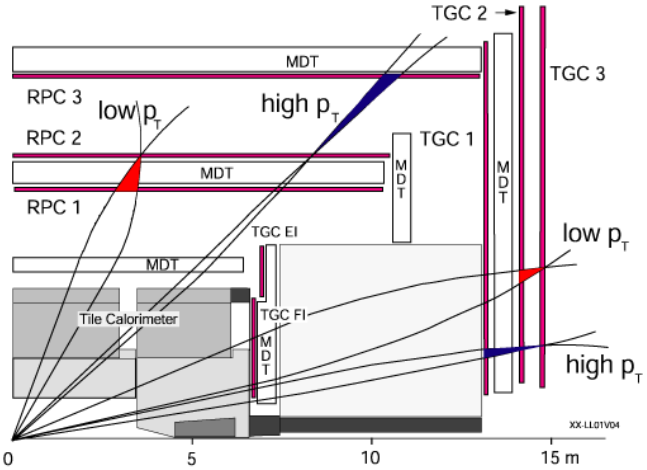

Figure 2: The low-p_T and high-p_T trigger scheme, showing the middle-pivot detector (RPC2), the inner low-p_T confirm detector (RPC1) and the outer high-p_T confirm detector (RPC3)

II. The Barrel Muon Trigger Electronics

A. *On-Detector Electronics*

The trigger tower on-detector electronics [3] is composed of two boards. The first called "Low-p_T PAD box" is mounted on the top of the middle-pivot RPC station, receives signals and looks for coincidences between the inner and the middle planes.
The other board, called "High-p_T PAD box", is mounted on the top of the outer station, receives the low-p_T trigger results and looks for coincidence with the outer RPC doublets.
Each PAD board hosts four Coincidence Matrix ASIC (CMA) Processors [4], which collect signals coming from the RPC front-end and provide the trigger and detector readout core functionalities (Fig. 3).

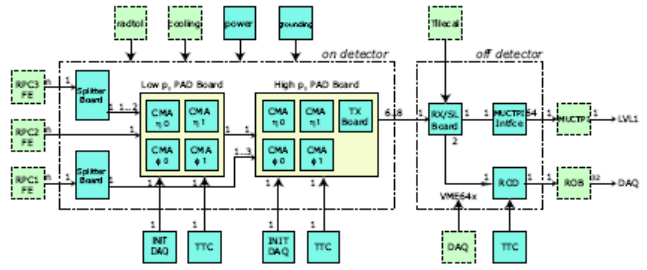

Figure 3: The on-detector barrel muon trigger electronic schema, showing the PAD boards that collect and elaborate data from the RPC front-end using the CMA processors and send output trigger and read-out data to the Sector-Logic/RX board.

B. *Off-Detector Electronics*

Trigger and detector read-out data from one trigger tower are sent via optical fibre to the Sector-Logic/RX board which collects data from one trigger sector.

The two main features of the Sector-Logic/RX board are:

- it reads trigger data from 6 or 7 towers belonging to the same sector, implements the sector trigger algorithm and sends the results to the Muon to Central Trigger Processor Interface (MUCTPI) module.
- it reads the detector read-out data from the towers, implements the event-building algorithm and sends the built read-out fragment to the Read Out Driver (ROD) module.

Sector-Logic/RX modules are VME boards located in the USA 15 room, far from the detector. Each of the 16 VME crates hosts 4 boards.
It has a direct communication with the ROD module, hosted on the same VME crate, through one 8-bit LVDS bus on a dedicated backplane. The MUCTPI modules placed on other VME crates, some meters away, communicate with the Sector-Logic/RX through a 32-bit LVDS bus using SCSI connectors.
The MUCTPI receives data from the trigger system of the Barrel, and of the End-Cap, resolving trigger in the overlap regions and sends data to the CTP (Central Trigger Processor). There are 8 MUCTPI boards dedicated to process data coming from the muon Barrel.

On the front panel of the Sector-Logic/RX there are 8 optical receivers so that there is no place for other connectors. For this reason we need an auxiliary board called "MUCTPI-Interface", which is located on the same VME crate, mounting on his front panel the MUCTPI SCSI connectors.
Since the ROD board receives detector read-out data from two adjacent trigger sectors, each ROD board needs 2 Sector-Logic/RX and 2 MUCTPI-Interface boards.
This "5 boards block" is called the "ROD Bus", and has this internal order:

MUCTPI-I / SL / ROD / SL / MUCTPI-I.

In each VME Crate there are 2 ROD-Bus (Fig. 4).

On each ROD-Bus, the communication among the internal boards is made using a Back-Panel Board (called ROD Panel), which is mounted on the backplane of the VME crate, that enables to share buses among adjacent slots.
The Sector-Logic/RX sends detector read-out data to the ROD and receives the TTC Timing Signals:

- CLK TTC: the LHC clock
- LV1A: signal that tells that a trigger event has been accepted
- BC-RST: the reset signal of the Bunch-Crossing counter
- EV-RST: the reset signal of the L1A counter.

Moreover it sends to the MUCTPI-Interface trigger data (Fig 5).

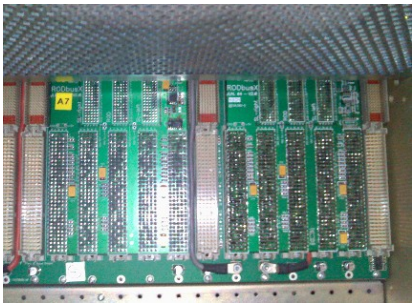

Figure 4 : Two ROD Panels, installed into a VME crate.

Figure 5 : The ROD Bus, showing the five boards mounted on the VME Crate in USA-15 room, one ROD, two Sector-Logic/RX and two MUCTPI-Interface boards.

III. The Sector-Logic/RX electrical schema

The Sector Logic Module logic core is based on two Xilinx FPGAs, one dedicated to the VME Communication interface (VME-FPGA) and others services (JTAG, I2C, etc..), and one dedicated to the trigger and read-out logic (SL-FPGA). The logical schema is presented in figure 6, while in figure 7 is shown a picture of the Sector-Logic/RX front view.

The main components of the board are:

- 4 Optical Receiver Card G2 Link RX, each with 2 Optical Link, that can receive 16 bit data at a frequency of 40 MHz
- 1 Xilinx FPGA Virtex-2 XC2V1000 575 used for VME communication.
- 1 Xilinx FPGA Virtex-2 XC2V2000 575 used for implementing all Sector Logic features.
- 3 PROM Xilinx XCV04F, for the storage of FPGA firmware (2 for SL FPGA, 1 for VME FPGA)
- 1 Serializer chip (DS90CR483) which converts 40 bit TTL input data, in 8 bit LVDS output data stream with a speed-rate of 240 Byte/s.
- 1 External FIFO IDT72V263 with a capacity of 8k 16-bit words.

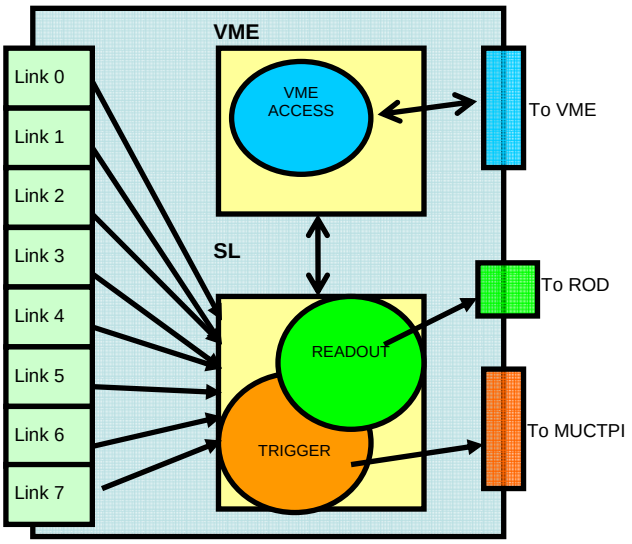

Figure 6 : The Sector-Logic/RX logical schema, showing input and output signals and the two FPGAs.

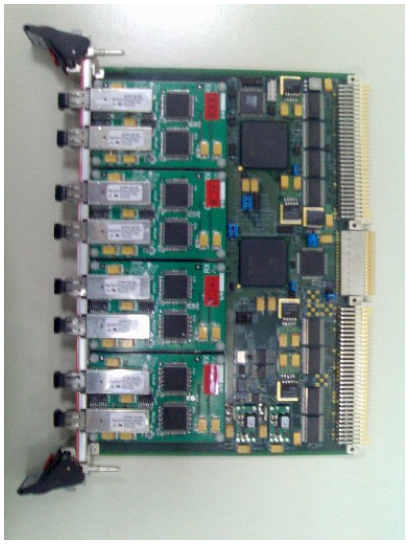

Figure 7: The Sector-Logic/RX board front view, showing the optical link receivers, the two Xilinx FPGA chips and the other components.

IV. The Sector-Logic/RX VME requirements

All the board logic is implemented using VHDL as the RTL synthesis language

The main feature of the VME FPGA logic is the implementation of the VME64x slave protocol.
Using a Single Board Computer (SBC) module as the Master VME, it is possible to read and write data from internal registers and FIFOs which are 32-bit long and are identified by a 7-bit internal address.
The working clock of the VME FPGA is the CLK LOCAL, generated by a 40 MHz quartz on the board.

The VME FPGA can access directly its 8 internal Registers and the external FIFO, and indirectly the 44 internal Registers and 12 FIFOs on the SL FPGA, via a 24-bit bidirectional communication bus; 16-bit for data, 7 for the internal address and 1 for the read/write command.
This FPGA works as the Master that begins a reading or a writing procedure on SL internal addresses.
When we want to write an SL internal address the VME FPGA begins the communication, it writes the data on the BUS, it waits for the acknowledge from the Sector Logic, and then it stops the communication.
When we want to read an SL internal address the VME FPGA starts a write Communication, then it releases the BUS, the SL writes the data, waits for the acknowledge from the VME FPGA, that finally stops the communication.
Since all the registers and FIFOs are 32-bit long, operations on them require two 16-bit transmissions.
The VME FPGA also controls the access on the external FIFO, the configuration signals of the 4 G2-LINK RX Cards and the Serializer chip, the implementation of the I2C protocol (not yet used) and the control of the JTAG signals.

V. The Sector-Logic/RX SL requirements

The SL PFGA logic can be divided into 4 main parts:

1. Trigger Logic
2. Read-Out Logic
3. VME access and services
4. Clock distribution

A. Trigger Logic

The trigger logic implements the trigger algorithm for one ATLAS trigger sector [4].
When a muon candidate is found by the on-detector electronics, the Sector Logic receives via optical fibre, a 16 bit PAD trigger word that contains the information about the trigger event (Fig. 8):

- **Threshold**: the value of the lowest programmable threshold passed from the low or high p_T RPC chambers.
- **ROI**: the Region Of Interest where the Muon was detected.
- **Overlap**: possible overlap in η or in φ between adjacent RPC detectors.
- **BCID**: the three low significant bit of the Bunch Crossing ID.
- **Busy-Xoff**: 1 bit that tells if the PAD internal FIFOs are almost full.

Bit	Mnemonic
15	Busy_Xoff
14	Reserved
13	Reserved
12	Reserved
11	BCID
10	BCID
9	BCID
8	Reserved
7	Overlap ETA
6	Overlap Phi
5	HitOPL
4	Threshold
3	Threshold
2	Threshold
1	ROI
0	ROI

Figure 8: The typical 16-bit Pad Trigger word format.

The trigger logic processes the (8x16)-bit data into a pipe line 3 bunch-cross (125 ns) long.
During the first clock the SL manages the η overlap within the sector: if 2 adjacent towers have detected the same muon, this is processed only one time.
In the second clock, the pipeline finds the first high-p_T Muon Candidate by using a 8x7 Matrix Comparator.
In the third clock the pipeline finds the second high-p_T Muon Candidate by using a 8x6 Matrix Comparator. The Sector-Logic/RX sends to the MUCTPI only two muon candidates and if there are more than 2, the SL flags it in the output packet on a dedicated bit (Fig. 9).
The total time needed by the trigger logic to process trigger data is 5 BC.

The output data are sent in a 32 bit word that contains information about:

- The overlap flag, the threshold and ROI values of the 2 Muon candidates
- The BC-ID
- The Flag of "More than 2 Candidates found"

The output trigger words are also stored into an internal FIFO, and are inserted into the read-out frame by the Event-Builder.
It is necessary to have the trigger data into the detector read-out information, in order to debug and monitor the events, and this is important also to perform the timing calibration of the different sectors.

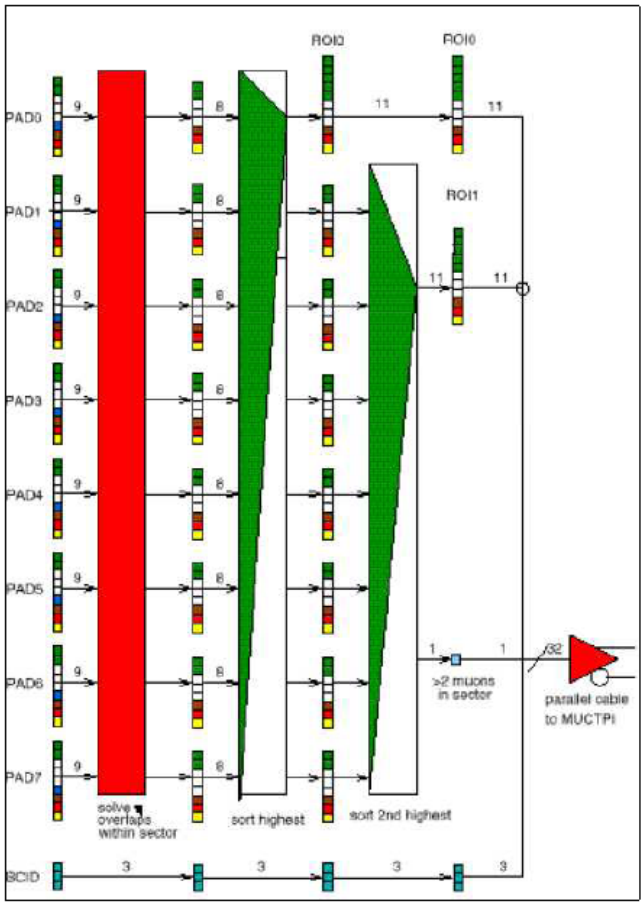

Figure 9: The Sector-Logic/RX Trigger pipeline schema, showing the three phases: overlap phase, first muon detection phase, second muon detection phase.

B. *Read-Out Logic*

The Read-Out Logic implements the Event Building algorithm and sends out data to the Serializer chip.

When a L1A Signal arrives from the TTC system, the Sector-Logic/RX receives a detector read-out packet from each tower.
Data arrive in the typical 16-bit PAD Frame Format (shown in figure 10) and are stored in internal FIFOs.
Every Frame is tagged with L1-ID (counter of L1 Accept event from the CTP) and BC-ID.

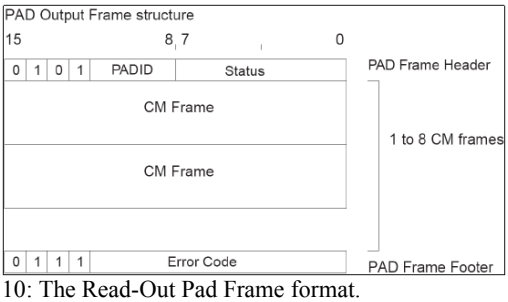

Figure 10: The Read-Out Pad Frame format.

As an L1A signal arrives from TTC, the event building logic reads one PAD frame from each FIFO, checks that the L1-ID and BC-ID are synchronized, reads the trigger event stored in the trigger FIFO described before, produces the 32-bit output frame in the typical SL/RX Frame format (shown in figure 11), and stores it in an output FIFO.

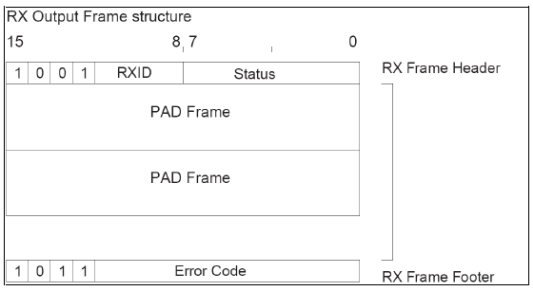

Figure 11: The Read-Out SL/RX Frame format.

Finally data are read from the external FIFO and sent to the Serializer, using 32-bit words at 40 MHz.
The Event Building Logic can operate with a 80 MHz clock, obtained by a DLL that doubles the 40 MHz operating clock.
Read-Out logic also provides the Busy logic, by checking the occupancy of the internal FIFOs and generating the Busy signals that prevents the trigger logic to send new L1A until the FIFOs are read.

C. *VME Access and services*

The VME Logic provides the reading and writing VME access from the VME FPGA, using the custom Master Slave protocol described before.
The VME Access is used for monitoring the board status, by reading the counters and the occupancy of the internal FIFOs.
Moreover it is also important during tests and debug phases. The Sector-Logic/RX is developed to be used as a general purpose board for testing PADs, other SL boards, RODs and MUCTPIs.
All input and output signals can be emulated by VME access. So it is possible to write the internal FIFOs emulating the PAD, or the TTC Timing signals emulating the TTC. It is possible to access directly the MUCTPI output data, and ROD output data. Moreover by mounting four G2Link TX (Transmitter) Cards instead of the RX (Receiver) cards, it is possible to send data to other SL boards, emulating the PAD board.
The problem is that the input data from PAD and TTC and output data to ROD and MUCTPI, uses the TTC Clock, while the VME access is made using Local Clock (a 40MHz clock obtained using a quartz mounted on board).
So the timing of the logic is not so simple.

D. *Internal Timing*

We have defined 4 Clock domain regions each with its own clock:

1. Input FIFO & Trigger Logic domain: we use this clock for the Trigger Logic and to write the Input FIFOs. This clock can be set as TTC or LOCAL.
2. Event Building domain: we use this clock for the Event-Building Logic, to read the Input FIFOs and to write the Output FIFO. This clock can be set as TTC, LOCAL or LOCAL x2.

3. Serializer domain: we use this clock to read the output FIFO and to send data to the serializer chip. This clock can be set as TTC or LOCAL.
4. VME Domain: we use this clock for the VME access. This clock can be set as LOCAL.

Since the 4 regions are separated from each other by asynchronous FIFOs, it is possible to set different internal clocks.

V. Conclusions

Four Sector-Logic/RX boards are currently installed in the USA-15 room.

During the last week, we used these 4 boards for the M4 integration cosmic run commissioning week.
Two RPC sectors (Sector 5A and 5C) were used in this RUN, so we took data from RPC detectors using 4 Sector-Logic/RX, and 2 ROD boards (Fig. 12).

Trigger Data were sent to one MUCTPI board together with Trigger Data from the End-Cap L1 Trigger System and finally to the Central Trigger Processor together with the Calorimeter Trigger Systems data.

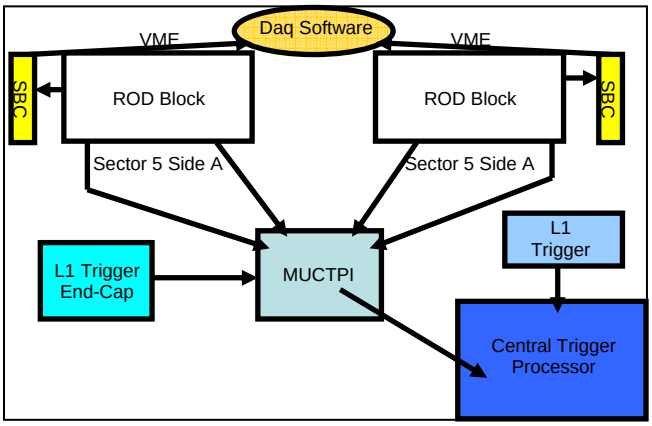

Figure 12: M4 Integration RUN Muon schema, showing the components used to take data from RPC Detectors.

We collected detector read-out data from RPC together with other ATLAS detectors (MDT, TGC, CSC), and Hadronic and Electromagnetic Calorimeters and TRT.
In particular RPC data were collected directly from the Sector-Logic/RX boards by the DAQ Software using VME access via a Single Board Computer on each VME Crate.

The results show that the Sector-Logic/RX boards are working correctly.
For the future, we have started the production of the missing 60 Sector-Logic/RX boards, and we will test and install them in the USA-15 Room.

VI. References

[1]http://atlas.web.cern.ch/Atlas/GROUPS/MUON/TDR/Web/TDR.html.

[2]http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html.

[3]http://sunset.roma1.infn.it/muonl1/

[4]F. Pastore, E. Petrolo, R. Vari, S. Veneziano, Performances of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger, Proceedings of the 11th Workshop on Electronics for LHC Experiments, Heidelberg, Germany, 12-16 Sept 2005.

[5] A. Salamon et al., "The Sector Logic demonstrator of the Level-1 Muon Barrel Trigger of the ATLAS Experiment", in Proc. VII Electronics LHC, Stoccolma, Sep 2001.