A Complete Set of Firmware for the TileCal Read-Out Driver

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Abstract

TileCal is the hadronic tile calorimeter of the ATLAS experiment at LHC/CERN. The Read-Out Driver (ROD) is the main component of the TileCal back-end electronics. The ROD is a VME 64x 9u board with multiple programmable devices which requires a complete set of firmware.

This paper describes the firmware and functionalities of all these programmable devices, especially the DSP Processing Units daughterboards where the data processing takes place.

I. THE TILECAL ROD MODULE

Both the electromagnetic and hadronic calorimeters in ATLAS use a common ROD motherboard (Figure 1) adapted to the specifications required in each case [1]. For this reason, the motherboards were produced together.
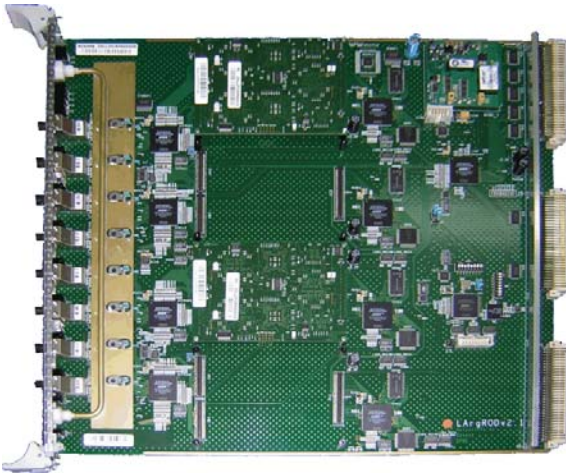

Figure 1: ROD motherboard with 2 Processing Units

Figure 2 shows a diagram of the ATLAS calorimeters common ROD including the main components within the board. These components and their function are described below.

1) Optical Receiver:

The data coming from the Front-End Boards (FEB) are received in the Optical Receivers (OR) located in the front panel of the ROD. There are 8 ORs mounted on each ROD and each one receives data from one super-drawer of the detector. The optical signal received is transformed by the OR into an electrical signal.

2) HDMP-1024 deserializers:

The differential signal coming from the ORs is then deserialized with 8 G-Links. The G-Link used in the ROD is the HDMP-1024 Agilent device. The G-links in the TileCal ROD are clocked at 40 MHz. It implies that each 25 ns a 16-bit word is received in the G-Links, providing a ROD input data bandwidth of 5,12 Gbps.

3) The Staging FPGA:

There are 4 Staging FPGA chips per ROD. The Staging FPGA distributes the input data to each Processing Unit (PU). It is possible to route up to four inputs to one PU. Thus, with only two PUs we can process all the data arriving to the ROD. This is the so-called Staging operation mode and it will be used in the TileCal experiment. Other functionalities of the Staging FPGA are the monitoring of the G-Links temperature and the injection of data to the PUs from an internal memory for debug and calibration tests.
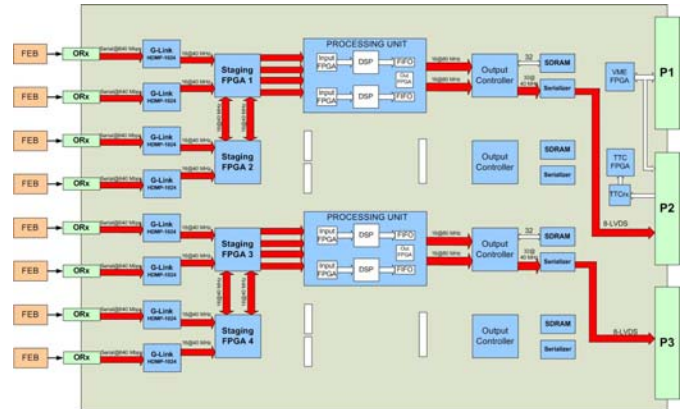

Figure 2: Block diagram of the TileCal ROD.

4) Processing Units:

The ROD has four slots for PUs but in the TileCal experiment will be used only two PUs per ROD. The ROD design with slots for PUs mezzanine boards allows flexibility for future upgrades. The DSP PU is equipped with two Input FPGAs and two DSPs [2]. These dual devices get double processing power in a single PU and in the Staging operation mode each Input FPGA and DSP has to process data coming from two inputs. In addition, an Output FPGA provides interface with the VME bus and with the TTC FPGA.

5) The Output Controller:

The Output Controller (OC) FPGA is the ROD output distributor. There are four OC mounted in the ROD but only two are used in the TileCal specifications. Each OC reads out the data coming from one PU and it builds a ROD fragment with the reconstructed data generated in four FEBs. It also adds S-Link header and trailers words to the output data according to the ATLAS TDAQ data format. Then, the OC sends this ROD event fragment to the next trigger level through the S-Link LSC cards located in the Transition Module (TM). Nevertheless it is possible to configure the OC to store the events in a SDRAM and to read out them from the VME bus.

6) The VME and BUSY FPGA:

There is one VME FPGA in each ROD. It provides communication between the ROD crate controller and all the components in the ROD. This communication allows configuration tasks, remote access to the JTAG chain and PUs booting. The Busy logic and Busy monitoring system is also implemented in the VME FPGA, as well as the interrupts handling.

7) The TTC FPGA:

The TTC information is received in ROD crates by the TBM and it is distributed to all the RODs in the crate through the backplane. This information is decoded at ROD level by the TTCrx and managed by the TTC FPGA which sends this information to the PUs. The TTC FPGA has different trigger operation modes and it is configurable with some VME registers. It is possible to trigger the ROD by the VME bus, locally or using the TTC information, which will be the normal trigger mode in the LHC.

II. TILECAL ROD MOTHERBOARD FIRMWARE SPECIFICATIONS

A. The Staging FPGA

There are four Staging FPGAs per ROD. The Staging FPGA is the ROD input data distributor. Each Staging FPGA receives data directly from two FEBs and it can receive the data of two more FEBs through a nearby Staging FPGA. Hence, the main function of the firmware implemented inside the Staging FPGA is to receive data from two G-Links or from another Staging FPGA and to send these data to the PU or to a nearby Staging FPGA.

In addition, due to its position the Staging FPGA has additional functionalities in the input stage of the ROD. It can be used to inject data events to the PUs for tests. Moreover, the Staging FPGAs are used to monitor and control the status of the G-Links. It allows to reset the G-Links, to check if the link is ready, to count the number of events received and to monitor the G-Links temperature measurements. The configuration and read-out of these functionalities is done trough the VME bus.
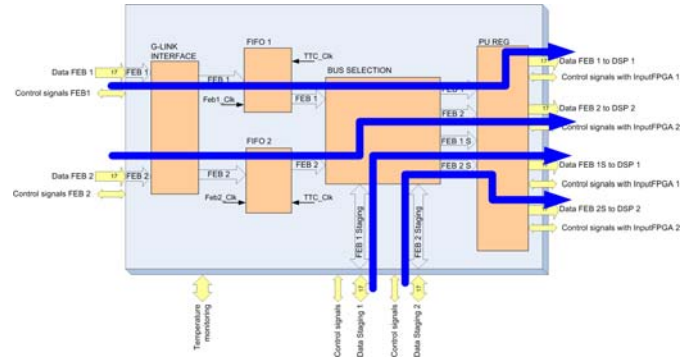

Figure 3: Staging FPGA with own PU dataflow

The four Staging FPGAs use the same firmware since the code is loaded from the same EPROM memory when the ROD is powered on. Nevertheless a hardware address allows to distinguish each Staging FPGA at firmware level. The hardware address is used to individually configure the Staging FPGAs. Although the firmware implemented is the same in the four Staging FPGAs, the functionality is not the same in all the cases. Since in TileCal only two out of four PUs are mounted, the functionality of each Staging FPGA depends on if the corresponding PU is mounted or not. In addition, the G-Links temperature monitoring system is performed in the third Staging FPGA for all the 8 G-Link chips.

The RODs already installed in their final placement in USA15 at CERN have the two PUs mounted in slots 1 and 3 (Figure 2). Hence, the Staging FPGA 1 and 3 should be configured to receive data from the G-Links and from the nearby Staging FPGA and to send these data to the PU (Figure 3) whereas the Staging FPGA 2 and 4 should transmit the received data to the nearby Staging FPGA. Since this configuration will be used during the experiment it is programmed in the firmware as default mode.

The main functionalities of the Staging FPGA are:

- To receive deserialized data from 2 G-Links and transmit them to the PU or to the nearby Staging FPGA.

- To provide a clock de-skew between the G-Link clock and the PU clock with a dual-clock FIFO implemented inside the device.

- G-Link chips reset and configuration.

- Interface with the VME bus for configuration and status read-out.

- Monitor the G_link chips temperature [3].

- Event injection to the PU for tests purposes.

B. The Output Controller

The OC FPGA is the data distributor in the output stage of the ROD. The main function of this FPGA is to receive the data from the PUs and to transmit them to the TM through the backplane. It formats the received events

according with the ATLAS official dataformat. Nevertheless, it is possible to configure the OC FPGA to receive data from another OC FPGA. This is the so called Staging mode. In addition, the data received in the OC FPGA can be read-out through the VME bus for tests purposes. Finally, the spy mode permits the read-out of some events through VME while the OC FPGA is sending out the data through the TM.
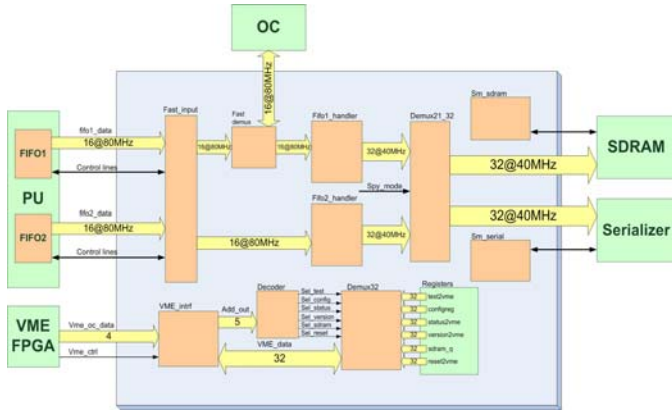

Figure 4: Output Controller FPGA block diagram.

Figure 4 shows the block diagram of the VHDL code implemented in the OC FPGA in order to achieve all these functionalities.

C. VME and Busy FPGA

The VME and Busy FPGA is the interface between the VME bus and the ROD motherboard. It provides communication with all the devices for configuration and monitoring tasks. Moreover, the VME and Busy FPGA has access to the JTAG chain for download firmware remotely. Furthermore, the VME and Busy FPGA is responsible for receiving and transmitting ROD interruptions and busy signals to the backplane.

The VME and Busy FPGA firmware provides:

- Communications through the VME bus with all the programmable devices in the ROD motherboard and in the PUs.

- Access to the JTAG chain for remote firmware downloading.

- Monitoring of the PUs available and the possibility of masking a mounted PU in order to remove it in the busy generation.

- Monitoring and transmission of the IRQs of the ROD motherboard.

- Gather the busy signals from the selected PUs and transmit the global busy signal to the TBM through the backplane.

D. TTC FPGA

The TTC FPGA is the responsible for the TTC information reception at ROD level. The TTC information is received in the TTC crate from either the CTP or the LTP. Hence, through an optical link it is transmitted to the TBM placed in the ROD crate. Finally, the TBM distributes this information to all the RODs through the backplane. Then, the TTCrx decodes the information in order to send the signals needed to synchronize the front-end data to the TTC FPGA.

Figure 5 shows the distribution of the TTC information at ROD level and the signals decoded by the TTCrx and transmitted to the TTC FPGA. These signals include the TTC 40.08MHz clock, the Level 1 accept (L1A), the reset for the event and bunch crossing counters, strobe signals for error detection and two addressed buses for trigger type commands transmission.

The TTC FPGA has three operation modes:

1) TTC mode:

This is the ATLAS operation mode. The TTC information is received though the TTCrx (Figure 5) [4]. The signals received permits the generation of the Event Identification (EVID) number, the Bunch Crossing (BCID) and the reception of the Trigger Type (TType) and addressed commands.
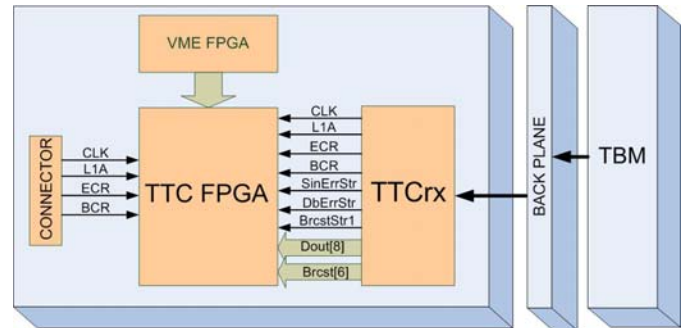

Figure 5: TTC signals distribution at ROD level in the so-called TTC operation mode.

2) VME mode:

This operation mode is used for tests and the EVID, BCID and TTYPE are directly written in the corresponding register through the VME bus. The complete TTC event is transmitted to the PUs with every EVID received.

3) LOCAL mode:

The LOCAL operation mode is also used for tests. In this case the TTC information is generated by using the signals received through a connector placed in the motherboard. This operation mode doesn't allow the reception of TTypes.

III. PROCESSING UNIT DAUGHTERBOARDS FIRMWARE

A. Introduction

The TileCal ROD is equipped with two PUs [2]. Each PU has to compute the data received from 4 FEBs and send it back to the ROD motherboard. The PU includes two Input FPGAs, two TMS320C6414@720MHz DSPs from Texas Instruments and two Output FIFOs. In addition, an Output FPGA provides VME and TTC interface with the motherboard (Figure 6).
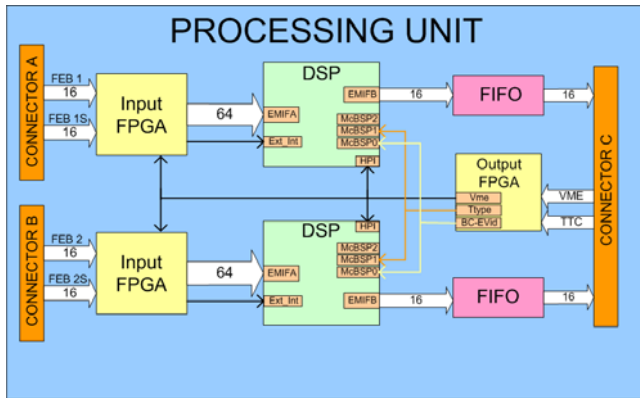

Figure 6: Processing Unit block diagram.

B. Input FPGA

The Input FPGA manages the data reception in the PU and checks the data before its transmission to the DSP. There are two Input FPGAs in each PU (Figure 6). Hence, each Input FPGA processes the data coming from two FEBs. The data are received from the Staging FPGA thought two 17-bit buses. These 17 bits include data and control signals. The data are transmitted to the DSP through a 64-bit External Direct Memory Address (EDMA) at 100 MHz (Figure 7).
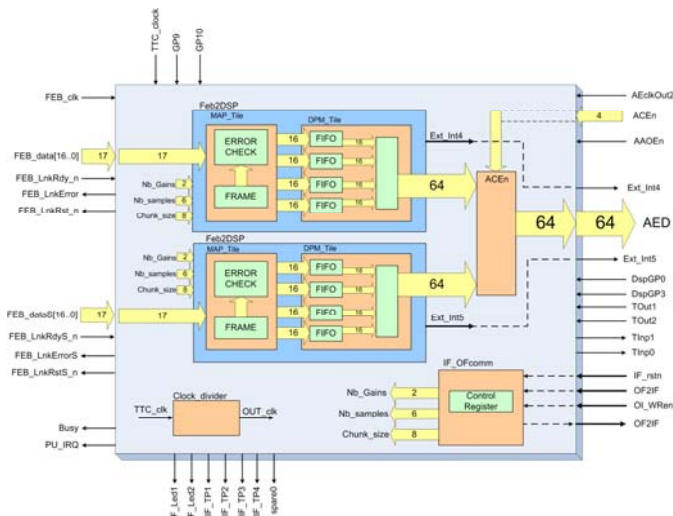

Figure 7: Input FPGA VHDL entities diagram.

The checking performed by the Input FPGA over each received event are:

- The received 32-bit DMU chip mask word is compacted in a 16-bit word.

- CRC checking of each DMU data block. The result is encoded in a 16-bit word in the DMU chip mask word.

- Global CRC checking. The CRC is computed over the whole event and transmitted in the global CRC word.

- The size of each event is checked taking into account the number of samples and gains of each event type.

C. Digital Signal Processors code

The Digital Signal Processor (DSP) is the main component in the TileCal ROD. The DSPs are responsible of data reconstruction in real time at the ATLAS first level trigger rate. The DSP has to compute the Energy, Time and Chi2 in less than 10 us at the ATLAS maximum rate and send the reconstructed data to the second trigger level. There are two DSPs in each PU, hence there are four DSPs per ROD. Each DSP process the data coming from two FEBs. Besides, the DSP synchronizes the front-end data with the TTC information received in the ROD through the TBM. Finally, some other algorithms, histogramming and commands are also processed by the DSP [5].
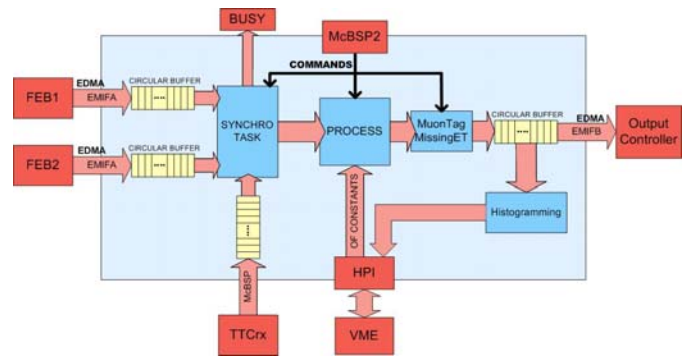

Figure 8: DSP code dataflow.

When the Input FPGA receives a complete event it sends an interruption to the corresponding DSP and the whole event is transferred to the DSP input buffer. There are two different interruptions in each Input FPGA in order to indicate which FEB the data corresponds to. The DSP stores the received events in two circular buffers, one per FEB (Figure 8). These input buffers store up to 16 events. When the buffer is full it stores the next event received in the first position. Once the event is reconstructed, it is copied to the DSP output circular buffer and transferred to a FIFO placed in the PU (Figure 6). The transfer between the DSP and the FIFO is handled by the EMIFB. In this case, the EMIFB has a 16-bit bus width, and it is clocked at 100 MHz.

The most important tasks performed in the DSPs are:

- Synchronization of front-end data with TTC information.

- Energy reconstruction applying the Optimal Filtering algorithm.

- Algorithms of Muon tagging and total transverse energy for Level 2 triggers.

- Internal Histogramming for reconstructed and raw data.

- Busy generation when the input buffer is almost full.

- To provide information regarding the drawers performance. This information is showed by the Trigger and DAQ software in the RITMO panel.

D. Output FPGA

There is one Output FPGA per PU and it is the interface with VME and TTC FPGAs. On one hand, as TTC interface the Output FPGA has to receive the TTC information received in the TTCrx and transmit this information to the DSPs through two serial ports (Figure 9). On the other hand, as VME interface it is used to download the firmware into the Input FPGAs and DSPs as well as to configure these devices.
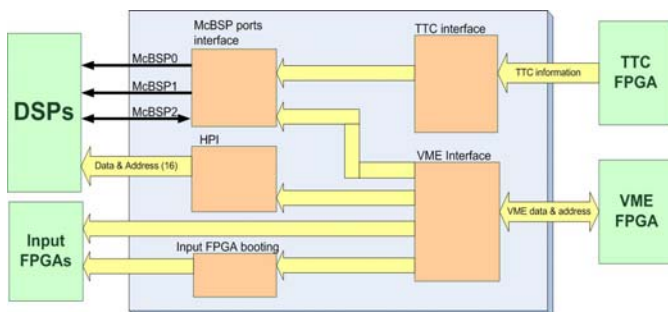

Figure 9: Output FPGA VHDL entities and dataflow.

The McBSP block is the interface with the DSP serial ports which are used to transmit the TTC information and commands In addition, the Host Port Interface (HPI) module is connected with the DSP HPI port which provides access to every internal memory address. The TTC and VME interface blocks implement the communication with the TTC and VME FPGAs. Finally, the Input FPGA booting module manage the code downloading in the Input FPGAs.

IV. REFERENCES

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