# Distribution of the Timing, Trigger and Control Signals in the Endcap Cathode Strip Chamber System at CMS

F.Geurts[a], M. Matveev[b], P. Padley[b]

[a]Fermi National Accelerator Laboratory, Batavia, IL 60510, USA
[b]Rice University, Houston, TX 77005, USA
matveev@physics.rice.edu

*Abstract*

This paper presents the implementation of the Timing, Trigger and Control (TTC) signal distribution tree in the Cathode Strip Chamber (CSC) sub-detector of the CMS Experiment at CERN. The key electronic component, the Clock and Control Board (CCB) is described in detail, as well as the transmission of TTC signals from the top of the system down to the front-end boards.

## I. Introduction

The Cathode Strip Chamber (CSC) sub-detector currently being commissioned at CERN comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of CMS. The goal of the CSC system is to provide muon identification, triggering and momentum measurement. The CSC electronic system consists of: (1) on-chamber anode and cathode front-end boards (AFEB and CFEB); (2) Trigger and DAQ boards in sixty 9U crates on the periphery of the return yoke of CMS; and (3) one Track Finder (TF) and four Front-End Driver (FED) 9U crates located in the underground counting room (Fig.1).

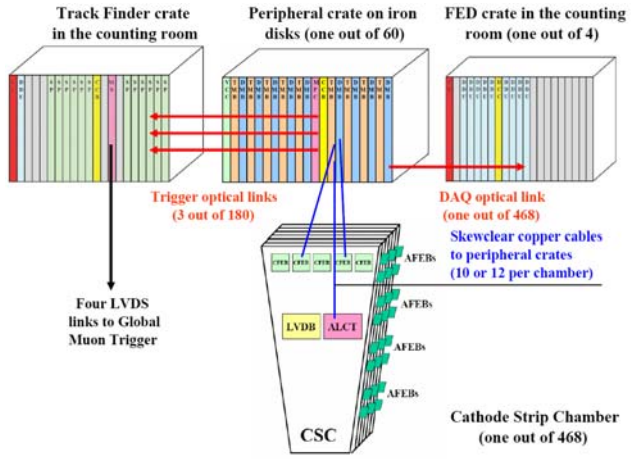


Figure 1: CSC Electronic System

In total, the timing, trigger and command information must be distributed to more than 3700 electronic boards in the entire CSC system.

## II. Layout of the CSC Timing, Trigger and Control System

The layout of the Timing, Trigger and Control (TTC) and Trigger Control components for the CSC detector is shown in Fig.2. The TTCmi (TTC machine interface) crate, TTCci (TTC CMS interface), TTCex (TTC encoder and transmitter), TTCoc (TTC optical coupler) and the TTCrx receiver ASIC are the CERN designed parts of the optical tree that allows the distribution of the LHC clock, synchronization commands and Level 1 Accept (L1A) decisions down to the sub-detector electronics. These parts are described in [1-2]. The TTCrx and QPLL ASICs reside on a TTCrq mezzanine [3] card on top of the Clock and Control Board [4] that has been designed at Rice University and will be described later in this paper. One CCB serves every peripheral and TF crate. In the Front-End Driver (FED) crates designed at Ohio State University (OSU) the Data Concentrator Card (DCC) [5] carries the TTCrx ASIC and acts as the source of clock and commands for the Detector Dependent Units (DDU) [6]. The Local Trigger Controller (LTC) [2] is a CMS specific module designed at CERN that allows operation of the sub-detector in a standalone mode using the local DAQ and local triggers. The Fast Monitoring Module (FMM) [7] is the main component of the synchronous Trigger Throttling System (sTTS) that provides the status of sub-detector partitions to the local and central Trigger Controllers.

The whole TTC/sTTS system at CMS is separated into 32 partitions that are hardwired in the TTC/sTTS tree. The CSC electronics occupies three partitions, including the Plus Endcap, Minus Endcap, and the TF, all controlled by a single LTC. Both Endcaps share a single TTCex. The TTCex is configured in dual mode and each partition uses one such a section. Each muon Endcap disk will have its own TTCoc. Each TTCoc is directly connected to its own socket on the TTCex. The FED crates will have direct fiber connections between the TTCex and the DCC. There will be a separate set of TTCex/TTCci modules for the TF crate.

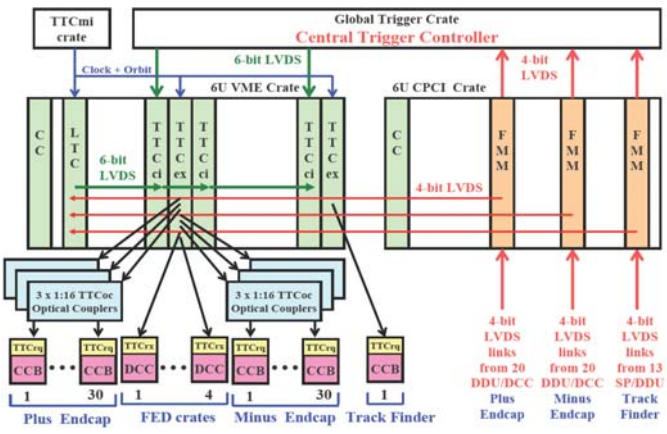


Figure 2: CSC TTC and Trigger Control System Layout

Every DDU and SP board provides its status information to the sTTS system via 4-bit LVDS links that are served by three FMM modules. In turn, the FMM boards supply the combined status of their partitions to the Local and Central Trigger Controllers (Fig.2).

The 6U TTC crate with the TTC boards (TTCci, TTCex, LTC) as well as the Trigger Control crate and the FMM crate are located in the underground counting room. A few spare optical fibers have been added in every CSC partition. In total, the TTC system of the CSC sub-detector provides precise timing, trigger and command distribution to 2736 on-chamber boards, 1056 peripheral boards, and 55 boards in the underground counting room.

## III. Clock and Control Board

The top component of the TTC distribution tree within the CSC system (with the exception of four FED crates) is the CCB. It resides in the middle of the peripheral and TF crates (see Fig.1) and carries the TTCrq mezzanine board with the TTCrx and QPLL ASICs. The TTC clock, Level 1 Trigger and synchronization commands are extracted from the TTCrx ASIC. In local mode the CCB may generate these signals from internal sources. A block diagram and a picture of the production version of the CCB are shown in Figures 3 and 4 respectively.

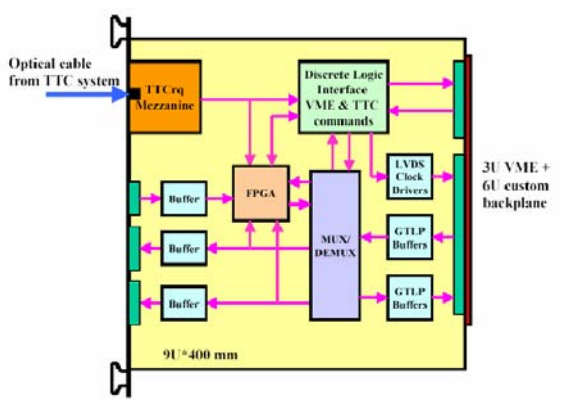


Figure 3: Clock and Control Board Block Diagram

The first prototype of the CCB [8] built in 2001 was implemented using a mezzanine Altera PLD. In order to reduce the cost, improve radiation tolerance and provide more flexibility we decided to use the Xilinx Virtex-2 XC2V250-4FG456 FPGA mounted directly on the main CCB board. Unlike the prototype, the most critical part of the CCB functionality on production board is implemented in discrete CMOS logic. These functions include the VME address and command decoding, generation of the Hard_Reset commands, clock and command distribution interfaces to custom backplane. While the peripheral and TF custom backplanes are different, the CCB pin layout is identical in both backplanes, so there is no need to build a unique CCB board for the Track Finder crate.

There are two modes of operation; the "Discrete logic", and the "FPGA" modes. In the "Discrete logic" mode the commands and L1A from the TTCrx ASIC are transmitted directly to the custom backplane. In the "FPGA" mode these signals are transmitted to the custom backplane either from the TTCrx through the FPGA, or are generated inside the FPGA upon specified VME write commands. There are several possible sources of L1A with programmable delay in the "FPGA" mode, including the Trigger and Data Acquisition Motherboards, VME, front panel etc. This feature is very convenient for various purposes of chamber testing, calibration and data acquisition and triggering in local mode, especially when the top level TTC components are not available or disconnected. Several critical internal and external (from custom backplane) signal outputs, including the L1A, are available on the front panel in the LVDS levels. This feature allows quick signal monitoring and debugging in a fully loaded crate, when needed. We have a CSC Local Trigger system set up using the L1A output of the TF CCB as an input to the LTC. The main mode of operation at the LHC is the "Discrete Logic" mode.

Figure 4: Clock and Control Board

Irradiation tests of the production version of CCB were conducted at the University of California (Davis) 63 MeV cyclotron in 2004. The discrete logic interface, FPGA and EPROM were irradiated up to 5 kRad while the CCB was distributing the clock, L1A and broadcast commands from the TTC source and the response was monitored from a target board in the VME crate. No errors were observed in the discrete logic unit or in the EPROM content that was continuously read back via JTAG bus. Three Single Event Upsets (SEU) were identified in the FPGA, at 2.1, 2.9 and 3.2 kRad doses. All were recovered after the Hard_Reset command. If the "FPGA" mode is used at the LHC operation, the SEU may be mitigated on a common or CCB-specific periodical "Hard_Reset" commands, as with all other on-chamber and peripheral electronic boards. Similar to all other VME boards in the system, the content of EPROM on the CCB board can be reprogrammed over VME within a few minutes.

## IV. Custom Peripheral Backplane Interface

Clock and command distribution from the CCB is implemented over custom backplanes. In the peripheral crates these are the 9U backplanes with the upper J1 connector compatible with the VME64x specification. In the TF crate the custom 6U backplane resides below the 3U VME64x compatible backplane. In the peripheral crate the CCB serves

nine Trigger Motherboards (TMB) [9] designed at UCLA, nine Data Acquisition Motherboards (DMB) [10] designed at OSU, and one Muon Port Cars (MPC) [11] designed at Rice University. In the TF backplane the CCB serves 12 Sector Processors (SP) [12] designed at University of Florida (UF, Gainesville) and PNPI (St. Petersburg, Russia), and one Muon Sorter [13] designed at Rice University. Both custom backplanes are designed at UF. In the FED crate the TTC source (DCC) typically supplies nine DDU boards. In this section we will discuss the peripheral backplane interface in detail; the clock and command distribution on the TF backplane interface is similar.

The B channel of the TTC system is intended for the transmission of individual and broadcast commands [1]. The 6-bit broadcast command is latched on the CCB board and along with the confirming strobe (equivalent to Clock40Des1 output of the TTCrx), is transmitted to the custom backplane bus. An 8-bit subset of the 14-bit individual command along with the confirming strobe (Data[7:0] and Data_Strobe outputs of the TTCrx respectively) are transmitted from the CCB to custom backplane as well. Both buses use the Gunning Transceiver-Logic Plus (GTLP) logic. The 100 Ohm bus terminations are located on both ends of the custom backplanes. The termination voltage is provided from the custom backplane and fixed at +1.5V.

There are five groups of signals in the custom backplane. Clock distribution and adjustments are discussed in more details in the Section V below. Fast Control Bus includes the 6-bit broadcast and 8-bit individual command busses with the corresponding 25 ns strobes, the L1A, the CCB status signals, and a few spare bussed lines. Out of 64 broadcast possible commands 32 commands have already been assigned in the CSC system. The decoding scheme is identical for both broadcast and individual command buses.

Among these commands, the “Hard_Resets” are intended for FPGA reloading from the respective EPROMs on CSC electronic boards to mitigate SEU due to radiation effects. These commands (including individual per each board type and one common for all boards) are decoded inside the CCB using discrete logic elements (which are immune to SEU to the expected dosage), expanded to 500 ns (as required for the Xilinx FPGA) and transmitted to peripheral backplane. Such an implementation allows all the receiving boards (TMB, ALCT, DMB, MPC) to connect the “Hard_Reset” signal directly to the PROG_B input of Xilinx FPGA.

Every board responds with the “Configuration_Done” signal as soon as successful reconfiguration is complete. These responses can be monitored over VME from the CCB as well as from each board in the crate. There are also the “Soft_Reset” signals assigned to allow FPGAs to be set into initial state without reloading. Altogether, these signals comprise the third group. The CCB itself, when in the “FPGA” mode, can also be reconfigured on a special “CCB_Hard_Reset” command.

A Special Purpose DAQ and Trigger Buses are intended for calibration, triggering, status and monitoring purposes. A full list of all signals can be found in the CCB specification [4].

## V. Clock Distribution and Adjustments

A low jitter 40.08MHz clock from the QPLL on TTCrq mezzanine card is distributed from the CCB to all slots over individual LVDS lines of the same length. A low jitter 80.16MHz clock from the QPLL is distributed to the Muon Port Card in the peripheral crate exclusively for the 1.6Gbps TLK2501 serializers that transmit selected trigger patterns to the CSC TF. There is also an on-board quartz oscillator that may produce 40.08MHz and 80.16MHz clocks instead of the TTC source. When the TTC clocks are used, the internal oscillator can be disabled.

The Trigger Motherboards (TMB) [8] in the peripheral crate serve one chamber each and provide all the required clock and commands for the Anode Local Charge Track (ALCT) board and trigger part of the cathode front-end boards (CFEB). The 40.08MHz clock is distributed to every board over separate LVDS lines. The commands as well as data are multiplexed at 80.16MHz (in order to reduce the number of lines) and transmitted over LVDS lines as well. Skewclear cables [14] are used to transmit the clock and commands to on-chamber electronics.

In such a large system as the CSC the fine and coarse delay adjustments at a various levels of the TTC distribution tree are of critical importance for timing the system in and for overall synchronization and data taking. One of the fundamental issues is that the trigger electronics must reliably identify the bunch crossing while the actual drift times span several bunch crossings (bunch crossing is one 40.08MHz clock tick). Another issue is that the CSC system comprises thousands of cables of various lengths. For optimal cable layout and placement, the length of optical fibers carrying the TTC and Trigger data, varies from 90 to 100 m. More than 5000 Skewclear cables from the chambers to peripheral crates vary in lengths from 6 to 15 m. So the variations in signal propagation from chamber to chamber up to the Track Finder within the CSC system may be as high as four bunch crossings.

The TTCrx ASIC allows coarse delay adjustments up to 15 bunch crossings for decoded commands and L1A as well as fine delays for the 40.08MHz clock with 100 ps accuracy. The CCB provides an isochronous 40.08MHz clock distribution on the custom backplanes without any further adjustments.

The TMB has several clock delays with the accuracy of 2 ns. The most important of them allow the following adjustments: (1) phase of the comparator clock on CFEB board to latch comparator data in the middle of the ~12 ns window; (2) phase of the output TMB-to-ALCT command for optimal latching TMB output data at the ALCT; (3) phase of the ALCT output data for optimal latching into the TMB. In addition, the ALCT has delay ASICs with the accuracy of 2.2 ns for optimal latching of raw data from the anode front-end boards into the FPGA.

The DMB provides 1 ns phase adjustment for the 40.08MHz clock to the DAQ logic on all CFEB boards.

## VI. Current Status and Plans

Three rounds of joint chamber and electronics tests were conducted at CERN in 2003 and 2004 with the structured 25 ns beam. Since the summer of 2005 a cosmic slice test was run on the surface of the detector assembly hall. The configuration evolved from three CSC chambers in one EMU station in the Plus Endcap to 36 chambers in three stations in October 2006, when the EMU system was participating in the Magnetic Test and Cosmic Challenge (MTCC) involving several CMS sub-detectors. The CSC electronics included the four fully loaded peripheral crates, one TF and one FED crate.

All the TTC (TTCmi crate, TTCci, TTCex modules) as well as Trigger Control (LTC) and sTTS (FMM) components were successfully integrated. The synchronization strategy was developed and implemented. As a result, all the 36 chambers were timed in and an error free data readout was reached. The CSC system operated in both Local and Global modes, including: (1) CSC own (TF-provided) and external triggers; (2) Local and Global DAQ readout; (3) LTC (local) and CTC (central) trigger control over TTCci. A low- and high-rate (up to 100 kHz) DAQ tests were conducted, with Data Quality Monitoring system in effect. The CSC electronics was tested with other sub-systems (RPC; Drift Tubes at a TF level; Global Muon Trigger).

As soon as the Plus Endcap disks were lowered down to detector cavern in late 2006 – early 2007, the CSC slice test activity shifted to Minus Endcap on the surface and now involves 18 chambers on two disks. Preparations for underground cosmic ray tests are well underway.

## VII. References


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