Final Test at the Surface of the ATLAS Endcap Muon Trigger Chamber Electronics

T. Kubota[a], M. Ishino[a], N. Kanaya[a], T. Kawamoto[a], T. Kobayashi[a], T. Kuwabara[a], H. Nomoto[a], H. Sakamoto[a], T. Yamaguchi[a], C. Fukunaga[b], M. Ikeno[c], H. Iwasaki[c], K. Nagano[c], M. Nozaki[c], O. Sasaki[c], S. Tanaka[c], Y. Yasu[c], Y. Hasegawa[d], H. Oshita[d],T. Takeshita[d], M. Nomachi[e],Y. Sugaya[e], T. Sugimoto[f], Y. Okumura[f], Y. Takahashi[f],M. Tomoto[f], T. Kadosaka[g], K. Kawagoe[g], H. Kiyamura[g], H. Kurashige[g] , T. Niwa[g], A.Ochi[g], C. Omachi[g], H. Takeda[g] , R. Lifshitz[h], N. Lupu[h], S. Bressler[h], S. Tarem[h], E. Kajomovitz[h], S. Ben Ami[h], O. Bahat Treidel[h], Y. Benhammou[i], E. Etzion[i], D. Lellouch[j], L. Levinson[j], G. Mikenberg[j], A. Roich[j]

[a] ICEPP, University of Tokyo, Tokyo, Japan
[b]Tokyo Metropolitan University, Hachioji, Japan
[c]KEK, High Energy Accelerator Research Organization, Tsukuba, Japan
[d]Shinshu University, Matsumoto, Japan
[e]Osaka University, Osaka, Japan
[f]Nagoya University, Nagoya, Japan
[g]Kobe University, Kobe, Japan [h]Technion Israel Institute of Technology, Haifa, Israel
[i]Tel Aviv University, Tel Aviv, Israel
[j]Weizmann Institute of Science, Rehovot, Israel

kubota@icepp.s.u-tokyo.ac.jp

Abstract

For the detector commissioning planned in 2007, sector assembly of the ATLAS muon-endcap trigger chambers and final test at the surface for the assembled electronics are being done in CERN and almost completed. For the test, we built up the Data Acquisition (DAQ) system using test pulse of two types and cosmic rays in order to check functionality of the various aspects of the electronics mounted on a sector. So far, 99% of all 320,000 channels have been tested and most of them were installed into the ATLAS cavern. In this presentation, we will describe the DAQ systems and mass-test procedure in detail, and report the result of electronics test with some actual experiences

I. Introduction

The sector assembly of the Thin Gap Chambers (TGC) is coming to end eventually at the end of August 2007 in CERN after about one and half years construction work. TGC is used to generate the level-1 muon endcap trigger signals in the ATLAS trigger system[1]. In order to supply the signals the TGC system covers the both endcaps of the detector with the wheel radius of 22m at about $\pm$ 15m from the interaction point. It covers the absolute value of pseudo-rapidity η from 1.05 to 2.4. Relative position of TGC in the detector can be found in Fig. 1 in which one-quarter view of ATLAS detector in the RZ plane is shown.

TGC is installed with three stations just behind the endcap toroidal magnet, which are called conventionally M1, M2 and M3 from inside to outside. A station of the high precision muon chamber (MDT) is installed between M1 and M2. The level-1 muon trigger signals in the barrel region are generated by RPC which has also three station structure, and there is an overlap region of RPC and TGC at the upper right corner. With three station structure (one triplet and two doublets) per endcap, TGC tries to measure and identify the isolated muons with two steps of the coincidence logics (conventionally called low-p_T and high-p_T coincidence in which p_T means transversal momentum). Three stations are installed separately in three wheels, and each wheel is segmented into 12 sections in which one section is called a sector or 1/12 sector. This 1/12 sector is a physical installation unit of the TGC system for both the chambers and electronics as well as a unit for the trigger and readout segmentation.

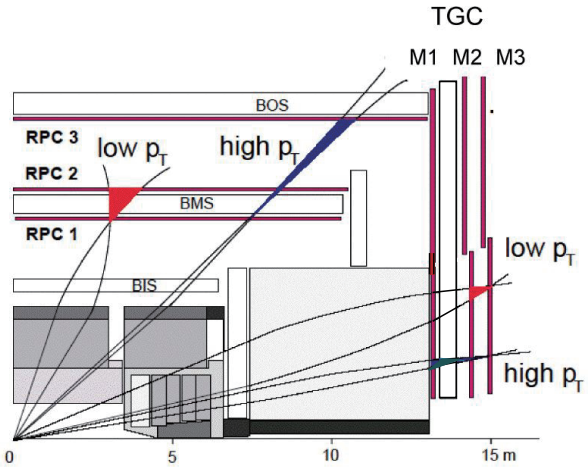

Figure 1: Muon chamber complex and Level1 muon trigger scheme in the 1/4 side view of ATLAS

The electronics system of the TGC detector is divided into

mainly two parts, the one is for the level-1 trigger generation and the other one is for the readout. In the trigger part, after precise delay adjustment and bunch crossing identification, the low p_T (using either triplet or doublet data) and high p_T muon (using both triplet and doublets) identifications are done firstly for the r- and ϕ- coordinates independently, and two data are combined and analyzed in the sector logic (SL). It produces a muon endcap level-1 trigger candidate signal eventually if both two coordinate data are matched in appropriate conditions.

The readout data are processed firstly in the ATLAS stand manner of the Level-1 pipeline buffer and derandomizer chain. Then the data are moved to our own data multiplexer and compressor system called the star switch (SSW) . Finally SSW sends the collected data to a ROD (Read Out Driver) module. The electronics modules and parts except SL and ROD, which are installed in the counting hut, are installed mostly in the immediate vicinity of the TGC either on the surface of a sector or at a VME crate installed at the outer rim of a sector. Most of the signal processing for the TGC hit data is, therefore, done at the detector side.

Although the electronics part on TGC has vital roles for the trigger and readout signal processing, repair of the system on-detector part is extremely difficult and the occasion is very limited once the sectors are installed in the ATLAS cavern. The system should be constructed rigid and it functionality should be checked cautiously from the various points of view when the sector is still stored in a surface building.

In this report we discuss mainly validity tests of the electronics system mounted on a sector using both embedded test pulse facilities and cosmic rays. We report the performance and some outcomes of the system test in the final section.

II. TGC Electronics

Fig. 2 summarizes a structure of the TGC electronics system. Electronics components are divided into two parts; on-detector and off-detector ones. The on-detector part is further separated into two parts, one is called Patch-panel and Slave board that is installed just behind the chamber (we call this unit as PS-board) and the other one is Hi-pT and Star Switch Control (HSC) crate that is installed at the outer edge of M1. About 10 PS-boards (the number depends on a station where the sector is installed) and an HSC crate are prepared to handle signals for each own 1/12 sector.

Digitized signals from Amplifier- Shaper- Discriminator (ASD) boards attached directly to TGC are inputted to Slave Board ASICs (SLB IC) after delay adjusted and bunch crossing identified in Patch-panel (PP) ASICs (PP IC). SLB performs local coincidence to identify muon tracks coming from the interaction point with $p_T \geq 6$ GeV, and output information of r, ϕ and $\Delta r, \Delta\phi$ for every muon candidate (low p_T coincidence with 2-out-of-3 logic using M1 or 3-out-of-4 logic using M2 and M3). The PP and SLB ICs are mounted together on a PS board. The PS board mounts also electronics for the detector control system (DCS) [2].

We also use an anti-fuse FPGA on this board. The FPGA is called from its functionality as JRC(JTAG Route Controller). JTAG is actively used to make access of registers in PP and SLB ASICs. The present system has two independent ways to up/download the JTAG data with these chips, the one is the DCS line and the other one is the SSW line. The JTAG data set on this later line come from the VME HSC-CCI chain. JRC is used to switch the JTAG data route.

The output signals of SLB are fed into a Hi-pT board, which is installed in an HSC crate. The Hi-pT board contains Hi-pT ASICs (HpT IC). An HpT IC combines information from two (for doublet) to three (for triplet) SLB ICs to make a global coincidence to find muon tracks with $p_T \geq 20$ GeV (high p_T coincidence). HpT IC also makes data compression to send its output over a distance of about 90m with serial data transmission of high speed optical link (G-link) to the counting hut where the off-detector electronics are installed.

Signals for r (wire hit information of TGC) and ones for ϕ (strip) are separately processed in the independent streams up to hi-pT coincidence operation, and the sector logic (SL) installed in the off-detector part combines these two streams and makes a coincidence in $r-\phi$ to identify muon signals in two dimensional space. SL can also identify muon tracks with six different p_T thresholds. At maximum two highest pT muon candidates per trigger sector (72 trigger sectors/side) are selected after successful $r-\phi$ coincidence, and the information is sent to the MUCTPI (ATLAS level-1 MUon Central Trigger Processor Interface) .

Since hit information for both coordinates will be used not only for the trigger decision logic but also for the second coordinate information for the ATLAS muon reconstruction in offline analyses, a readout system must be implemented. Readout data are processed also in SLB IC which implements pipeline buffers during the LVL1 processing time and FIFO for selected events (derandomizer). At every LVL1 accept (L1A) signal, data are serialized in SLB IC and sent to a data multiplexer/compressor, which we call Star Switch (SSW).

ROD receives data from nine to ten SSWs. Data received by ROD are stored in its FIFO memory, which is prepared for every input channel. All the data stored in FIFOs are sorted and merged with the identical L1A identification number. ROD sends then L1A classified data to the ATLAS central DAQ facility in the end.

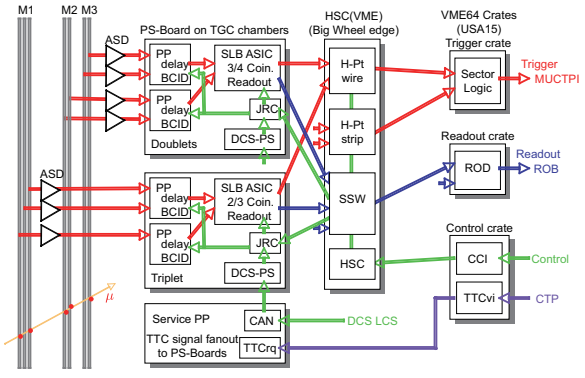

Figure 2: TGC electronics overview – components and connection scheme, original figure in color.

III. Sector Test

Since the mechanical structure of the 1/12 sector and its construction sequence has been reported previously in [3], we discuss mainly in this section the sector test procedure.

After chamber/electronics mounting and cable connection are done, the sector test dedicated for the electronics should be done in order to confirm the following items ;

1. functionality of ASD,
2. validity of signal cable connection,
3. functionality of a PS board – check operability and functionality of ASICs mounted on the board,

The above inspection is accomplished one by one through steps of register initialization, ASD test pulse scan, timing adjustment, and SLB test pulse scan. These steps are discussed in the following subsections.

A. Register Initialization

Total two kinds of ASICs (PP and SLB) and one FPGA are used in a PS board. They have naturally various registers, and these registers should be set some appropriate values before we do data acquisition work. By doing this setup procedure, we can roughly check overall functionality of components mounted on the PS board. Since all the registers are accessed with JTAG, we can check also the JRC functionality and the connectivity of the category 6 cables between SSW and a PS board.

B. ASD Test Pulse Scan

The functionality of ASD and cable connection between a PS board and an ASD on chambers can be checked using ASD test pulses. A PP IC generates a test pulse each time when it receives a test pulse trigger signal from TTC. After being adjusted through variable amplification and variable delay circuits the test pulses are injected into ASD. The pulses are eventually re-injected to the PP ASIC after being processed normally (amplified, shaped and discriminated) in the ASD chip. This is mechanism of ASD test pulse generation. If there are missing channels found in this test pulse scan, we can guess the problem of ASD itself or connectivity its cable.

With the ASD test pulses, we can also confirm the functionality of the delay circuit installed in PP IC. With this circuit, we can adjust the timing of 25ns/28 step independently channel by channel. Before the signal is inputted to the trigger decision logic in SLB IC, which is installed immediately after PP IC, all the signals must be synchronized accurately. The cable length from ASD to a PS board depends on their relative position in a sector, and thus cables of various length are used in a sector. The delay circuit can absorb this difference. By adjusting the signal timing from the cable length value, we can also check the functionality of the delay circuit, and synchronize the signals.

C. Timing Adjustment

In the ATLAS system, the trigger signal, which we call L1A (Level 1 Accept), will come after some microseconds of the latency time from the input time of the actual hit data into DAQ chain. In order to keep the readout data until L1A, we have to facilitate a pipeline buffer of maximum depth of 128 steps for all the input channels using FIFO memory. The depth is adjustable according to trigger latency. We have to adjust the timing of the pipeline output (depth) just on the L1A timing. As the latency will be changed if the configuration of the trigger decision logic behind the SLB IC are modified, it is important to confirm that the pipeline buffer adjustment works fine. By measuring the timing difference between the ASD test pulse and L1A, we can calculate the pipeline depth. The value can be stored in a 7-bit register in an SLB chip. We have confirmed the validity of the adjustment from a hit map.

In Fig. 3 we show a result of the delay test of 16 channels in an ASD. After evaluating the nominal delay value, we have artificially changed the delay values for 16 channels commonly. In the readout sequence, we must keep the hit data of the L1A bunch (called current bunch), the previous and the next bunch. In this figure, we can find how many channels out of sixteen are identified in the previous, current or next bunch. Most of the data are identified in the next bunch if we increase the delay value from the nominal value while all the data are still in the current bunch if the increasing time is kept less than 25ns.

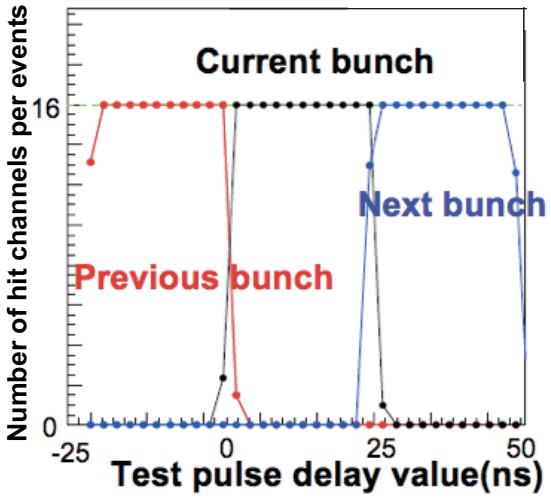

Figure 3: A result of the delay scan for one ASD, original figure in color.

D. SLB Test Pulse Scan

The SLB chip has also test pulse generation circuit. We use test pulses from this circuit (SLB test pulse) to diagnose the functionality of the readout part. In SLB there is a test pulse pattern register. By setting one/zero to a bit of this register we can control the test pulse on/off for the corresponding input channel. We have used this test pulse to validate the readout chain from SLB up to ROD. Frequency of the test pulse can be adjusted remotely from TTC. Although we can check the functionality of the trigger logic using this test pulse pattern register facility,

we have not actively used this method. Validity of the trigger logic function in SLB was confirmed through the cosmic ray test described in the next section.

IV. Cosmic Ray Test

We have used cosmic rays not only for synthetic test of the chambers but for the functionality check of the TGC electronics also. Using of all the seven layers (one triplet and two doublets) with full TGC trigger logic to find cosmic ray muons is unsuitable because the trigger window is formed in pointing geometry (in the TGC trigger scheme muons are assumed to come always from the interaction point to keep low the background muon rate). In addition, only a temporary gas system for TGC has been available for this test, and the chamber efficiency was estimated to be at most 20% with this gas system (Co2 was used).

We have achieved the cosmic muon trigger using a specially arranged local trigger logic with solely a triplet or a doublet. In this case the region to check the validity was limited within the trigger logic mounted in SLB IC. Although this is not a full debug to the complete trigger chain, we have checked the functionality of the SLB trigger logic in this manner. In Fig. 4, we show the hit maps of wire (r-coordinate) and strip(ϕ-coordinate) channels using one quarter parts of a sector for M3 wheel. In this part, we have total six different types of chambers. In the hit maps we have shown the ones of five types (called T5, T6 to T9). The difference of the type is the size of trapezoidal shape. The chambers from T5 to T9 are aligned with r coordinate from inside to outside. Geometrical sizes of individual chambers are adjusted to form a small sector shape if we lay the five chambers in appropriate way.

For this small sector configuration, as the trigger condition, we have set the two hits out of the two layers (2-out-of-2) on top of the standard low-p_T muon identification logic, and we made logical OR of signals from all the trigger units for the cosmic muon trigger.

Since the five chambers are aligned in r-direction with the overlap regions at the boundaries, the abscissa in the wire hit map covers r-coordinate continuously over 10m. Bumps shown in the map observed come from the double counting of the overlap regions.

In the hit map of strips we have merged five different hit maps into one histogram. ϕ-coordinate are all common for all the hit maps since all the chambers occupy the same ϕ region in the small sector.

Doing the cosmic ray test and inspecting hit maps as shown in the figure, we have debugged the low p_T trigger logic installed in SLB with the actual muon signals coming from TGC. The trigger rate observed was 20Hz, and it is well consistent with the predicted value with the sector area, chamber efficiency and trigger condition.

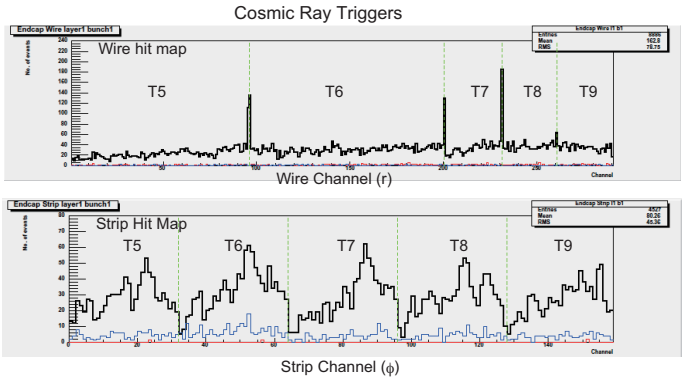

Figure 4: Hit maps for wire and stripes with the cosmic ray triggers (M3 doublet). The data were taken from 1/4 of a whole sector in which five geometrically different chambers (from T5 to T9) are used.

V. Summary

We have usually done the sector test and cosmic test immediately right after the sector construction was completed, and made debug of the whole electronics mounted on the sector. The number of total sectors are 72 all in all, and the number of total electronics channels exceeds 320 000. For such a great deal of channels, we encountered naturally many problems through the tests, but most of the problems could be identified the reasons. These were broken ASD, incomplete ASD installation, damage of cable line(s), connectors or ASICs. Once we have identified the reason of a problem, we have cured the problem in principle immediately - changed the bad cable, component or even board itself if the problem is concerned with several components. There were of course many missing channels also due to mechanical problem of chambers. In this case we have changed the chambers.

We have had, however, a problem that bothered us long time to speculate the right reason. Since there are many users in this community to use this component, we would like to discuss the problem.

We use the LVDS serializer/deserializer "SN65LV1023 (Tx)-SN65LV1224B (Rx)" chipsets [4] for serial data transfer from a PS board to both a SSW and to a Hi-pT board. As discussed previously we use the category 6 cables (15m length) for these connections. This serializer part was found broken frequently (at maximum 10% of chips out of 70 chips used in a sector was found out of order). After long struggling to identify the problem, we eventually speculated that the chip was broken as we just connected the cable. As we show in Fig. 5, difference of signals through the normal and broken ones are apparent from the oscilloscope measurement.

The source of the problem may come from the charges stored in the category 6 cable. If we connect the cable with the serializer, then huge amount of charge are flowed to the serializer (Electrostatic Discharge (ESD) phenomena), and it is broken consequently. After conceived this idea and taken the discharge procedure before the cable connection, the serializer problem was almost eliminated. Please note that TI released re-

cently the new chipset of LVDS serializer called SN65LV1023A which is just an updated version of SN65LV1023, although this update may not be related directly to this problem.

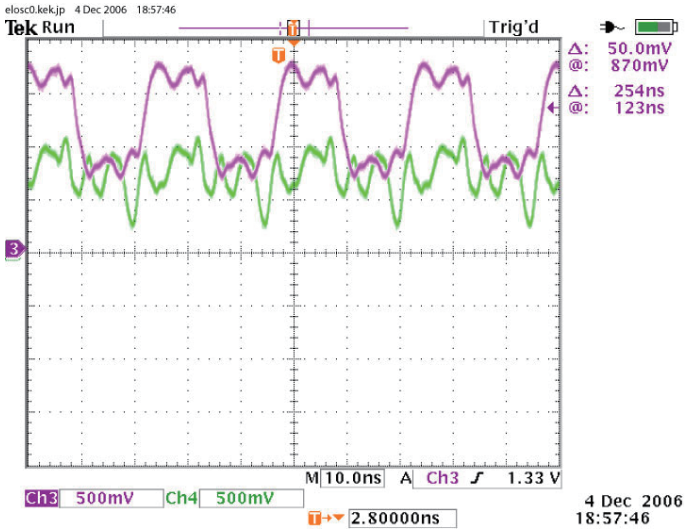

Figure 5: Output signal waves of the normal and broken LVDS serializers. White noise shape are found in the output from broken one while regular pulse shape with 40MHz clock is the one come from the normal serializer.

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