Proposal, development and test of an analog front-end electronic board for Nemo telescope

L. Caponetto[d], A. Gabrielli[a,b], E. Gandolfi[a,b], F.M. Giorgi[a,b,*], D. Lo Presti[c,d], N. Randazzo[d]

[a] Università degli Studi di Bologna, Dipartimento di Fisica
[b] Istituto Nazionale di Fisica Nucleare, sezione di Bologna
[c] Università degli Studi di Catania, Dipartimento di Fisica
[d] Istituto Nazionale di Fisica Nucleare, sezione di Catania
[*] Corresponding author, on behalf of the NEMO collaboration

giorgi@bo.infn.it

Abstract

The NEMO collaboration is involved in the R&D of the main technologies for the project of a km^3 scale underwater neutrino telescope. The proposed detector is made up of thousands of Optical Modules (hereafter OM), spread over the entire volume for Čerenkov light detection. Each OM is equipped with a photo multiplier tube (PMT) and an electronic circuit for data acquisition and transmission (DAQ-Board). This work points out the possible benefits of a hybrid solution based on an analog ASIC (Application Specific Integrated Circuit) employed for the analog signal acquisition and an FPGA (Field Programmable Gate Array), a digital programmable IC (Integrated Circuit) which performs the data acquisition and the data transmission.

I. INTRODUCTION

There are some observed astronomic phenomena which still are not explained by the current standard theories; such events involve the production of cosmic Ultra High Energy (UHE) particles (with observed energies up to 10^{20} eV) and they may yield an associated flux of high-energy neutrinos.

Considering the flux of UHE neutrinos, estimated by theoretical models, a km^3 scale detector is needed for astronomic research [1]. Neutrino has in fact a great advantage over photons and protons: the lack of electric charge and the low cross section let this particle propagate straightforward and for very long distances. These properties are useful for the deep-space astronomic researchers who, in the last decades, are giving neutrinos a prominent role in many deep-space investigation techniques.

For this reason the activity of the NEMO collaboration has been mainly focused on the development of key technologies for the km^3 underwater telescope and on the research and characterization of an optimal site for the detector installation.

The first to propose water as a cheap and useful target was M. A. Markov in the early Sixties [2]. The fundamental effect, on which the detection is based, is the emission of Čerenkov light by the muons created after a UHE neutrino collision with the target. These debris take most of the incoming neutrino energy becoming so ultra-relativistic particles propagating nearby in the same original direction.

Like in other underwater Čerenkov detectors such as ANTARES [3], another important experiment towards the km^3 telescope, light detection is performed by PMTs with a sensitivity down to single photo-electrons.

No solar light can reach a depth of 3500 m beneath the sea level, hence solar photons will not provide background noise. However there are other sources of photons at this depth, such as ^{40}K decay, bioluminescence and atmospheric muons.

Atmospheric muons can travel for many kilometers under the sea level before being absorbed, and so they must be distinguished from the ones formed after UHE neutrino interactions. Since only neutrinos can cross the entire Earth diameter almost without being absorbed, every upward muon should be considered as produced by a neutrino interaction. Directional information is hence very important for this kind of experiment and, considering the necessity to perform astronomic researches, the NEMO collaboration is developing a neutrino telescope with an angular resolution which is, according to several simulations, much less than one degree.

II. THE TELESCOPE

The proposed structure for the experiment is a three dimensional lattice of optical modules, each one containing a PMT and the related front-end electronics, spread over a volume of 1 km^3. The necessity for such a huge detector is imposed by the very low neutrino cross section with ordinary matter. The mechanical support for all these sensitive modules is a rectangular grid of towers, each one made up of 18 floors connected by flexible metallic cables, an anchor at the bottom and a floater on top providing the vertical traction.

Many sites in the Tyrrhenian and Ionian Seas have been studied by the collaboration, and some of them have been pointed out as optimal for this kind of telescope [4]. The optical attenuation length, the current speed and the bioluminescence are the most important water properties that have been investigated. The site known as *Km3*, situated 80 km away from the coast of Capo Passero (Sicily), seems to be particularly suitable, even for its sea floor smoothness. In December 2006 a prototype tower, consisting of 4 floors only, has been deployed few kilometers away from Catania for test purposes. For this reason the name of Test Site was given to this location and the whole testing operation is called Nemo Phase-1.

Nowadays is under development a later and more complete testing facility called NEMO Phase-2 which will be made up

of a complete 18-floor tower housing 72 OMs to be deployed in the *Km3* site. Two floors of the Phase-2 experiment will be dedicated to new R&D projects about the front-end acquisition system, in order to improve it by new technologies and new acquisition strategies. The remainder 16 floors will be equipped by almost the same technology adopted in NEMO Phase-1 [4].

III. Board description

The data acquisition board described in this paper is a prototypal front-end developed on mechanical and electronic specifications of the Nemo Phase-1 OMs (see Fig. 1). This solution is based on the full custom chip LIRA (analog delay line from the Italian acronym) for PMT anode and dynode signal analog sampling [5]. This board integrates the analog front-end technology with a reconfigurable digital control logic device for data preprocessing and transmission with the aim to be fully compliant with current acquisition apparatus deployed in the Test Site.

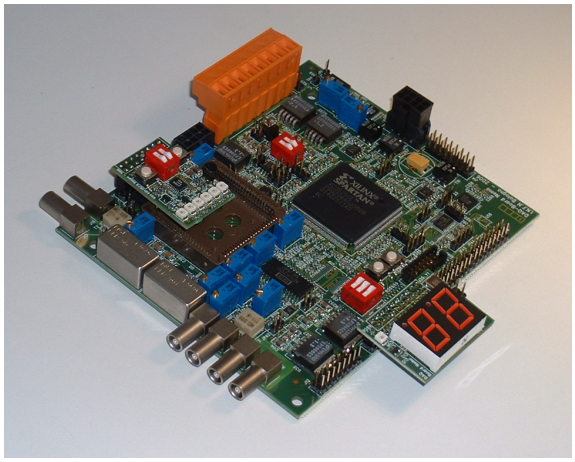

Figure 1: The DAQ board

A. Layout overview

The board has been realized on a four layer PCB (Printed Circuit Board): the top and the bottom layers were used to route signals, and the inner ones for power distribution and ground planes. To meet the Phase-1 OM mechanical constraint the layout was developed over a 130×110 mm surface area, 10 mm wider on each side than the Phase-1 acquisition board called FEM [6] but still Phase-1 compliant. The mounting holes are compatible with the retention system at the base of the present PMTs. The board is, as suggested before, a mixed signal PCB and this imposed severe layout constraints in addition to those due to mechanical compliance and room budget. A well known issue is in fact the trend of digital electronics to induce noise on analog traces of the PCB; to avoid this, particular layout strategies were taken into account.

First of all the analog devices have been placed together and apart from the digital ones subdividing the board topology into two dedicated areas: one half for the analog front-end and one half for digital data conversion and transmission to reduce digital noise cross-talk. Digital devices introduce also high frequency noise on the power supply because of their fast transient current absorption. To provide less noisy power to the analog memory, to the A/D converters and to voltage-reference resistor ladders dedicated voltage regulators were used. In the ground inner layer the metal plane is divided into two parts, each one under the relative analog or digital half of the board.

B. Power sources and distribution

Power supply for the whole OM comes in a 5 V voltage which, under operative conditions, is supplied by the FCM-b (Floor Control Module board): the first level data concentrator which the OM is directly connected to [7]. An auxiliary power supply connector allows to connect the board to laboratory instrumentation. The FCM-b delivers power to each OM through the same physical medium used for data transmission. Two pairs of twisted cables are used to send data with a differential standard, one for the incoming instructions and the other for event transmission toward the data concentrator FCM-b. Exploiting a 5 V common mode voltage difference between these two transmission lines it is possible to power the whole board and the high voltage module required by the PMT. The circuit for signal extraction and galvanic decoupling is the same of the current digital front-ends mounted on Nemo Phase-1. As mentioned before there are dedicated power supply planes for the analog and digital circuits for a total amount of five voltage regulators (three digital, two analog) and one 5 V stabilizer. The FPGA device needs to be powered at three different voltages, supplied by three digital regulators: 3.3 V for the output drivers, 2.5 V an auxiliary power supply for specific embedded device such as digital clock managers, and 1.2 V for the digital logic core. Most of other external digital devices such as the on-board PLL and configuration proms, etc... share the same 3.3 V supply used for the output drivers of the FPGA. The analog memory and others analog devices, such as the ADC input interface and the read-out multiplexer, are powered by 3.3 V or 2.5 V dedicated analog voltage regulators.

C. Debug detachable modules

For test purposes two detachable debug modules were added. They integrate a led display, a temperature sensor, a quartz oscillator and two push buttons and switches. This solution allows to save a considerable area on the main board and allows to remove all the light emitting electronics foreseeing a test with a real PMT in the dark room.

D. Clock infrastructure

The capability to reconstruct a muon track with this detector, is provided by a sharp timing of the events: for this reason all the front-end modules work synchronous to the same clock. Each OM receives a 5 MHz Master Clock on a twisted pair cable then a PLL (Phase Locked Loop) device multiply the frequency by four to obtain a 20 MHz clock. A dedicated multiple clock buffer IC distributes it to the FPGA, to the LIRA chip and to the ADC. The 200 MHz sampling frequency is provided only internally in chip LIRA by an integrated PLL.

The digital logic implemented inside the FPGA is synchronous with the 20 MHz clock using it to generate the 20 MBaud up-link data stream, to control the acquisition process and to control the A/D sample converter.

E. Analog front-end

The front side of the analog front-end is the PMT signal conditioning electronics. The aim of this circuit, made up of inductive transformers, passive filters and resistors ladders, is to decouple the PMT anode and dynode signal from the analog memory, and to adapt the impedance of the the signal to that of the memory. The conditioning circuit include also an 80 ns delay line, corresponding to the time taken by the trigger to analyze the incoming PMT signal.

The T&SPC (Trigger and Single Photon Classifier) unit, is integrated inside the LIRA chip and it is used to compare the anodic signal to different voltage thresholds: it triggers the acquisition process when the lower threshold is crossed, then classifies the pulse dynamic range with a higher threshold. A time threshold is also used to classify a narrow single photo-electron pulse or a close double shot or a complex over-threshold waveform. When the signal classification time has elapsed, the results are sent to the control logic and the analog memory starts sampling the delayed anode and dynode signal in two of its memory lines.

An analog memory line, or channel, is an array of capacitors which stores the input signal into a discrete number of analog samples. Sampling both anode and dynode pulses of each photo-electron extends the dynamic range of acquisition: the anode pulse is in fact the same dynode signal about a factor of 10 higher gain. A third memory channel is used to sample the 20 MHz clock signal for successive timing elaboration. These three memory channels, which sample simultaneously at 200 MS/s, form a memory block, which is made up of 3×250 memory cells; this means that a hypothetic continuous sampling would last up to 1.25 μs.

The number of acquisition samples for any given kind of event (long/short, anode/dynode dynamics) can be easily modified because this parameter is directly controlled by the control digital logic (FPGA). In order to reduce the dead time, there are two memory blocks inside the chip LIRA: when one is in sample mode, the other is reading out data at a 20 MHz rate. A read out operation of an entire block takes 12.5 μs (50 ns $\times$ 250 cells), ideally supporting a short-event rate of 2 MHz (10 sample per event, 25 events over 12.5 μs). The successive bottleneck introduced by data formatting and data transfer (discussed later) makes impossible to continuously afford such a high rate. Nevertheless it is possible to sustain short bursts of 2 MHz short-event activity, and time duration of supported bursts, after which the OM would go blind, depends only on the digital FIFO depth.

For every crossing of the lower-threshold, the T&SPC generates a start pulse which is received also by the digital logic which should manage the analog memory allocation.

F. Acquisition digital control logic

The control of the chip LIRA during the acquisition and read-out processes is provided by a FPGA, allowing a more flexible acquisition strategy. The LIRA chip contains the trigger and the classifier, the external control logic takes into account the information provided by these units and then directly control the memory usage. The control firmware keep trace of the LIRA read/write address pointers: in this way it is possible to know when a memory block needs to be read or when it is ready to write again.

When a start pulse is generated by the T&SPC the firmware immediately enables the memory block that is in write mode to sample the waveform. At the same time the classification of the pulse is stored: it will be recalled later at the moment of sending the data packet. When the acquisition of an event fills in a memory block, the FPGA tries to switch it in read mode if the other one has been already read [8].

When a memory block is set in read mode by the digital control logic, the read out and data conversion process starts. The conversion is performed by a pipelined ADC with 10 bits of resolution working synchronous with the 20 MHz sample outcoming rate. An analog multiplexer is required to route the correct LIRA output (anode/dynode) to the A/D converter since a memory block reads out its channels all together. The control logic switches in real time the MUX on the right channel taking into account the previous classification asserted by the T&SPC: a lower signal should be read from the anodic channel which grants a higher gain, in case of a higher pulse the dynodic channel will be selected. Digital data is then stored in a FIFO, implemented inside the FPGA, waiting to be packed and sent.

The clock waveform sampled in the third channel of each block contains the time information of the corresponding event. The firmware implements a special algorithm to extract from its shape the standard 16 bit time stamp.

G. Floor Control Module interface

Once data have been digitized, labeled with the proper time stamp and stored in a FIFO, a specific component implemented inside the FPGA, called Data Pack and Transfer Unit (DPTU), formats the data packets and send them towards the shore. In the Phase-1 experiment the first data concentrator to which the DAQ board is connected is the FCM-b. It is connected to the all 4 OMs of a floor and it is designed to gather the data and to send them to the shore station [7]. The communication protocol adopted between the OM and the FCM is proprietary and the board described in this work has been developed to be compatible with it.

The communication is serial, bidirectional and synchronous, with a dedicated channel for the clock distribution. Both data channels use differential signaling with 5 V difference in their common mode voltage to bring power the DAQ-board. The circuit to extract the DC component from the data stream has been realized on the base of Phase-1 FEM project [6]. In summary: three pulse inductive transformers decouple the data lines and the clock channel, three resistor-ladders recover the common mode voltage for the LVDS and RS485 standards and, in the

end, specific transceivers are connected to the FPGA.

H. On-line reconfiguration option - Safe Dual Boot

A particular architecture was developed to give a maximum flexibility of the firmware even when the board will be integrated on a tower and deployed. The goal is to achieve the remote programmability of the FPGA without introducing extra smart components but granting a safe reboot in case of upload failure. Since the FPGA is responsible for the communications, a bad reconfiguration would compromise the whole OM. For this reason another PROM was added to retain a safe and permanent configuration file to be recalled in case of necessity.

The concept is illustrated in Fig. 2. The configuration stream of the two PROMs is multiplexed towards the FPGA: the external multiplexer, driven by the FPGA itself, is latched and interconnects the safe and permanent PROM as a power-on default. In this way it is always possible to return to a safe tested version of the firmware switching off and subsequently on the power of the board.

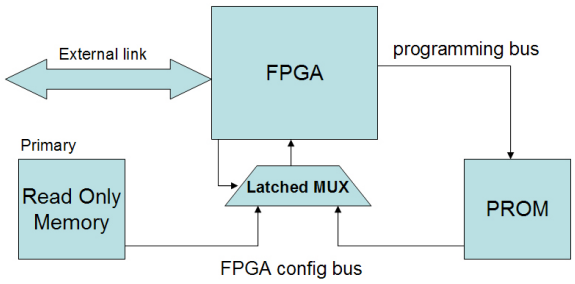

Figure 2: Safe Dual Boot architecture

IV. Board testing

Different testing setup were prepared to determine the efficiency and the performance of the board.

The first test bench concerned the digital logic components. The JTAG port of the board has been interfaced to a PC with an USB adapter and several Boundary Scan configurations were tested. All the digital devices were available on the chain: the FPGA and the two PROMs were correctly detected and programmed. Then we tried a power-on bootstrap of the board observing that the auto configuration of the FPGA by the primary PROM worked properly. Further tests involved the Safe Dual Boot resource. Hence we programmed both the PROMs with the JTAG cable: on the primary PROM we stored the configuration for a down-counter which switches the external latched MUX to the secondary PROM when it reaches the zero and then it sends a reconfiguration pulse to the FPGA itself. On the secondary PROM we downloaded a simple code displaying a double “8” on the seven-segment display. Afterward we proceeded to physically reset the board: just after the power-on the primary firmware was loaded, we observed the down-counter’s steps on the display. When the counter reached zero the FPGA reconfigured itself and then displayed a double 8. Repeating the procedure led to the same results. At the moment the secondary PROM has been programmed directly by the PC connected to the JTAG port, so we just proved that the hardware works. To test the definitive and complete solution a firmware download protocol should be implemented and tested.

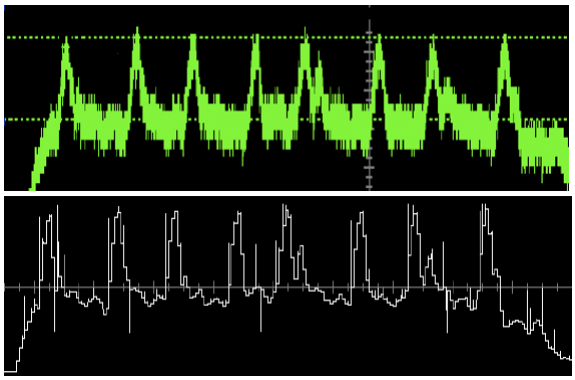

Figure 3: The analog waveform during the LIRA read-out and the relative digital data.

The second testing setup involved the analog acquisition with the chip LIRA. The FPGA was programmed with the acquisition control firmware and, in place of a real PMT signal, an equivalent pulse has been shaped with an arbitrary waveform generator. This procedure demonstrated the correct interaction between LIRA and the FPGA and confirmed the reliability of the proposed architecture. The FPGA managed correctly the read/write cycles of the analog chip and stored digital samples in an embedded FIFO. With a logic state analyzer we studied the correspondence of the digital waveform acquired with the analog pulse train. In Figure 3 is presented the result of the comparison.

The latter test setup was realized to check the communication protocol and the data flow towards the data concentrator FCM-b [7]. As shown in Figure 4 the entire data transmission chain of the NEMO Phase-1 experiment has been installed in our laboratory, from the data acquisition board to the data storage in a hard drive of a PC. The chain consists of the DAQ-board, the off-shore FCM-b and the on-shore FCM-b connected to a PC by a PCI bus. With this setup we tested the slow control handling, and the data transfer over the synchronous proprietary protocol implemented between the DAQ-board and the off-shore FCM-b.

Figure 4: Communication test bench

V. Conclusions

The aim of this work was to realize a front-end prototype electronic board based on the multichannel analog acquisition ASIC LIRA. It was realized to comply with the Optical Modules integrated on the NEMO Phase-1 mini-tower and capable to replace, in principle, the present ones. The improvements brought by this analog technology lead to a substantial increase in the linearity of the the signal to many hundreds of photo-electrons and a notable reduction in the power consumption.

Accurate tests were performed about digital logics and acquisition procedures. At the first power-on the board showed a good overall behavior, no short circuits were detected and all the power-monitor LEDs switched on with a total power consumption of about 700 mW. All the digital logic devices have been tested, including the SDB architecture.

The front-end electronics were tested emulating a PMT with a pulse generator at a rate of 80 KHz, as observed in the test site.

The data transmission protocol is now under test.

References

[1] J. G. Learned, K. Mannheim. *High Energy Neutrino Astrophysics*. Ann. Rev. Nucl. Part. Sci. 50 (2000) 679-749.

[2] M. A. Markov. *On high energy neutrino physics*. Proc. 1960 Annual Int. Conf. on High Energy Physics (Rochester, NY - 1960) 578.

[3] V. Bertin et al. *First results of the Instrumentation Line for the deep-sea ANTARES neutrino telescope*. Astroparticle Physics 26 (2006) 314-324.

[4] E. Migneco, et al. *Status of NEMO*. N.I.M.A 567 (2006) 444-451.

[5] D. Lo Presti. *A VLSI ASIC front end for the optical module of the NEMO underwater neutrino detector*. N.I.M.A 567 (2006) 548-551.

[6] C. A. Nicolau. *An FPGA-based readout electronics for neutrino telescopes*. N.I.M.A 567 (2006) 552-555.

[7] G. Bunkeila. *Data transmission and acquisition in NEMO*. N.I.M.A 567 (2006) 559-562.

[8] A. Gabrielli. *Development of an electronic board for a neutrino telescope project*. N.I.M.A 556 (2006) 302-307.