Design of on-chip data sparsification for a mixed-mode MAPS device

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Abstract

The device described in the paper is built up of a bidimensional matrix of Monolithic Active Pixel Sensor (MAPS) and an off-pixel digital readout sparsification circuit. The readout logic is based on std-cells and implements an optimised technique aimed at overcoming the readout speed limit of future large-matrix pixel detectors for particle tracking, by matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers in vertex detectors. The work extends a first version of a mixed mode device submitted on Nov. 2006 and implemented with the same technology.

I. INTRODUCTION

The paper describes the design of a mixed-mode ASIC that implements a matrix of MAPS cells along with a digital readout sparsification circuit. The MAPS cells have been fabricated and tested in the past years [1-3] with different layout flavours and now this ASIC, besides the MAPS, includes digital readout capabilities. In the past, a first small version of a mixed-mode design with readout capabilities was submitted on Nov. 2006 and preliminary tests show that the readout logic works properly [4].
In more detail, the ASIC presented in this paper includes the full custom cell, which is the matrix of MAPS, and provides all the control signals for the readout logic via std-cells. Plus, the mixed-mode design approach extends the performance of the chip as both the matrix and the readout logic have been developed separately and, eventually, integrated together. In particular the matrix of MAPS has been described with a VHDL-Verilog model and used as a macro-cell block within a bigger digital design. The global place-and-route has been also digitally designed. The design is implemented via the STM 0.13μm CMOS digital technology and was submitted on July 2007. The design has been carried out within the SLIM5 Collaboration [5].

II. THE CIRCUIT

The circuit is a digital architecture for a sparsified readout that interfaces with a matrix of 256 Monolithic Active Pixel Sensor (MAPS). It is the base for a prototype of a mixed-mode ASIC, namely Apsel3D. It readouts and sparsifies the hits of a matrix of 256 pixels. Once read, the hits are switched off. The matrix is divided into regions of 4 x 4 single pixels thus, 256 pixels are clustered into 16 groups of 16 pixels each, here-in-after named macro-pixels (MPs). In addition, the matrix is arranged in 32 columns by 8 rows of single pixels or, from a different viewpoint, in 8 columns of MPs, called macro-columns (MCs), by 2 rows of MPs, called macro-rows (MRs).
The global architecture might be considered as a circuit that work in two different operating modes, called custom-mode and digital-mode. If fact, it can be connected to the full-custom matrix of MAPS or to a digital matrix emulator composed of standard cells. In the first case the pixels may only be switched on via striking particles while in the second case the digital matrix must be loaded during an initial slow-control phase. The digital-mode allows to easily testing the readout capabilities without locating the ASIC under radiation. In addition, once tested the ASIC in digital mode the response can be compared with the custom-mode results. The two different implementations share the same matrix's I/O pins and may be selected and activated only one at a time. For both modes, before running, a slow-control phase is required to load an internal configuration. In particular, 16 mask signals should be provided to select the MPs, that are to be used and which are not, for examples in case they are too noisy or broken. Default mask, after a reset phase, is all-at-1, meaning no-mask. Moreover, it must be selected which of the two operating modes is wanted and, consequently, which matrix is to be enabled. The default mode, after a reset phase,

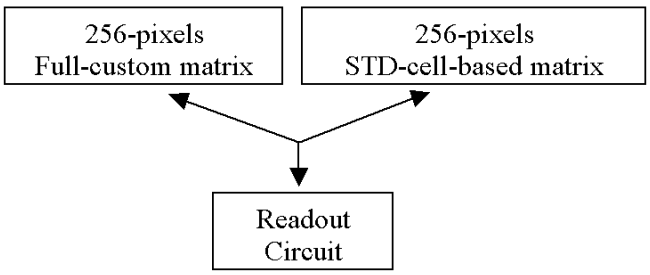

Figure 1: operating modes: custom-mode and digital-mode

is the digital-mode. In addition, only for the digital-mode, 256 registers should be loaded to simulate a given charge injection on the silicon area. Default registers, after a reset phase, are all-at-0, meaning no hits. All in all, readout circuit operates in the same manner for the two modes.
Fig. 1 shows a sketch of the operating modes of Apsel3D. Basically, let us say that the when the matrix has some hits (pixels that detect an over-threshold charge), it is swept from left to right and, all the hits present in a column of pixels, from 1 to 8, can be readout in one clock period (see Fig. 2). Moreover, the readout may imply a temporary data storing in an output queue hence, this readout operation starts as long as the hardwired readout queue (FIFO-like memory) has free locations. The hits' information is composed of space

coordinates associated with a time mark (time-stamp). The final space-time formatted data are then either sent to the output port, or temporarily stored in the FIFO-like memory in case the output port is busy sending previous hit information. Thus, in principle, the architecture can readout the matrix up to 8 hits at a time in case they belong to the same column and

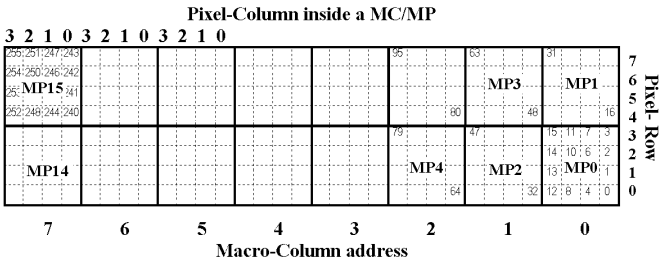

Figure 2: the matrix divided in MC, MR, MP and single pixels

can send the formatted data to the output but, at the same time, the output port can accept only one hit information at a time and this is why a queuing system is necessary.

II. The Matrix

Let's give a brief functional description of the readout logic. The matrix of pixels is grouped into 16 squared macro-pixels (MPs). Each MP is activated and frozen via dedicated wires while the reset and readout phases are carried out via wires that are shared over the entire matrix. The dedicated wires may also be masked, one by one, in case they would be too noisy or "burned", to avoid reading not-significant hits. At a given time, for example when a bunch-crossing signal is provided, the MPs that own at least one hit are seen via fast-or wires and frozen. In other words, when at least one pixel out of the 16 that build up a MP is on, a fast-or MP's output signal goes high. Then, when a bunch-crossing is over, all the fast-or signals of the MPs indicate the status of the matrix. These MPs are then frozen via MPs' dedicated wires. Thus, the readout phase can start over the activated MPs. The spatial coordinates of these MPs are associated with a time-stamp, whose registers are located outside the matrix. Then, one at a time, the columns of interest are enabled and the MPs' output data are written on a readout bus. Once the MPs have been readout they are set free. Then the process moves to another column of MPs. The readout phase involves one column of MPs at a time and this leaves the rest of the matrix free and capable of detecting new hits. Thus, the matrix may own hits, along with their personal time-stamps, belonging to different bunch-crossings. During the readout phase the matrix is swept and all the hits belonging to a given bunch are readout, reset and set free. The process continues till all the MPs have been readout. All these capabilities have been designed into a single die composed of a large full-custom matrix of pixels that is readout via a standard-cell based digital circuit.

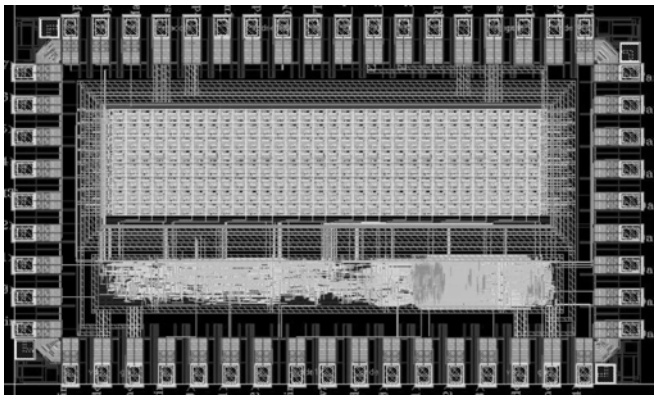

Figure 3: Apsel3D layout

Fig. 2 shows the organization of the entire matrix composed of 256 pixels. In more detail, there are:

- 8 macro-columns (MCs), addressed from left to right, ranging from 7 to 0,
- 8 rows of pixels, addressed from top to bottom, ranging from 7 to 0,
- 4 columns of pixels inside each MP addressed from left to right, ranging from 3 to 0.

In this view, each pixel is identified via a MC, a single column inside the MC and a pixel row. By converting these coordinated in digital logic it turns out 3+2+3 bits, i.e. 8-bits altogether which exactly address 256 pixels. This is the way the addresses are sent to the readout output port.

Fig. 3 shows the Apsel3D layout. The whole layout dimension is 2343.56μm by 1379.24μm. The pitch of the pads is 120.54μm on the left, bottom and right sides. The pitch of the top side pads is 114.16μm.

III. Conclusion

The work extends a first version of mixed mode device submitted on November 2006 [4] and implemented with the same technology.

The work has been developed within the SLIM5 collaboration [5] and the ASIC was submitted on July 2007 to STM 0.13μm CMOS digital technology. It will lead to future improvements to design a high-density thin MAPS detector with an on-chip sparsified digital readout system, for particle tracking, aimed at matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors.

IV. References

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