Serial Powering of Silicon Sensors

E. G. Villani[a] , M. Weber[a], M.Tyndel[a], R. Apsimon[a]

[a]STFC, Rutherford Appleton Laboratory

g.villani@rl.ac.uk

Abstract

Serial powering is a technique to provide power to a number of serially chained detector modules. It is an alternative option to independent powering that is particularly attractive when the number of modules is high, as in large-scale silicon tracking detectors for particle physics. It uses a single power cable and a constant current source. On each module power is derived using local shunt regulators. Design aspects of local shunt regulators and system aspects of serial powering will be discussed. Test results and measurements obtained with a silicon strip supermodule will be presented. Specifications of radiation-hard custom serial powering circuitry will be discussed.

I. INTRODUCTION

Current silicon detector systems for particle physics usually power individual detector modules independently. This means that each module has its own power supply. For large scale detectors, like the ATLAS Pixel detector and the ATLAS Semiconductor Tracker (SCT), this implies that tens of thousands of cables are needed to power the front-end electronics. The power cables are of the order of 100m long (one way) and their resistance (including return) can be as high as 4.5 ohms. The power consumed by the front-end electronics is typically tens of kW and power efficiency (defined as the ratio of effective power delivered to the loads and total power delivered by the power supplies) can be as low as 30% -50% due to joule losses in cables. For future detectors, with five or ten times more electronic channels, very serious problems arise if independent powering is considered: lack of physical space for 5- to 10- fold increase in number of power cables, too low power efficiency, excessive multiple scattering that leads to creation of secondary particles and very high cost. Serial powering provides an elegant solution to these problems and, as such, is of great interest to SLHC and ILC trackers.

In this paper, after an introduction to serial powering and its comparison with independent powering, properties of local shunt regulator needed in a serial powering approach will be discussed. Related design issues and experimental results of implemented shunt regulators will be presented. An over-current protection scheme for shunt regulation will be discussed and related experimental results presented. The latest experimental results from stave arrangements will be shown. Finally, specifications for a custom ASIC powering chip will be provided and discussed.

II. POWERING SCHEMES COMPARISON

A common method to provide power to a number of loads is to independently power them, namely each load is powered by a dedicated power supply. This method guarantees higher redundancy and flexibility, but quickly becomes cumbersome in terms of the number of power connections when the number of loads increases. In this respect a better approach would be to use a single power source to power a number of loads, connected in parallel. An alternative to the latter would be its Norton equivalent arrangement, consisting of a serial powering scheme, in which a single source provides power to a number of loads serially connected as in figure 1.

In the specific case of a system of silicon detectors, a serial powering scheme consists then of four basic elements: a current source, a series of modules, a shunt regulator in each module and AC or opto-coupling to provide communication between the modules and the external world. The specific serial arrangement is shown in figure 2. The number of long power cables can thus be reduced by a large factor, depending on the number of modules powered in series. Furthermore, the power efficiency can be increased hugely ([1], [2]).

In each module the shunt regulator usually provides constant voltage to the local load, normally the digital section. The series regulator connected to the output of the shunt supplies power to the analogue section. The serial arrangement sees each module sitting at a different potential, hence AC-coupling is normally required to communicate with the external world. The dynamic impedance seen from each module ground to the ground of the current source is the sum of the output impedances of the shunt regulators in between, thus the shunt regulator has to show low output impedance. This ensures a good global ground connection hence lower picked up noise.

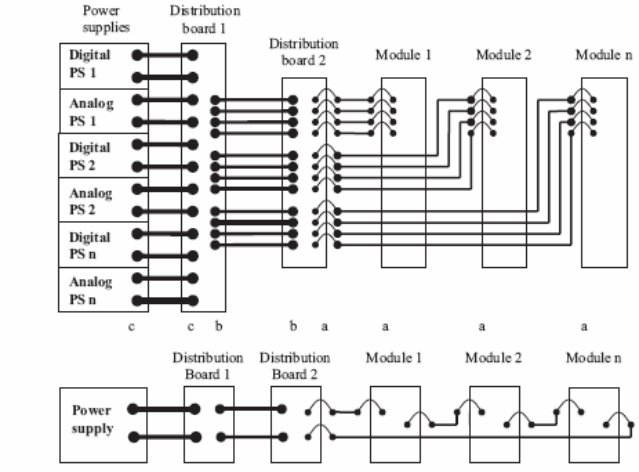

Figure 1: Comparison of an Independent (top) and Serial (bottom) Powering scheme.

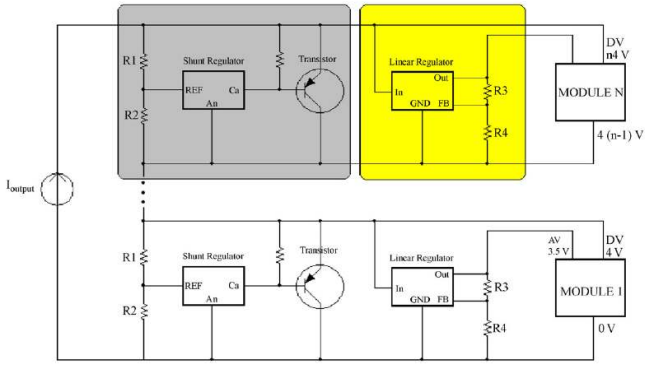

Figure 2: Example of a Serial Powering scheme.

III. SHUNT REGULATOR DESIGN

The schematic diagram of the shunt regulator implemented in the serial powering systems analysed over a period of two years is shown in figure 3. In figure 4 pictures of the actual boards used to implement the serial powering are shown. Each board includes the shunt regulator, the series regulator and three LVDS buffers for data communication plus passive components. The smallest board, consisting of a four layers PCB, is about less than 2% of the size of the biggest board: it was designed to be fitted on a stave supermodule, shown in figure 5, to carry out tests on serial powering scheme in a more realistic detector arrangement [3].

Initial tests performed on the shunt regulator showed a bias dependent oscillation at the output. An analysis of the small signal equivalent circuit predicted a reduced phase stability margin for higher ESR of the output capacitor. The oscillation essentially disappeared when C1, C2 in the original schematic were replaced with a low ESR rated capacitor.

To assess the performance of the shunt regulator in terms of output impedance a small sinusoidal current around 10mA peak to peak has been superimposed onto the DC bias current, nominally 500mA. The output of the shunt regulator has been monitored using an oscilloscope. Of both the small signal current and the voltage output ripple the most probable value (MPV) has been determined from histograms. The ratio of the two MPV is then taken as a measure of the MPV of the absolute value of the output impedance. A similar procedure was used to determine the phase output. A resulting picture of both output impedance module and phase is shown in figure 6.

The output impedance shows a corner frequency of around 1MHz, consistent with the open loop gain nominal plot of the TL431 employed in the design of the shunt regulator. For lower frequencies it remains below 1Ohm and reaches up to 70Ohm at 40MHz.

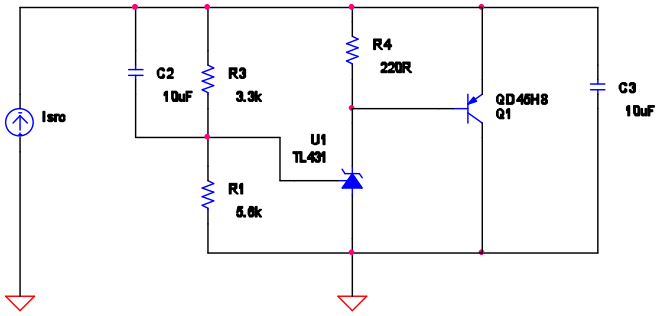

Figure 3: Shunt regulator schematic

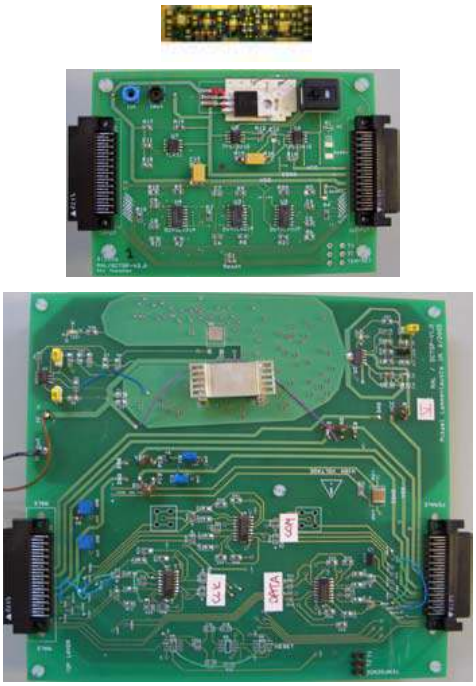

Figure 4: Serial Powering boards evolution: lower board size 150x150mm, middle 111x83mm, top 38x9mm. The boards implement essentially the same functionality.

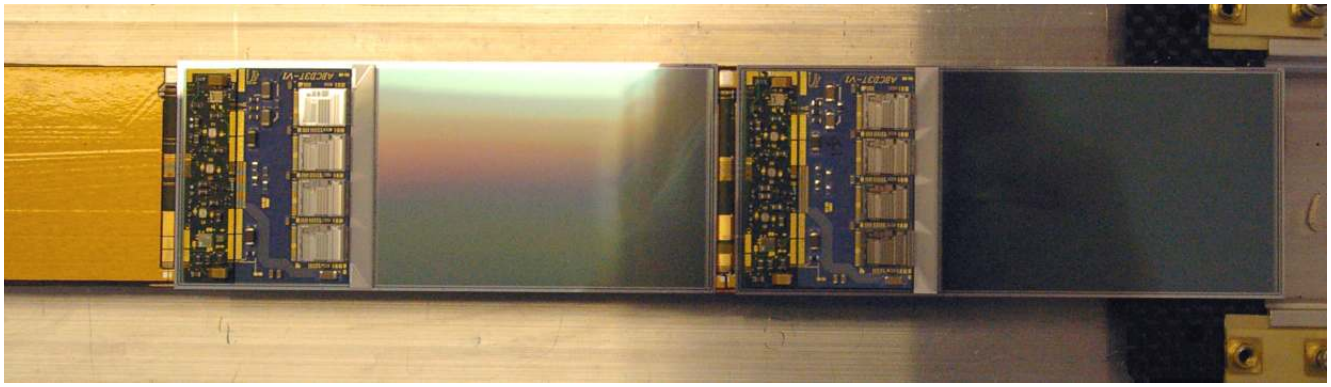

Figure 5: Serial Powering stave arrangement. Only 2 of eventually 6 modules are mounted.

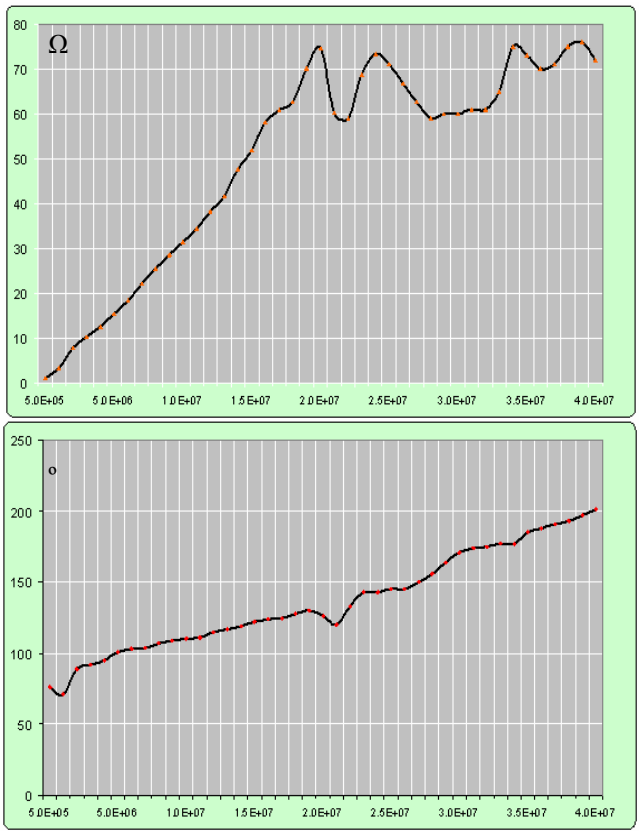

Figure 6: Module of output impedance (Ω) and phase delay (degrees) of shunt regulator vs. frequency.

As a result of the relatively low shunt regulator output impedance, each sensor can be referenced to the current source ground, rather than to the module ground. Namely, it becomes be possible to use a single HV power supply to bias a number of sensors, instead of using one bias for each module. This would provide another advantage in terms of cable savings, an important factor for short strips, figure 7.

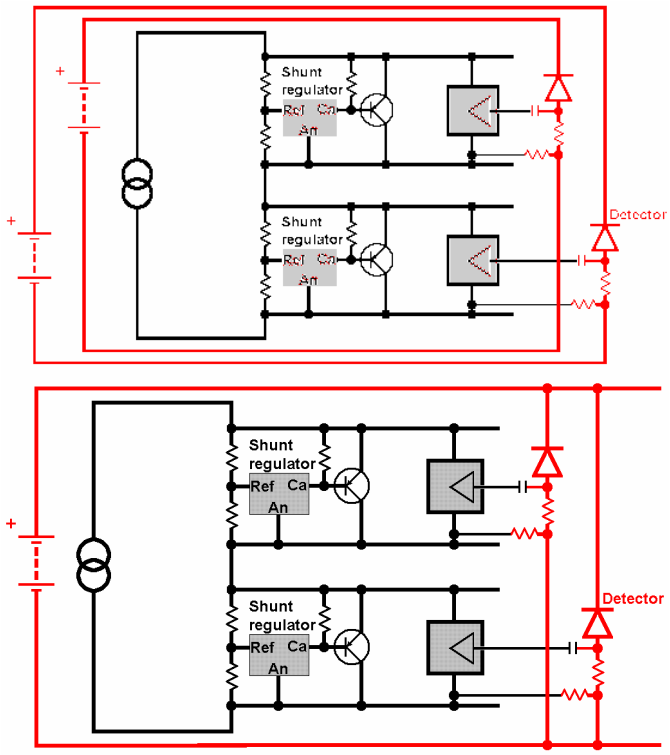

Figure 7: Comparison of single (top) and multiple (bottom) HV sensor biasing. In the multiple arrangement, a single HV line biases several sensors.

IV. Protection Scheme

Several failure modes have been identified and compared quantitatively with independent powering schemes. One failure condition sees the hybrid not properly operational as a result of clock missing. This in turn implies that less current is drawn by the hybrid thus a higher current flows through the power device of the shunt regulator. This extra power dissipation raises the regulator temperature, possibly resulting in some damage.

A test on the reliability of the regulator was performed by supplying it with up to 600mA. The load is a hybrid with no

clock and without cooling. The temperature of the regulator was measured using a thermal imager, see figure 8.

It can be seen that the power device temperature rises to approximately 130ºC in these conditions. A further test was then performed at 700mA for half an hour and the regulator performances were subsequently found unchanged.

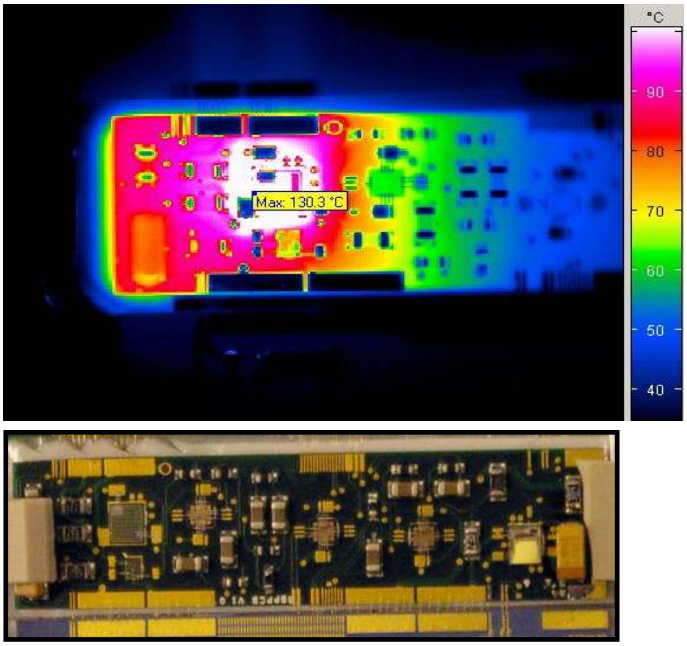

Figure 8: Thermal analysis of shunt regulator.

In order to limit the chances of damage or degradation arising from such over current condition, a general protection scheme has been devised and tested. In it the current through the power device is monitored and if it exceeds a set threshold for a set time it triggers a feedback path in the shunt regulator to decrease its voltage output, see figure 9. In this way the current keeps flowing along the serial chain as before, so as to keep the remaining modules operational, but the dissipated power by the shunt regulator in the faulty module is reduced.

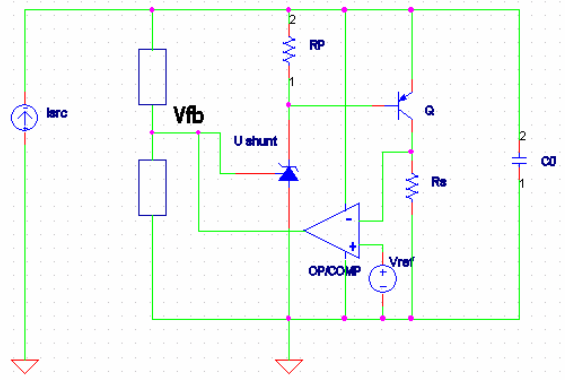

Figure 9: General protection scheme for shunt regulator.

In figure 10 some experimental results obtained from a prototype are shown: following an over-current condition from 40mA to 1500mA the shunt regulator's output voltage decreases from 4V to 1V in a few ms. It then recovers to the nominal value when the current is lowered. This voltage reduction could be also triggered digitally, provided the digital section is designed to work with a reduced voltage.

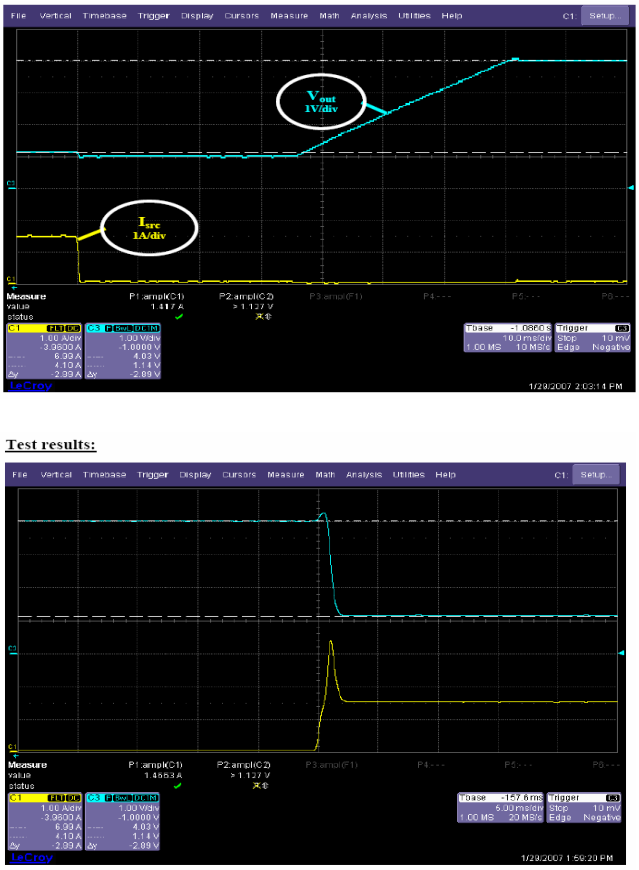

Figure 10: Experimental results of protection scheme.

V. TEST RESULTS

Some of the latest experimental results obtained from the serial powering scheme implemented so far are shown in figures 11and 12. More experimental results are available ([4]). It can be seen that noise performances of such powering scheme are comparable if not better than those of independent powering scheme.

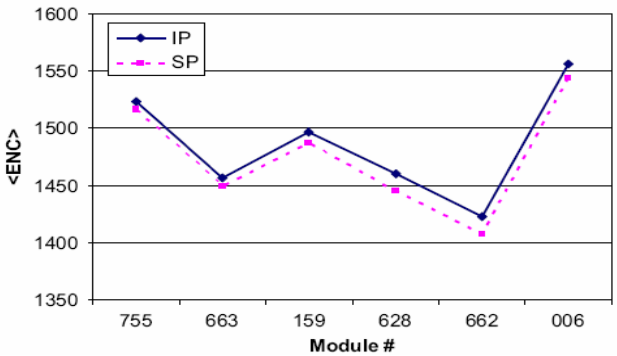

Figure 11: Average noise (ENC) for six SCT modules powered independently (IP) or in series (SP).

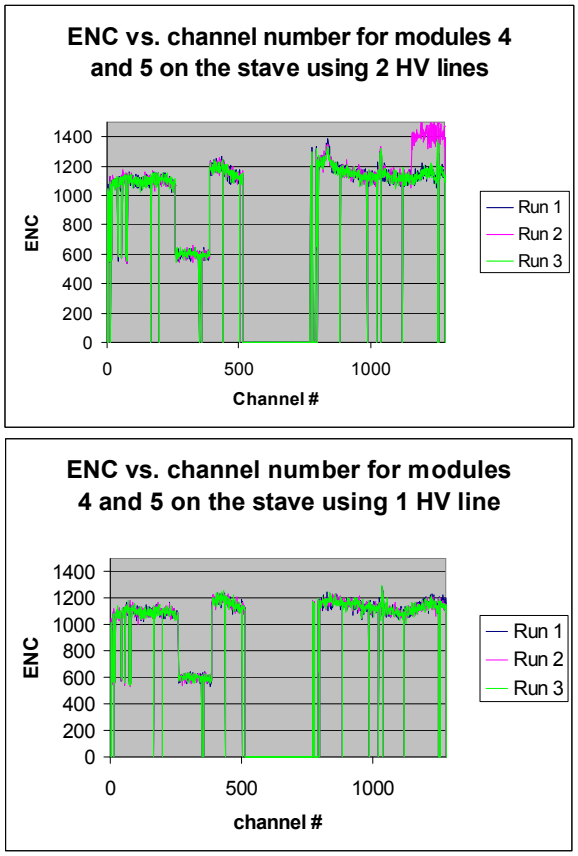

Figure 12: Noise (ENC) for stave fitted with two modules serially powered. Comparison between single (bottom) and independent (top) HV biasing. The missing channels are due to a chip on hybrid not bonded to sensor.

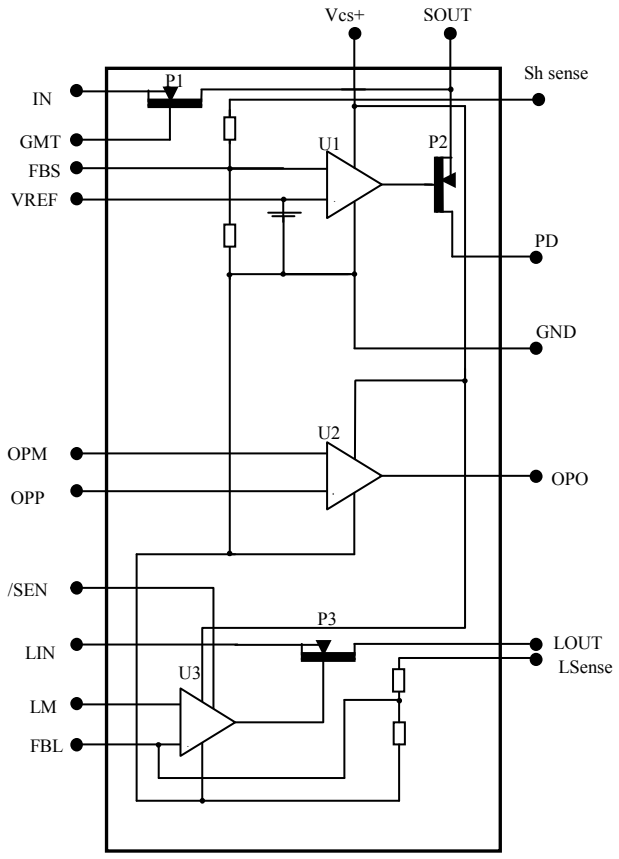

Figure 13: Schematic diagram of SMARP chip for Serial Powering Scheme.

VI. ASIC DESIGN

The next logical step in the Serial Powering scheme is to integrate all the needed functionalities into a dedicated ASIC. With this idea, specifications for a radiation-hard, general purpose, power supply IC to be used in serial powering schemes have been developed. A general schematic diagram of such chip, SMARP, is shown in figure 13. It includes a shunt regulator, a series regulator, an additional operational amplifier, a high power pass transistor and LVDS buffers (not shown here).

VII. CONCLUSIONS

The reliability and effectiveness of the Serial Powering schemes in increasing power efficiency, reducing the amount of material and cost has been demonstrated with several designs of increasing compactness. Of crucial importance in achieving good performances is the quality of the shunt regulator. The actual implementation has been thoroughly investigated and tested. The concept of an over-current protection scheme has been introduced and a prototype has been successfully evaluated.

The next crucial step is the design of a custom general purpose ASIC SMARP, integrating all the functionalities needed for a serial powering scheme.

VIII. REFERENCES

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