The Implementation of the power supply system of the CMS Silicon Strip Tracker

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Abstract

The power supply system of the silicon strip tracker of the CMS experiment provides HV bias and LV power to the 15000 modules of the detector, arranged into 1944 "power groups" and 256 "control rings". Around 1200 power supply modules, disposed on 29 racks, operate in a "hostile" radiation and magnetic field environment, 10 m away from the beam crossing region. They power the detector through $\simeq$ 50 m long custom-designed "Low Impedance" cables, adopting the sensing wire technique to compensate voltage drops. Detector "power groups" and "control groups" are powered by modules of different architecture, which are fed by 48 V sources, provided by AC-DC converters installed in the racks. This paper reports the experience acquired in the implementation of the system, the rack layout, the grounding scheme, the power budget, the heat dissipation on racks. A comprehensive Quality Assurance program ensured the performance, using a well defined protocol, shared with the board's manufacturer, for acceptance tests and failure detection.

I. INTRODUCTION

The tracker of the CMS experiment [1] at the LHC collider is composed of a central pixel detector, located at a small distance (R $<$ 15 cm) from the beam pipe, and of a silicon strip detector (SST), between 22 cm and 110 cm from the beam pipe, which covers the pseudorapidity region $|\eta| < 2.6$ (5.5 m length) [2].

The SST is subdivided into four sub detectors: four inner concentric layers ("Tracker Inner Barrel" or TIB) complemented by two mini-endcaps ("Tracker Internal Disks" or TID), six concentric outer layers of detectors ("Tracker Outer Barrel" or TOB) and two endcaps, each one composed by nine disks of detectors, named "Tracker Endcap" (TEC). Overall it comprises 15000 detector modules, featuring around 10^7 readout channels.

The signal readout is based on the APV25 front end (FE) chip [3]. Each detector module is equipped with either four or six chips, depending on the number of strips of the sensor. The digital control is performed by the "Communication and Control Unit" (CCU) chips. Several CCUs are daisy-chained to form a so-called CCU-ring (or control group). Each CCU-ring is powered by a dedicated power source.

II. THE SST REQUIREMENTS

The digital control circuitry partitions the SST into 256 CCU-rings. Each control group requires a dedicated +2.5V power line, with an average consumption of about 7 W, depending on the number of the control units in the ring.

Each SST module requires one high voltage (HV) bias (0-600V) for the sensors and two low voltage (LV) power regulators, respectively +2.5 V and +1.25 V, for the analogue FE and opto-electronics circuitry. The average LV current consumption is about 1.5 mA per channel, which, multiplied by the total number of readout channels, gives 15 kA current. The sensor's leakage current, even after 10 years at LHC, should still be well below 1mA [2].

Table 1: The SST power groups and the on detector power consumptions in standard conditions.

	N. APV	I2.5 [A]	I1.25 [A]	Pw[W]
avg./group	37	5.6	2.3	16.0
Max/group	56	8.4	3.4	25.2
Min/group	12	1.8	0.7	5.3
Total	72 784	10 066	4 731	31 079

The silicon strip modules are grouped into 1944 "detector power groups" in order to share the power services. Detectors belonging to the same power group belong also to the same control group and to the same cooling loop. Table 1 shows the main parameters characterizing the tracker groups.

The power demand of each group scales both with the number of modules and the number of readout channels. The consumption is roughly 260 mA per APV pair (including the consumption of the opto-electronics) plus 85 mA per module on the +2.5V line and around 120 mA per APV chip pair on the +1.25V line. A 10% spread around these values may be present, due to chip-to-chip variations. These values were measured on fully integrated detector structures, and are consistent with the FE chips specifications. The power consumption does depend on the settings adopted to configure the FE opto-electronics. Reference settings, suited for running at LHC, were identified for each subdetector; the consumptions quoted above are referred to as the "standard consumption" case.

III. THE POWER SYSTEM

A. Powering scheme

The power supply project for the CMS SST started in the year 2000 in Florence according to the following guidelines [4]:

- a modular system of "Power Supply Units" (PSUs) for the detector groups with both LV and HV regulators and of "Control Power Supply Units" (CPSUs) equipped with

2.5 V regulators, serving the CCU-rings;

- voltage regulators are placed outside the tracker volume. The sensing wire technique is adopted in order to ensure the nominal LV values on the load (+2.5V and +1.25V);
- the voltage is referenced on the detector. All regulators have "floating" return lines;
- PSUs and CPSUs feature a hard-wired safeguard system, ensuring the safe operation of the system;
- the power supplies are powered by two external +48V DC sources, coupled by means of the DC-DC technique: one source ($48\mathrm{V_P}$) for the regulators, the other ($48\mathrm{V_S}$) for the service electronics of the PSU/CPSU.

B. The EASY4000 system

The designed system was successfully implemented using CAEN technology, with the "EASY 4000" system. Two independent PSUs are hosted in one 6U high and 4.4 cm wide board, named "power supply module" (PSM, CAEN's A4601H). The "control power supply module" (CPSM, CAEN's A4602), has identical dimensions and hosts one CPSU. Up to 9 boards (A4601H and/or A4602) are hosted in one standard Eurocard crate (6Ux19"), which provides $48\mathrm{V_P}$ and $48\mathrm{V_S}$ rails, interlock and general reset bus lines. The first slot in the crate ("slot 0") hosts the interlock-card, which interfaces the interlock and reset lines to the "Tracker Safety System" (TSS) and to the "Tracker Control System" (TCS). Boards may be "hot inserted" inside powered racks; cables are connected through interconnect boards ("back boards") which form a patch panel at the back of the crate.

The control of the modues is based on mainframes (SY1527) hosting up to 16 "branch controllers" (A1676A). Each A1676A controls all the PSMs and CPSMs contained in up to six crates, through six CANBUS lines (one per crate).

Each PSU and CPSU features one microprocessor which manages the CANBUS communication and controls and monitors the voltage regulators. All communications with the microprocessor are opto-coupled, so to leave the voltage regulators electrically isolated.

Common hard-wired safeties featured by PSMs and CPSMs channels are: current limiters, over-voltage protection, temperature sensors. Reset and interlock commands are instead handled by the on-board microprocessor [4].

AC-DC converters, CAEN's A3486 ("MAO"), powered by the three-phase provided by the LV infrastructure, provide $48\mathrm{V_P}$ and $48\mathrm{V_S}$ to PSMs and CPSMs. Each MAO may be configured to provide either two 2 kW channels or one 4 kW channel, at an output voltage adjustable between 44 V and 52 V. Each MAO is remotely controlled through one of the CANBUS lines attached to the crates.

The power supplies are located in the "Underground Experimental Cavern" (UXC) at both sides of the detector, at a distance of around 10 m from the beams interaction point. They will stand a magnetic field of 400 G and a neutron flux of $3\ 10^9\ \mathrm{n/cm^2}$ (20 MeV equivalent) in 10 years at nominal LHC operation. As verified in experimental tests (see [5]) the A4601H and A4602 can operate in magnetic fields up to 2 kG and can sustain a neutron flux of $10^{10}\ \mathrm{n/cm^2}$ in ten years without significant degradation of their performance.

Table 2: The SST power supply channels: adjustable voltage ranges, max current (or power) and max voltage drop compensation. For the A4601H board only channels of one PSU are listed.

Model	channel	V at load	max I/pow	$\mathrm{V_{max}^{drop}}$
A4601H	LV0	2.3 - 2.75 V	13 A	4 V
(for each PSU)	LV1	1.15 - 1.35 V	6 A	4 V
	HV0-HV1	0-600 V	12 mA	-
A4602	LV0-LV3	2.3 - 2.75 V	7 A	6 V
A3486	CH0-CH1	44 - 52 V	2500 W	6 V

C. Racks

Table 3 summarizes the components of the entire SST power supply system. The power supply units are located on a total of 29 racks installed at three different levels of "balconies" situated at both the "FAR" and "NEAR" side of the detector in UXC. The system is controlled from the "Underground Service Cavern" (USC) by 29 branch controllers (one per rack) hosted inside 4 SY1527 mainframes. CANBUS lines are routed from USC to UXC through $\simeq$ 100 m long 50-pin multi-wire cables (one per rack).

Table 3: The SST power system components.

	Model	quantity	location
Mainframe	SY1527	4	USC
Branch Controller	A1676A	29	USC
Racks		29	UXC
EASY 4000 crates		129	UXC
interlock cards		129	UXC
AC-DC converters	A3486	78	UXC
PSM	A4601H	984	UXC
CPSM	A4602	110	UXC

Standard racks are 56 U high; six racks (out of 29) are limited to 46 U due to space constraints. The standard rack layout includes five crates and up to three MAO units. Rack cooling is provided by water cooled heat exchangers and turbines for the closed air-flow. Two turbines and five heat exchangers are required in 56 U racks in order to ensure effective cooling. The $48\mathrm{V_S}$ within the rack is provided by one channel of the first MAO; the remaining channel and the other two MAOs provide the $48\mathrm{V_P}$. The MAOs are under the control of a SY1527 and the dedicated branch controller in USC.

The layout of 46U racks comprises only four crates, two MAOs, four heat exchangers and two turbines. These special racks are disposed as "triplets", with one external MAO providing $48\mathrm{V_S}$ to three racks.

D. Detector power supply grouping.

Racks are populated according to a "block" scheme. One block is a group of one or more contiguous crates hosting PSMs and CPSMs powering the detectors of an integer number of

cooling loops. Typical block sizes are one, two (TIB,TID,TOB) or even three crates (TEC). For TEC one block corresponds to a full sector ($1/8^{\rm th}$ of one endcap, which includes 9 control groups and 48 power groups).

The choosen layout accounts for the grounding scheme of the detector (the circuitry of a cooling loop shares the same reference voltage) and the interlock functionality (in case of cooling failure, the interlock system interlocks all the crates hosting the power groups belonging to the failing cooling loop).

Other considerations in filling the racks are: load balancing (mix, when possible, high demanding with low demanding power groups), cable routing (the cable channel exits with respect to the rack position).

E. Dimensioning of the system

The power cable cross section, the PSU capability to compensate voltage drops, the heat dissipation on racks, the number of AC-DC converters and the total power available from the mains are the basic issues in dimensioning the system.

In order not to run the system at the edge of its capability, a 1.6 "safety factor" is applied on top of the "standard conditions" consumption reported in table 1, for both $\rm i_{2.50}$ and $\rm i_{1.25}$. These factors are intended to cover possible increase of the power demand due to (for example): variations of the FE settings from the "standard condition", aging of the detector (increased sensor's leakage currents, higher gains needed by the opto-chain); operation at higher voltages (if needed, LV voltages may be varied by about $\pm$ 10%).

Table 4: Power requirements in the "standard conditions" case and after the 1.6 safety factor is applied.

	Standard	safety
Avg. $\rm i_{2.50}$ per group	5.6A	9.1A
Avg. $\rm i_{1.25}$ per group	2.3 A	3.6 A
Power delivered to pow. groups	64 kW	137 kW
% on cables	48 %	57 %
Power delivered to CCU-rings	3.7 kW	8 kW
Total $48\rm V_P$ required	109 kW	215 kW
Total $48\rm V_S$ required	24 kW	24 kW
Total 48 V required:	134 kW	239 kW
Avg. $48\rm V_P$ required per crate	800 W	1700 W
$48\rm V_S$ required for one full crate	215 W	215 W
Heat dissipation per crate	570 W	810 W

Table 4 summarizes the global power consumption of the tracker. Globally PSMs and CPSMs can erogate up to 145 kW power. The limit is determined by the number of installed AC-DC converters, the total power available from three-phase infrastructure and the cooling infrastructure on racks. More than 50 % of this power is dissipated on cables. The control power requires about 6 % of the total. The total power envelope requested to the three-phase infrastructure [6] is 275 kW. About half of this power is dissipated on the racks, due to the limited efficiency of AC-DC and DC-DC conversions. Heat dissipation from 56 U racks may exceed 5 kW. Each crate dissipates on average 810 W; this includes the $48\rm V_S$ service power, which for a full crate is 215 W.

IV. The power supply module production

A. Prototyping

Good high frequency isolation and fast over voltage protection are among the aspects which were immediately addressed with the first PSM prototypes [4].

The isolation of each PSU channel from the surroundings is about 100 Ω at 5 MHz and increases at lower frequencies. This is important in a scheme working with floating independent channels.

When compensating the voltage on a long cable, special care must be taken to prevent the generation of over voltages whenever an abrupt current consumption variation occurs. Three actions are taken [4]:

- implementation of a fast hardware Over Voltage protection circuit ("crow bar") which quickly (order of 100 μs) limits the channel's output voltage whenever the sensed voltage is out of range;
- partitioning of the FE system in order to avoid simultaneous resets of all the APVs within the same power group, thereby limiting the current variations;
- adoption of special "low impedance cable" to power the electronics. Low impedance diminishes the amplitude of over voltages and helps keeping under control (no oscillatory behavior) the voltage after the transients.

Prototype boards were successfully deployed in several beam tests with detector setups (see [7] for example).

B. Production

The first fully integrated detector structures became available just before starting the production of the power supplies. Latest adjustments of the voltage regulators to the input impedances of the detectors were applied, which made a bit critical the transition from prototypes to production power supplies.

The evolution from prototypes to production was a bit critical. Just before going to production the transition to H-type ("hostile environment") boards was implemented. At the same time the first fully integrated detector structures were available and latest adjustments of the voltage regulators to the input impedances of the detectors were applied.

Two problems were identified after production was launched, namely a 600 Hz oscillation of the LV channels, which showed up only when powering real detector structures in data acquisition conditions, thus escaping any quality assurance procedure based on passive loads, and a synchronization problem in the ramp-up of the two LV lines under high load ($\rm i_{2.50} >$ 8A). These problems, which did not affect the prototype units, forced a minor intervention on large part of the production.

Some modifications to the grounding connection of the boards were also implemented. The PSM and CPSM front, back and lateral plates are all connected to the local ground on crates, together with the input $48\rm V_P$ and $48\rm V_S$ return lines coming from the AC-DC converters. The external shield of the power cables is floating at the power supply end, and is connected to

the detector structure at the cable detector end (at the "PP1" patch panel, see below). All crates in the rack are connected together; racks are soldered to the floor of balconies, whose structure is connected to the UXC cavern ground.

Throughout the production an extensive quality assurance (QA) program has been implemented. This was initiated in Florence and Torino and continued at CERN with the support of the Catania, Bari and Torino INFN groups.

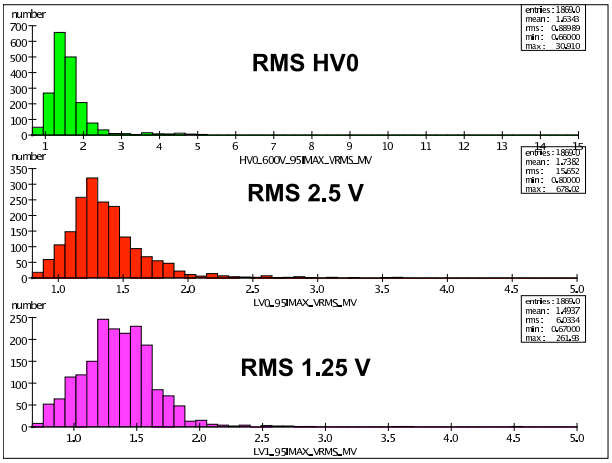

Figure 1: Distribution of RMS noise (mV) as obtained from QA tests on HV, 2.5V and 1.25V channels of production A4601H.

Reception tests are performed on received boards through an automated "test equipment" [5], which conditions and measures at different working points each PSU channel. Among the tests performed:

- channel switch ON procedure, voltage delivery compliance at various current loads, ramp-up and ramp-down procedures;
- efficiency measurement on the LV channels. Efficiency has to be higher than 70 % at 85 % of the maximum load;
- crow-bar circuit intervention and tolerance to sudden current transitions. This is implemented by simulating a current step function of 3 A amplitude (by means of dynamic loads);
- noise measurement: the RMS measured on each channel has to be lower than 3.75 mV for LV channels and 7.5 mV for HV channels;
- functionality of the interlocks.

Figure 1 shows the RMS measured on 2.5V, 1.25V and HV channels on substantial part of the production. Noise distributions are centered around 1.5 mV and within specification limits.

After the QA reception tests, A4601H and A4602 boards are submitted to the burn-in procedure before they can be accepted for installation. Boards are run at the edge of their power ($i_{2.50}$ = 10A, $i_{1.25}$ = 6A, i_{HV} = 10 mA) using special resistive loads. Each board has to sustain 36 h of burn-in in 3 cycles of uninterrupted functioning. In addition, also interlock and ON/OFF stress tests are performed. The burn-in setup built at CERN is able to test up to 50 PSMs at a time; load cards and PSMs occupy four cooled racks.

V. POWER CABLES

Power cables have to cover a total distance of roughly 50 m from the PSMs (CPSMs) down to the tracker structures. The connection is made by two tracks: one 28-56m long cable placed mostly outside the CMS detector volume, and one $\simeq$ 6 m long track lying entirely inside the volume [4]. The two parts are connected at the periphery of the CMS detector, in the so-called "patch panel 1" (PP1) regions, through interconnection boards. In total there are 16 tracker PP1 regions per detector half-end; each PP1 holds 10 interconnect-boards, 2 reserved for power control cables and 8 for detector power cables.

Inside the tracker volume cables of various diameters with Aluminum power conductors are deployed (Aluminum "Multi Service Cables"), while outside copper conductors are used. Power Long Control Cables (PLCC) deliver the control power to the CCU-rings. They are standard multi-wire cables, with different designs and dimensions for TIB/TID, TOB and TEC detectors.

A special "Low Impedance Cable" (LIC), designed and developed by the Florence CMS group, is used for the power groups. This cable uses 50 enameled 0.6 mm^2 copper wires for the LV power, arranged in two concentric layers and placed in such a way that any 2.5 V (1.25 V) wire is flanked by two Return wires. The result is low inductance ($\simeq$ 13 nH/m), high capacitance ($\simeq$ 7 nF/m) and low resistance (1.25, 1.73, 4.44 $m\Omega/m$ respectively on Return, 2.5 V and 1.25 V lines), which ensure very good performances even at large distances. At the center of the cable ten twisted pairs provide HVs, sense connections and other services required. An external braided wire shields the cable conductors.

The enameled conductors have proven to have no relevant mechanical problems for this kind of application. The wires are class 180, grade 2, with minimum 30 μm enamel thickness. The single wire resistance at 20 ^{0}C is 31 mΩ /m. The enamel is based on polyurethane, which meets the requirements for LHC.

The certified working voltages of the LIC cable are 600 V for the twisted pairs and 30 V for LV conductors. The minimum bending radius is 80 mm.

LIC cable prototypes were produced at various stages and successfully used in several beam tests and detector integration setups. Around 2500 "production" LIC cables have been manufactured, for a total length of $\simeq$ 85km. Two companies, Novacavi S.p.A. and Elettronica Conduttori S.r.l., assembled the cables, while Thermo Engineering S.r.l. performed the connectorization.

A detailed QA program was performed throughout the cable procurement. Table 5 summarizes the tests performed on each cable spool, before cutting to individual lengths. The tested voltages largely exceed the certified working voltages. Destructive tests are also performed, on a sample basis, for each production

lot: after producing some severe mechanical stress ("U" bending, crushing, traction) the perforation voltage of the conductors is measured and required to be higher than 1000 V_{DC} for LV wires and higher than 10000 V_{AC} for the other conductors.

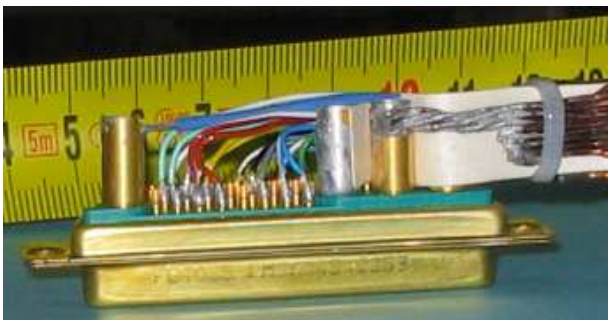

Figure 2: Connectorization of a LIC cable.

The connectorization technique for enameled wires was developed. Enameled wires are shaped into three bundles (one per conductor, 2.5V, 1.25V and RTN). Each bundle is bathed in tin/lead at 390 ^{0}C . The bath dissolves the enamel and provides soldering of the wires within the bundle. Both the temperature and the duration are important in order to obtain good electrical contact. Bundles are then shaped to fit the pins in the appropriate connectors. Aramidic paper is used to secure isolation between bundles. The twisted-pair wires are subsequently connected and the entire connector is molded with a polyurethane-based compound (RAKO-PUR by Rampf).

Accurate reception tests are performed on connectorized cables. Continuity and isolation are tested. The resistance along the LV lines is accurately measured and required to be within 10% of the expected value.

The cable production rate reached 120 cables/week. The initial throughput ($\simeq$ 90%) raised to over 99 % during production, when the soldering process was further refined.

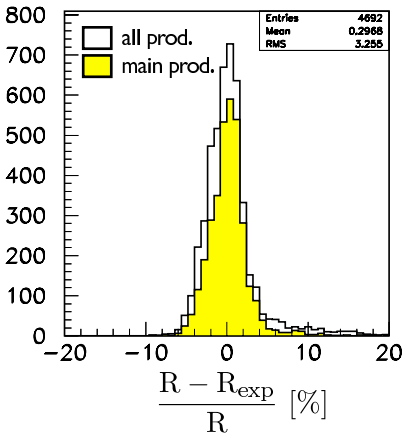

Figure 3: Relative difference [%] between the measured resistance of the LV conductors and the resistance expected; cables pass the acceptance criteria when this difference is lower than 10%. The yellow histogram represents data relative to the bulk of the cable production, when connectorization procedure was refined.

Table 5: LIC cable quality assurance tests. R_{exp} is the resistance expected on the basis of the cable length.

type	value	description
tests performed before connectorization:		
isolation	3000 V	twisted pairs
isolation	250 V	enam. wires
Traction	820 N / 60 s	(destructive test)
"U" shape bends	75 mm radius	200 cycles (destr. test)
"U" shape bends	20 mm radius	5 cycles (destr. test)
Crush	150 kg / 80 mm	(destr. test)
tests performed after connectorization:		
resistance	$R - R_{exp} < 10\%$	2.5, 1.25 and RTN lines
continuity	$R < 10\Omega$	twisted pairs and shield
isolation	$R > 100M\Omega$ at250V	2.5, 1.25 and RTN lines
isolation	$R > 1G\Omega$ at1000V	twisted pairs and shields

VI. Conclusions

The power system for the CMS silicon strip tracker is a huge modular system providing $\simeq$ 2500 complex channels with LV and HV regulators powering the detectors and the control circuitry. Good electrical isolation of the channels, full remote control and robust, hard-wired safeguard system are the guidelines followed in its implementation. An extensive quality assurance program has been fulfilled during the production of its components, and it is presently being installed and commissioned. An innovative "low impedance" cable, featuring low inductance, high capacitance and low DC resistance, is used to route the power to the detector.

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